GENERAL DESCRIPTION

The SP6650 is ideal for portable applications that use a Li-Ion or 3 to 4 cell alkaline/NiCd/NiMH input. The SP6650 extends battery life with it's unique control loop scheme (patent pending), which maintains high efficiency levels (> than 90%) over a wide range of output currents. Features such as Inductor peak current control, protects the power supply from overload or short circuit conditions, controls the startup current to prevent output overshoot and excessive battery drop, and gives the user more flexibility in choosing an appropriate coil to optimize solution cost, size and performance. Other features include a dedicated pin for manual shutdown, a battery low indicator, and thermal protection.

The SP6650 is offered in a RoHS compliant, lead free 10-pin MSOP package.

APPLICATIONS

- **PDA**
- **CD Player**
- **ADSL Modem**
- **Digital Still Camera**

FEATURES

- **95% High Efficiency**
- **Proprietary Control Loop**
- **2.7V to 6.5V Input Voltage Range**
- **3.3V or Adjustable Output Voltage Range**
- **2% Output Voltage Accuracy**
- **600mA Output Current**
- **100% Duty Cycle Operation**
- **Programmable Inductor Peak Current Limit (0.95A or 0.5A)**
- **No External FET's Required**
- **3V Battery Low Indicator**
- **2.7V Undervoltage Lockout**
- **Shutdown Control**
- **Small 10-Pin MSOP**

TYPICAL APPLICATION DIAGRAM

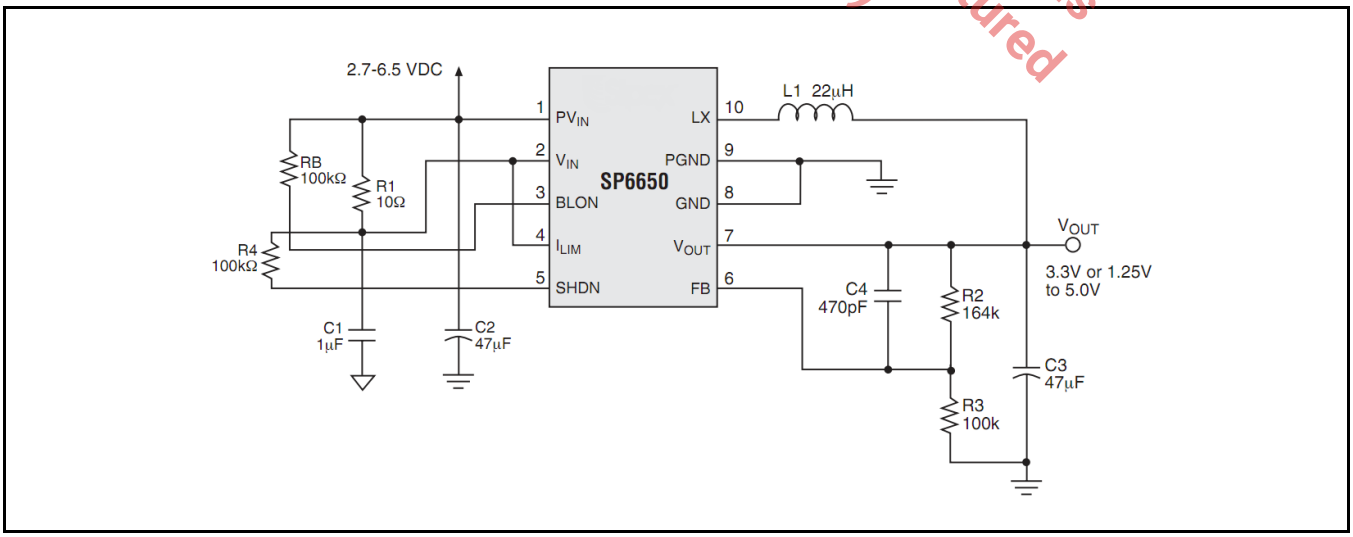


Fig. 1: SP6650 Application Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

PV_{IN}, V_{IN} 7.0V
All Other Pins .....-0.3V to V_{IN} +0.3V
PV_{IN}, PGND, LX Current 2A
Storage Temperature ..... -65°C to 150°C

OPERATING RATINGS

Input Voltage Range V_{IN}..... UVLO to 6.5V
Ambient Temperature..... -40°C to +85°C

ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{LIM} = SHDN = V_{IN}, FB = GND, L_1 = 22µH, C_{IN} = C_{OUT} = 47µF, T_A= –40°C to 85°C.

Parameter	Min.	Typ.	Max.	Units		Conditions
Input Voltage Operating Range	UVLO		6.5	V	•	
Undervoltage Lockout Threshold	2.6	2.7	2.8	V	•	V_{IN} Rising
Undervoltage Lockout Hysteresis		120		mV	•	
FB Set Voltage, V_{REF}	1.23	1.25	1.27	V	•	V_{OUT} tied to FB Pin
V_{REF} Load Regulation		0.5		%	•	I_{LOAD} = 0 to 600mA V_{IN} = 3.6V, V_{OUT} = 3.3V
V_{REF} Line Regulation		0.5		%	•	V_{IN} = 3.6V to 6.5V V_{OUT} = 3.3V, I_{LOAD} = 200mA
V_{REF} Line and Load Regulation		0.65		%	•	V_{IN} = 3.6V to 6.5V I_{LOAD} = 0 to 600mA
V_{OUT} Accuracy	3.23	3.30	3.37	V	•	I_{LOAD} = 100mA, V_{IN} = 3.6V
V_{OUT} Line and Load Regulation	3.17	3.30	3.43	V	•	V_{IN} = 3.6V to 6.5V I_{LOAD} = 0 to 600mA
On-Time Constant - K_{ON} Minimum T_{ON} = K_{ON}/ (V_{IN}-V_{OUT})		2.7		µs*V	•	
PMOS Switch Resistance		0.4	0.8	Ω	•	I_{PMOS} = 200mA
NMOS Switch Resistance		0.3	0.8	Ω	•	I_{NMOS} = 200mA
V_{IN} Pin Quiescent Current		70	150	µA	•	SHDN = V_{IN} = FB = 1.5V
V_{IN} Pin Shutdown Current		0.3	500	nA	•	SHDN = 0V
V_{OUT} Pin Quiescent Current		7	12	µA	•	SHDN = V_{IN} = FB = 1.5V
V_{OUT} Pin Shutdown Current		0.1	500	nA	•	SHDN = 0V
Power Efficiency		92 95 88		% % %	•	I_{LOAD} = 600mA I_{LOAD} = 100mA I_{LOAD} = 1mA
Minimum Guaranteed Load Current	600 300	700 350		mA mA	•	I_{LIM} = V_{IN} I_{LIM} = 0V
Inductor Current Limit	0.75 0.40	0.95 0.50	1.15 0.60	A A	•	I_{LIM} = V_{IN} I_{LIM} = 0V
Inductor Current Limit		-100		ppm/ °C	•	
Falling BLON Trip Voltage	2.88	3.00	3.12	V	•	
BLON Trip Voltage Hysteresis		2.9		%	•	
BLON Low Output Voltage			0.4	V	•	V_{IN} = V_{OUT} = 3.0V, I_{SINK} = 1mA
BLON Leakage Current			1	µA	•	V_{BLON} = 3.3V

Parameter	Min.	Typ.	Max.	Units		Conditions
Rising Over-Temperature Trip Point		140		°C	•	
Over-Temperature Hysteresis		14		°C	•	
SHDN, ILIM Leakage Current		1	500	nA	•	
SHDN, ILIM Input Threshold Voltage	0.60	0.90	1.8	V	•	High to Low Transition
	0.60	1.25	1.8			Low to High Transition

BLOCK DIAGRAM

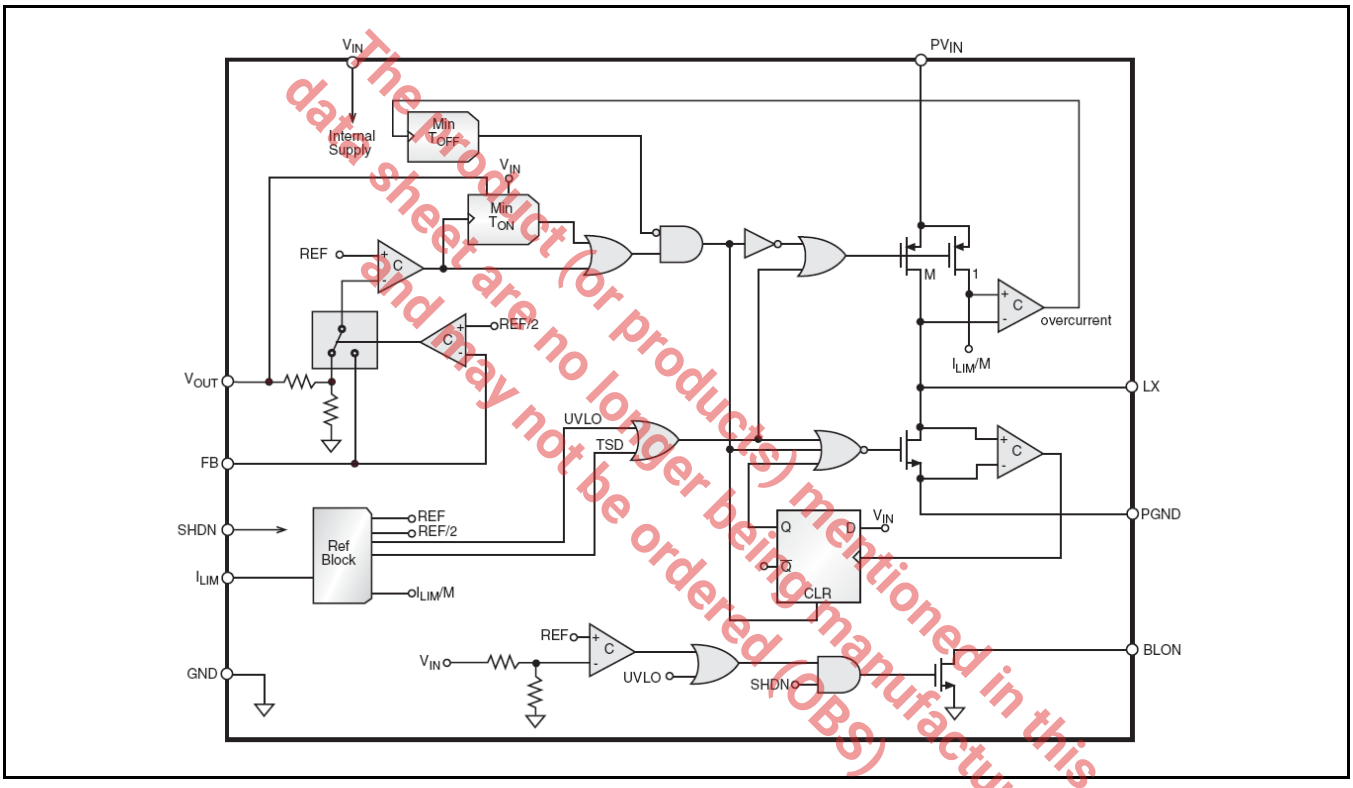


Fig. 2: SP6650 Block Diagram

PIN ASSIGNMENT

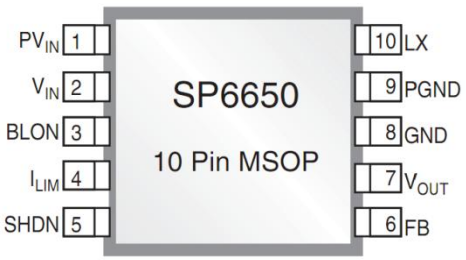


Fig. 3: SP6650 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
PV_{IN}	1	Input voltage power pin. Inductor charging current passes through this pin.
V_{IN}	2	Internal supply voltage. Control circuitry powered from this pin.
BLON	3	Open drain battery low output. V_{IN} below battery low threshold pulls this node to ground. V_{IN} above threshold, this node is open.
I_{LIM}	4	Inductor current limit programming pin. Tie pin to V_{IN} for 0.95A peak inductor current limit. Tie pin to ground for 0.5A peak inductor current limit. TTL input threshold.
SHDN	5	Shutdown control input. Tie to V_{IN} for normal operation, tie to ground for shutdown. TTL input threshold.
FB	6	External feedback network input connection. Connect a resistor from FB to ground and FB to V_{OUT} to control the output voltage externally. This pin regulates to the internal bandgap reference voltage of 1.25V. Tie FB to ground to use the internal divider for a preset output voltage of 3.3V.
V_{OUT}	7	Output voltage sense pin. Used for internal feedback divider and timing circuit.
GND	8	Internal ground pin. Control circuitry returns current to this pin.
PGND	9	Power ground pin. Synchronous rectifier current returns through this pin.
LX	10	Inductor switching node. Inductor tied between this pin and the output capacitor to create regulated output voltage.

ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
SP6650EU-L	-40°C≤T_A≤+85°C	6650 EXXX YWW	10-pin MSOP	Bulk	Lead Free	
SP6650EU-L/TR				2.5K/Tape & Reel		
SP6650UEB	SP6650 Evaluation Board					

"YY" = Year – "WW" = Work Week – "X" = Lot Number; when applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

Schematic and BOM from Application Information section of this datasheet.

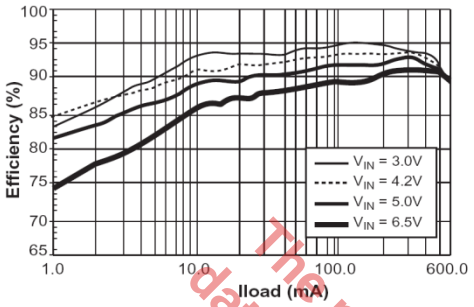


Fig. 4: Efficiency vs. Output Current, V_{OUT} = 3.3V, L1 = 22µH (Sumida CDRH6D28), I_{LIM} = V_{IN}

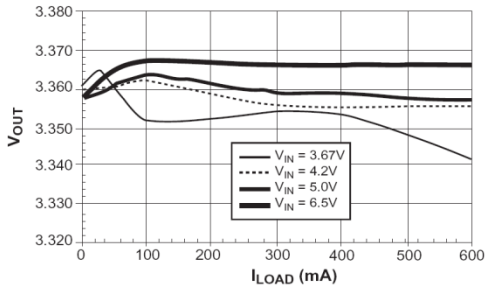


Fig. 5: Line/Load Rejection, V_{OUT} = 3.3V, L1 = 22µH (Sumida CDRH6D28), I_{LIM} = V_{IN}

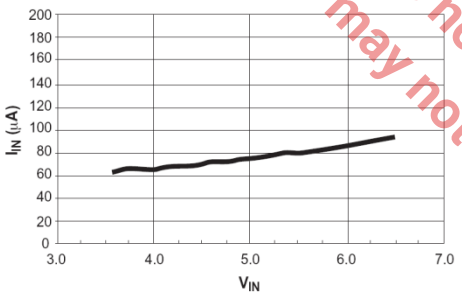


Fig. 6: No Load Battery Current, V_{OUT} = 3.3V, L1 = 22µH (Sumida CDRH6D28), I_{LIM} = V_{IN}

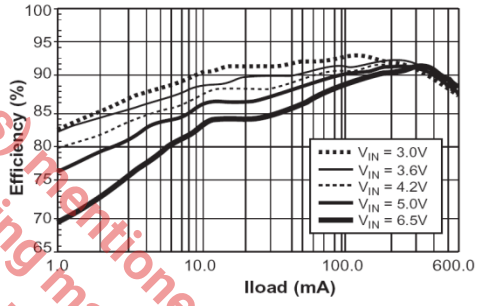


Fig. 7: Efficiency vs. Output Current, V_{OUT} = 2.5V, L1 = 22µH (Sumida CDRH6D28), I_{LIM} = V_{IN}

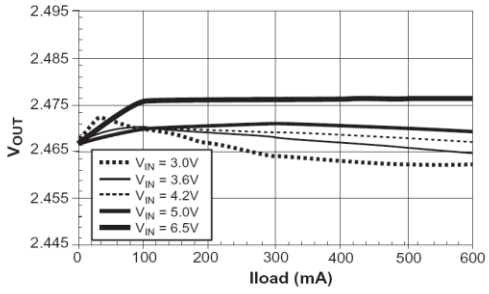


Fig. 8: Line/Load Rejection, V_{OUT} = 2.5V, L1 = 22µH (Sumida CDRH6D28), I_{LIM} = V_{IN}

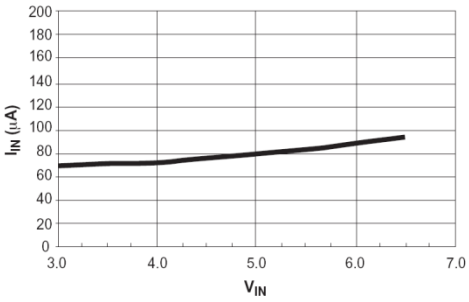


Fig. 9: No Load Battery Current, V_{OUT} = 2.5V, L1 = 22µH (Sumida CDRH6D28), I_{LIM} = V_{IN}

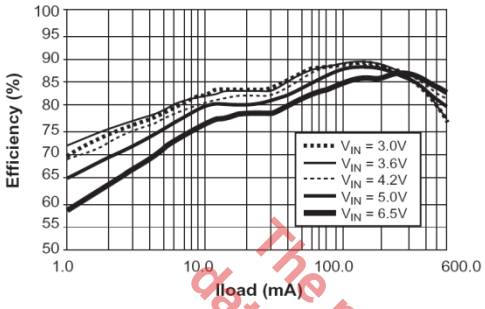


Fig. 10: Efficiency vs. Output Current, V_{OUT} = 1.25V, L1 = 22µH (Sumida CDRH6D28), $I_{LIM} = V_{IN}$

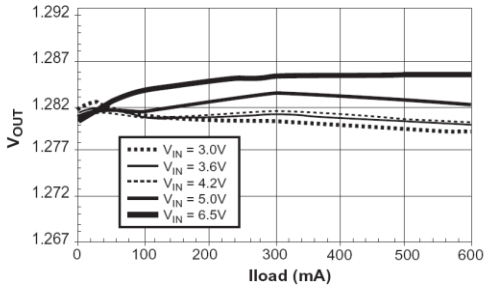


Fig. 11: Line/Load Rejection, V_{OUT} = 1.25V, L1 = 22µH (Sumida CDRH6D28), $I_{LIM} = V_{IN}$

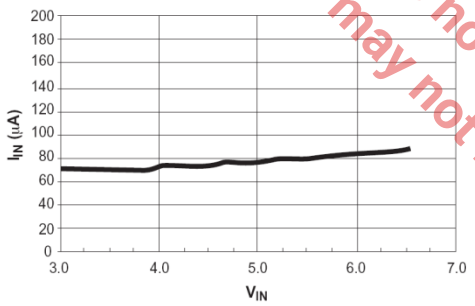


Fig. 12: No Load Battery Current, V_{OUT} = 1.25V, L1 = 22µH (Sumida CDRH6D28), $I_{LIM} = V_{IN}$

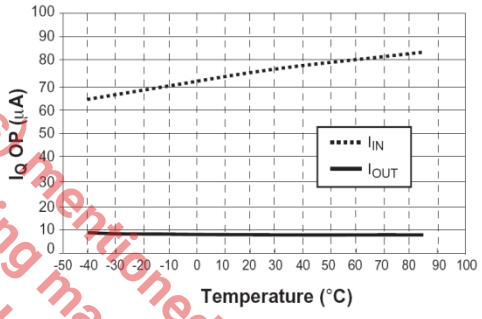


Fig. 13: Quiescent Current vs. Temperature. V_{IN} = 3.6V, SHDN = V_{IN} (Enabled)

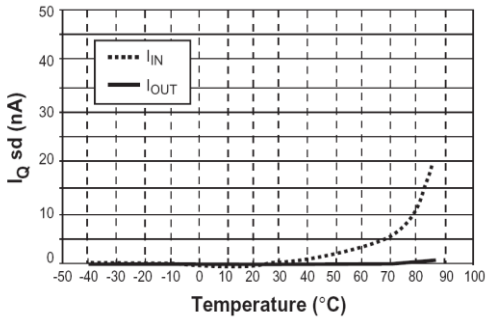


Fig. 14: Quiescent Current vs. Temperature. V_{IN} = 3.6V, SHDN = GND (Shutdown)

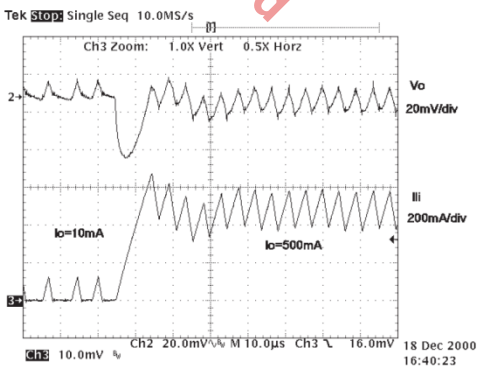


Fig. 15: Load Step Transient Response, V_{OUT} = 2.5V, 10mA to 500mA. L1 = 22µH (Sumida CDRH6D28), $I_{LIM} = V_{IN}$

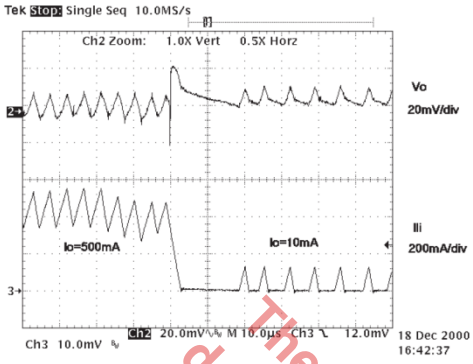


Fig. 16: Load Step Transient Response, V_{OUT} = 2.5V, 500mA to 10mA. L1 = 22µH (Sumida CDRH6D28), I_{LIM} = V_{IN}

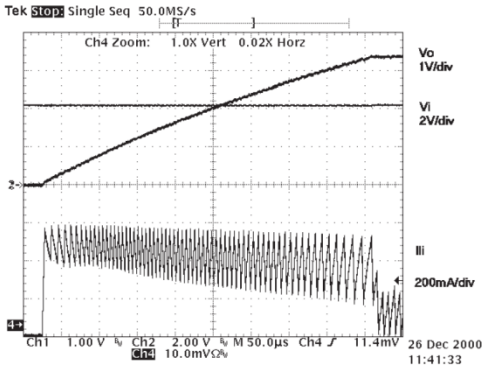


Fig. 17: Low I_{LIM} Startup, V_{IN} = 4.2V, VOUT = 3.3V. I_{LIM} tied to GND, Internal Feedback R_{LOAD} = 33Ω.

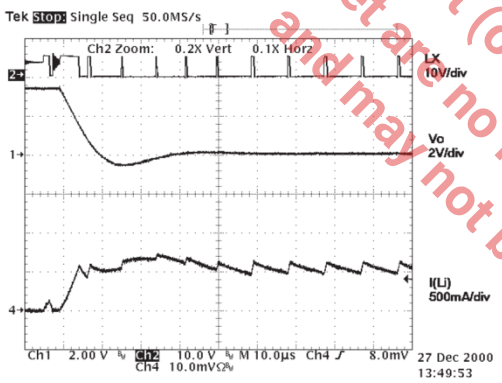


Fig. 18: Dead Short. V_{IN} = 5.0V, I_{LIM} tied to GND. Start I_{OUT} = 37mA, V_{OUT} = 3.3V. Finish I_{OUT} = 500mA, V_{OUT} = 20mV.

THEORY OF OPERATION

The SP6650 is a synchronous buck regulator with an input voltage range of +2.7V to +6.5V and an output that is either preset to +3.3V, or adjustable between +1.25V and VIN. The SP6650 features a unique on-time control loop that runs in discontinuous conduction mode (DCM) or continuous conduction mode (CCM) using synchronous rectification. Other features include overtemperature shutdown, overcurrent protection, undervoltage lockout, digitally controlled enable, a battery low indicator, and an external feedback pin.

The SP6650 operates with a light load quiescent current of 70µA using a 0.4Ω PMOS main switch and a 0.3Ω NMOS auxiliary switch. It operates with excellent efficiency across the entire load range, making it an ideal solution for battery powered applications and low current step-down conversions. The part smoothly transitions into a 100% duty cycle under heavy load/low input voltage conditions.

ON-TIME CONTROL

The SP6650 uses a precision comparator and a minimum on-time one-shot to regulate the output voltage and control the inductor current under normal load conditions. As the feedback node (negative terminal of the loop comparator) drops below the reference, the loop comparator output goes high and closes the main switch. The minimum on-time one shot is triggered, setting a logic high for the duration defined by:

$$T_{ON} = \frac{K_{ON}}{V_{IN}-V_{OUT}}$$

where:

K_{ON} = 2.7µs*V constant

V_{IN} = V_{IN} pin voltage

V_{OUT} = V_{OUT} pin voltage

The outputs of the loop comparator and the ontime one shot are OR'd together, inverted, and buffered to drive the gate of the high side PMOS main switch. Increasing inductor current causes the output to increase through the ESR (equivalent series resistance) of the output capacitor. As V_{OUT} rises above the regulation threshold, the loop comparator output resets low. Termination of the on cycle occurs when both the loop comparator and the on-time one shot goes to logic low, or the inductor current limit has been reached.

The discharge phase follows with the high side PMOS switch opening and the low side NMOS switch closing to provide a discharge path for the inductor current. The decreasing inductor current and the load current cause the output voltage to droop. Under normal load conditions when the inductor current is below the programmed limit, the off-time will continue until the output voltage falls below the regulation threshold, which initiates a new charge cycle via the loop comparator.

The inductor current "floats" in continuous conduction mode. During this mode the inductor peak current is below the programmed limit and the valley current is above zero. This is to satisfy load currents that are greater than half the minimum current ripple. The current ripple, I_{LR}, is defined by the equation:

$$I_{LR} \approx \frac{K_{ON}}{L} * \frac{V_{IN}-V_{OUT}-I_{OUT}*Rch}{V_{IN}-V_{OUT}}$$

where:

L = Inductor value

I_{OUT} = Load current

Rch = PMOS on resistance, 0.4Ω typ.

If the I_{OUT}*Rch term is negligible compared with (V_{IN}-V_{OUT}), the above equation simplifies to:

$$I_{LR} \approx \frac{K_{ON}}{L}$$

For most applications, the inductor current ripple controlled by the SP6650 is constant regardless of input and output voltage. Because the output voltage ripple is equal to:

$$V_{OUT}(ripple) = I_{LR}*R_{ESR}$$

where:

R_{ESR} = ESR of the output capacitor

the output ripple of the SP6650 regulator is independent of the input and output voltages. For battery powered applications, where the battery voltage changes significantly, the SP6650 provides constant output voltage ripple throughout the battery lifetime. This greatly simplifies the LC filter design.

ON-TIME CONTROL: CONTINUED

The maximum loop frequency in CCM is defined by the equation:

$$F_{LP} \approx \frac{(V_{IN}-V_{OUT})*(V_{OUT}+I_{OUT}*Rdc)}{K_{ON}*[V_{IN}+I_{OUT}*(Rdc-Rch)]}$$

where:

F_{LP} = CCM loop frequency

Rdc = NMOS on resistance, 0.3Ωtyp.

Ignoring conduction losses simplifies the loop frequency to

$$F_{LP} = \frac{1}{K_{ON}} * \frac{V_{OUT}}{V_{IN}} * (V_{IN}-V_{OUT})$$

OR'ing the loop comparator and the on-time one shot reduces the switching frequency for load currents below half the inductor ripple current. This increases light load efficiency. The minimum on-time insures that the inductor current ripple is a minimum of K_{ON}/L, more than the load current demands. The converter goes in to a standard pulse frequency modulation (PFM) mode where the switching frequency is proportional to the load current.

LOW DROPOUT AND LOAD TRANSIENT OPERATION

OR'ing the loop comparator also increases the duty ratio past the ideal $D=V_{OUT}/V_{IN}$ up to and including 100%. Under a light to heavy load transient, the loop comparator will hold the main switch on past the on-time one shot pulse until the output is brought back into regulation. Also, as the input voltage supply drops down close to the output voltage, the main MOSFET resistance loss will dictate a much higher duty ratio to regulate the output. Eventually as the input voltage drops low enough, the output voltage will follow, causing the loop comparator to hold the converter at 100% duty cycle. This mode is critical in extending battery life when the output voltage is at or above the minimum usable input voltage. The dropout voltage is the minimum (V_{IN} - V_{OUT}) below which the output regulation cannot be maintained. The dropout voltage of SP6650 is equal to I_L (0.4Ω + R_L) where 0.4Ω is the typical $R_{DS(ON)}$ of the P-Channel MOSFET and R_L is the DC resistance of the inductor.

The on-time control circuit seamlessly operates the converter between CCM, DCM, and low dropout modes without the need for compensation. The converter's transient response is quick since there is no compensated error amplifier in the loop.

INDUCTOR OVER-CURRENT PROTECTION

The inductor over-current protection circuitry is programmed to limit the peak inductor current to 950mA (pin 4 tied to V_{IN}) or 500mA (pin 4 to ground). This is done during the on-time by comparing the source to drain voltage drop of the PMOS passing the inductor current with a second voltage drop representing the maximum allowable inductor current. As the two voltages become equal, the over-current comparator triggers a minimum off-time one shot. The off-time one shot forces the loop into the discharge phase for a minimum time causing the inductor current to decrease.

At the end of the off-time loop, control is handed back to the OR'd on-time signal. If the output voltage is still low, charging begins until the output is in regulation or the current limit has been reached again. During startup and overload conditions, the converter behaves like a current source at the programmed limit minus half the current ripple. The minimum T_{OFF} is 6µs (typ.) at V_{OUT} = 0V and 2µs (typ.) for V_{OUT} greater than 1.5V.

UNDER-VOLTAGE LOCKOUT

The SP6650 is equipped with under-voltage lockout to protect the input battery source from excessive currents when substantially discharged. When the input supply is below the UVLO threshold both power switches are

open to prevent inductor current from flowing. The internal reference and regulator circuitry are enabled drawing the 70µA light load quiescent current on pin 2. The rising input voltage UVLO threshold is +2.7V, with a typical hysteresis of 120mV to prevent chattering due to the impedance of the input source.

UNDER-CURRENT DETECTION

The synchronous rectifier is comprised of the inductor discharge switch, a voltage comparator, and a latch. During the off-time, positive inductor current flows into the PGND pin 9 through the low side NMOS switch to LX pin 10, through the inductor and the output capacitor, and back to pin 9. The comparator monitors the voltage drop across the discharge NMOS. As the inductor current approaches zero, the channel voltage sign goes from negative to positive, causing the comparator to trigger the latch and open the switch to prevent inductor current reversal. This circuit along with the ontime one shot puts the converter into PFM mode and improves light load efficiency when the load current is less than half the inductor ripple current defined by K_{ON}/L.

THERMAL SHUTDOWN

The converter will open both power switches if the die junction temperature rises above 140°C. The die must cool down below 126°C before the regulator is re-enabled. This feature protects the SP6650 and surrounding circuitry from excessive power dissipation due to fault conditions.

SHUTDOWN/ENABLE CONTROL

Pin 5 of the device is a logic level control pin that shuts down the converter with a logic low, or enables the converter with a logic high. When the converter is shut down, the power switches are opened and all circuit biasing is extinguished leaving only junction leakage currents on supply pins 1 and 2. After pin 5 is brought high to enable the converter, there is a turn on delay to allow the regulator circuitry to re-establish itself. Power conversion begins with the assertion of the internal reference ready signal which occurs approximately 150µs after the enable signal is received.

BATTERY LOW INDICATOR

The regulator bias voltage on pin 2 (V_{IN}) is divided down and compared to the internal +1.25V reference voltage. When pin 2 voltage drops below +3.00V, an open drain NMOS on pin 3 (BLON) sinks current to ground. Tying a resistor from pin 3 to V_{IN} or V_{OUT} creates a logic level battery low indicator. A low bandwidth comparator and 2.9% hysteresis filter the input voltage ripple to prevent noisy transitions at the threshold.

EXTERNAL FEEDBACK PIN

The SP6650 comes with a factory preset output voltage of +3.3V when pin 6 (FB) is grounded. Otherwise, the output voltage can be externally programmed within the range +1.25V to +5.0V by tying a resistor from FB to ground and FB to V_{OUT} (pin7). See the applications section for resistor selection information.

APPLICATION INFORMATION

EXTERNAL COMPONENT SELECTION

Inductor

According to the pulse frequency modulation (PFM) algorithm, the peak to peak output ripple current can be calculated as:

$$I_{LR} \approx \frac{K_{ON}}{L}$$

K_{ON} = 2.7µs*V is a constant for SP6650 and is set by the parameters of the internal ON-time calculation circuitry. For the recommended 22µH inductor, typical ripple currents are ILR = 123mA in discontinuous conduction mode (DCM) operation. During continuous conduction mode, the speed of the loop comparator determines the current ripple. It is approximately equal to 200mA with a 22µH inductor.

The value of the inductor is chosen based on the constant KON and acceptable current ripple. Two additional inductor parameters are important: its current rating and its DC resistance.

When the current through the inductor reaches the level of I_{sat}, inductance drops down to 70% from the nominal. This non-linear change can cause stability problems or excessive fluctuation in current ripple. To avoid this, the inductor should be chosen with saturation current at least equal to the maximum output current of the converter plus half of the ripple. To provide the best converter performance in dynamic conditions such as start-up and load transients, inductors with saturation current close to the chosen I_{LIM} are recommended.

The second important inductor parameter, DC resistance, directly defines the efficiency of the converter, therefore, the inductor should be chosen with the minimum possible DC resistance for a particular design. Recommended types of the inductors for different applications are given in Table 1. Preferred inductors for on board power supplies with the SP6650 converter are shielded inductors to minimize radiated magnetic fields emissions.

All components recommended for typical designs like those shown in the applications schematics are given in Table 1.

Input and Output Capacitors

Output capacitor is often selected based on the requirement on the output ripple voltage. In a Buck regulator, the output ripple is determined by ESR (equivalent series resistor) of the output capacitors and inductor ripple current

$$V_{OR} = ESR * I_{LR},$$

where VOR = peak to peak output ripple voltage.

SP6650's adaptive on-time scheme provides a constant inductor ripple that is independent of input voltages and thus makes it easier to select the output capacitor. In many power supply designs, the ripple voltage needs to be less than 3% of the DC output voltage. Using low ESR tantalum or electrolytic capacitors to reduce the output ripple.

Due to the nature of the PFM control, certain output ripple is required for stable operation. The loop comparator requires minimum of 15mV ripple on the FB pin to reliably toggle the comparator output. That translates to an output ripple of

$$V_{OR(MIN)} = \frac{15mV * V_{OUT}}{V_{REF}}$$

where V_{REF} = 1.25V is the internal reference voltage.

To reduce the output ripple and improve stability, a small capacitor can be paralleled with the feedback voltage divider as shown on page 1. This capacitor forms a high pass filter with feedback resistor to increase the ripple voltage seen by the FB pin. The value of the capacitor should be in the range of 100pF to 500pF. Although the 3.3V output can be programmed simply by connecting the FB pin to the ground, using this external feedback scheme can significantly reduce the output ripple. For output ripples less than 15mV, for instance when ceramic capacitors are used, an

artificial ramp can be generated and superimposed onto the output.

The schematic and description is shown in Additional Application Circuits.

Another function of the output capacitor is to hold up the output voltage during the load transient, and thus prevent excessive overshoot and undershoot. For that, the recommended capacitor value is greater than 22uF.

An input capacitor can reduce the peak current drawn from the battery, improve efficiency, and significantly reduce high frequency noises induced by a switching power supply. The applicable capacitors are tantalum, electrolytic and ceramic capacitors. An RC filter is recommended on the V_{IN} pin (pin 2) to effectively cut down the noise which can impact the IC control circuit. The time constant of the RC filter needs to be at least 5 times higher than the switching period, calculated as $1/F_{LP}$ during CCM.

Output Voltage Programming

The output voltage can be programmed by the external voltage divider as shown on page 1. First pick a resistor value less than 100k for R3. A large R3 value would reduce the AC voltage seen by the loop comparator because the FB pin capacitance (can be as high as 10pF) can form a low pass filter with R3 paralleling with R2. Lack of AC voltage to the loop comparator would give rise to pulse jittering and higher output ripple. Once the R3 value is picked, R2 can be calculated from

$$R_2 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) R_3$$

Designation	Description	Manufacturer	Part Number	Comments
INDUCTOR L1	22µH/0.77Arms/0.104DCR	TDK	SLF7030T-220MR86	Shielded
	22µH/1.1Arms/0.071DCR	Murata	LQS66C220M04	
	22µH/0.095DCR	Sumida	CDRH6D28	Shielded
	47µH/0.76Arms/0.15DCR	Murata	LQS66C470M04	Shielded
	47µH/0.72Arms/0.37DCR	Sumida	CR54	
C2, C3, Input, Output filter Capacitors	47µF/350mΩ/500mA	Nemco	LSR47/10C-350	
	47µF/350mΩ/500mA	AVX	TPSC476010R0350	
	33µF/375mΩ/542mA	AVX	TPSC336010R0375	
	22µF/700mΩ/348mA	AVX	TPSB226010R0700	
R2, R3	100K/63mW/1% tolerance	Any Approved		Any package 0402, 0505, 0603, etc…
R1	10/63mW/5% tolerance			

Table 1

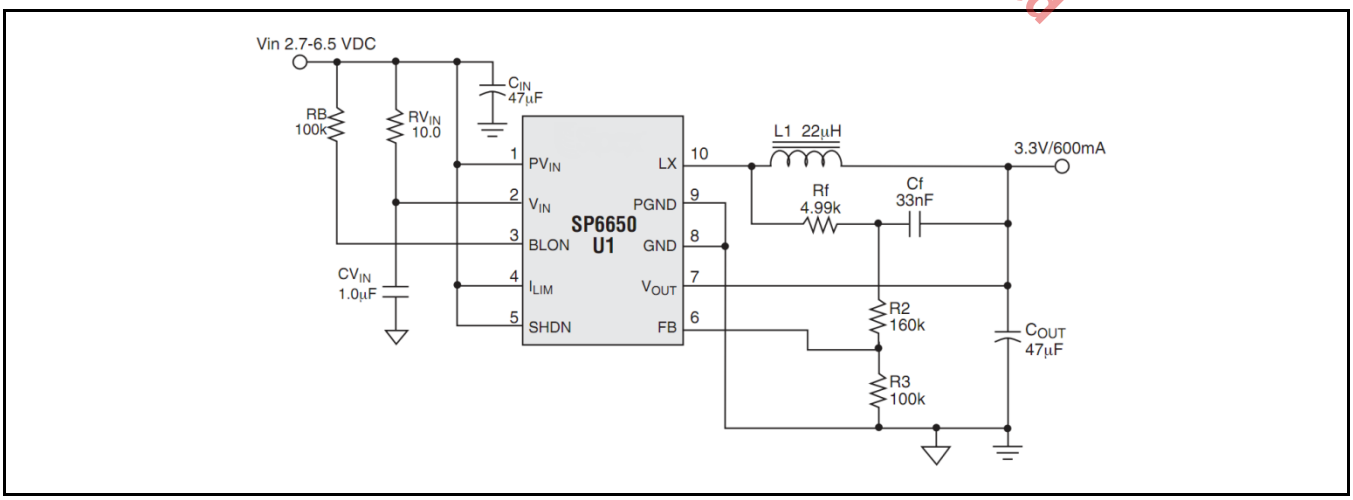


Fig. 19: Additional Application Circuit with Low Output Ripple

The additional Rf/Cf network used in Figure 19 generates an artificial ramp from the LX pin voltage and superimposes it to the feedback pin. As a result, the internal loop comparator doesn't have to rely on output ripple to run PFM. Now low ESR output capacitors, such as ceramic capacitors, can be used, and the output ripple can be reduced by two to three times. For the best result, size the Cf and Rf values so the network would introduce 10 to 30mV ripples to the FB pin. Oversized ripple would compromise the load regulation and also cause oscillation during load transient. Load transient response and output ripples from Figure 16 circuit are shown in Figure 20 and Figure 21, respectively. The added ripple voltage can be calculated from

$$\Delta V = \frac{K_{ON}}{RfCf}$$

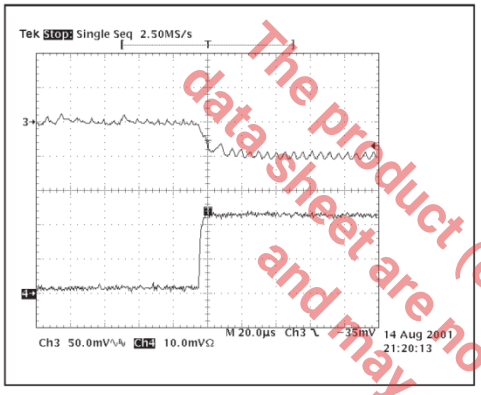


Fig. 20 V_{OUT} transient response from 50mA to 500mA load step. CH1- V_{OUT}, CH4 - I_{LOAD}

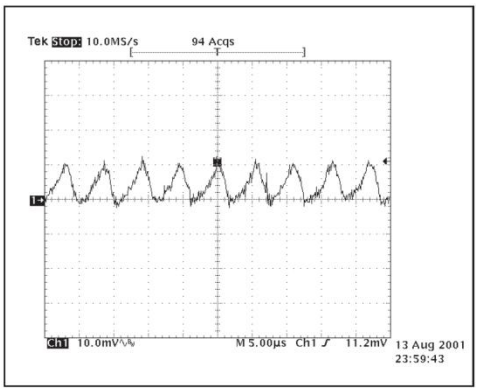


Fig. 21 Output ripple CH1-output ripple. V_{IN} = 5, V_{OUT} = 3.3V, I_{LOAD} = 600mA

SP6650 can also be configured with few external components to achieve buck-boost voltage conversion. Efficiency of 75% to 87% can often be obtained depending on the load current and output voltage. Figure 22 and Figure 23 demonstrate two typical applications in which the USB input is converted to a 12V and a well regulated 5V.

The operation of the circuit is as follows. When the internal high side PMOS turns on, the LX pin swings to the input voltage which turns on the external NMOS Q1. A voltage equal to Vin is then applied to the inductor to cause the inductor current rise linearly. Since there's no current delivered to the output, the output capacitor is discharged by the load current. Therefore, the internal PMOS can be only turned off by the over-current comparator since the loop comparator would never toggle during this state. When the internal PMOS is open, the internal low side NMOS is turned on. This pulls the LX pin to the ground and turns off the Q1. As a result, the Schottky D2 is forward biased and conducts the inductor current to the output. Now the inductor experiences a reversed voltage equal to V_{OUT} and its current ramps down linearly. As expressed in the Operation section under Inductor Over-Current Protection, a minimum T_{OFF} timer is activated after the over-current comparator is triggered in the previous state. Before T_{OFF} expires, the internal PMOS will not turn on, and the inductor will not be recharged even when the output voltage drops below the regulation voltage. This reduces the maximum load current that can be delivered by this circuit. Since T_{OFF} is reverse proportional to the V_{OUT} pin voltage, the V_{OUT} pin is pulled up using a voltage divider tying to the input voltage. As a result, a 5V to 12V conversion can provide maximum 120mA load. This buck-boost circuit can regulate an output voltage higher, lower or equal to the input voltage.

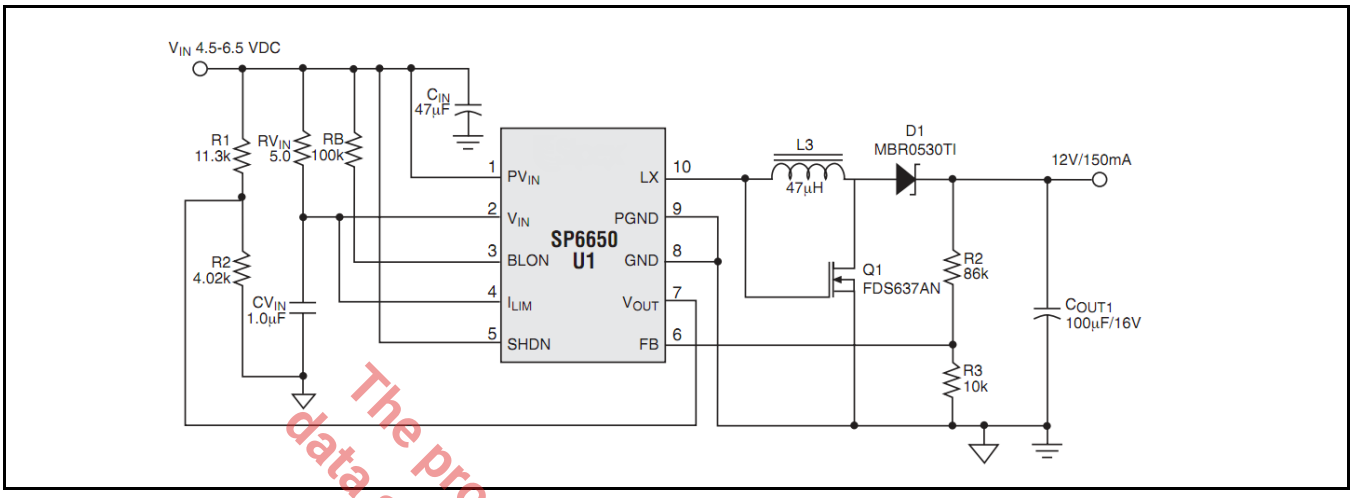


Fig.22: Additional Application Circuit: V_{IN} = 5.0V, V_{OUT} = 12V, and Max I_{LOAD} = 150mA.

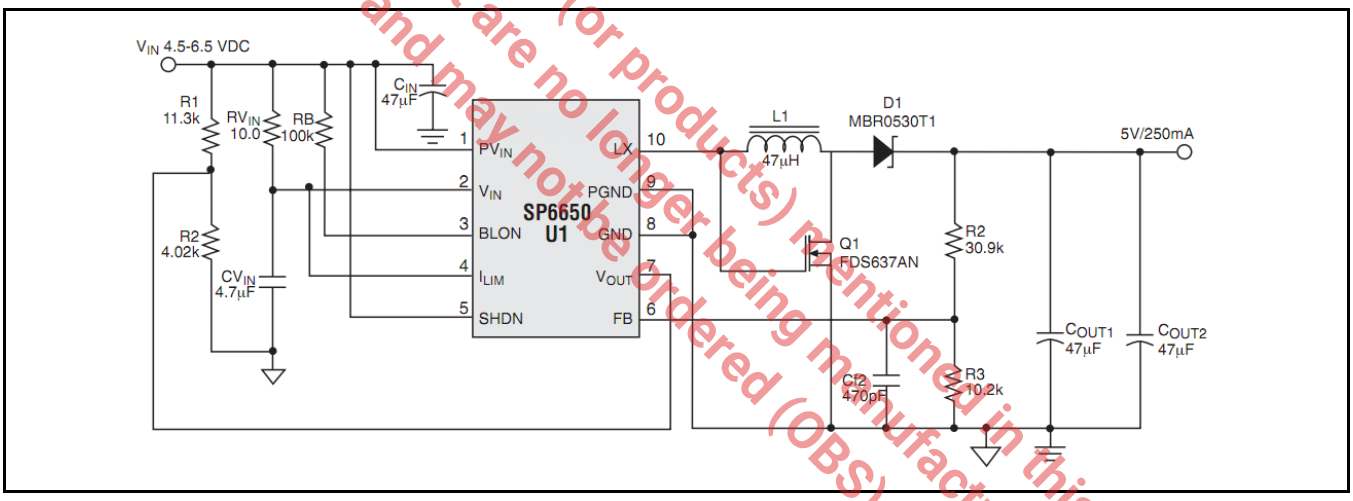


Fig. 23: Additional Application Circuit: V_{IN}= 5.0V, V_{OUT} = 5.0V, I_{LOAD} = 250mA.

LAYOUT CONSIDERATIONS

Proper layout is a very important part of the onboard power supply, affecting normal functionality of the DC-DC converter itself and EMI. Because of the high frequency switching of the converter, the traces that couple an electric field can conduct currents under the AC voltages across the parasitic capacitance. Magnetic field coupling traces can induce currents like transformers.

To avoid an excessive interference between the converter and the other active components on the board, some rules should be followed.

Avoid injecting noise into the sensitive part of the circuit via the GND Plane. Input and output capacitors conduct the current through the GND Plane and high frequency components of the current can degrade the sensitive circuitry. Separate the power and signal grounds and connect them at one point to minimize the noise injected from the power ground to the signal ground. "Star" connection of the ground traces is shown on Figure 24, where GND is the minus pole of the output capacitor.

Power loops on the input and output of the converter should be laid out with the shortest and widest traces possible. The longer and

narrower the trace, the higher the resistance and inductance it will have. The AC current in long traces radiates EMI noise affecting the sensitive circuits. The length of traces in series with the capacitors increases its ESR and ESL and reducing their effectiveness at high frequencies. Therefore put the input capacitor as close to the appropriate pins of the converter as possible and output capacitor close to the inductor.

The external voltage feedback network should be placed very close to the FB pin as well as bypass capacitor C4. Any noise traces like the Lx pin should be kept away from the voltage feedback network and separated from it by using power ground copper to minimize EMI.

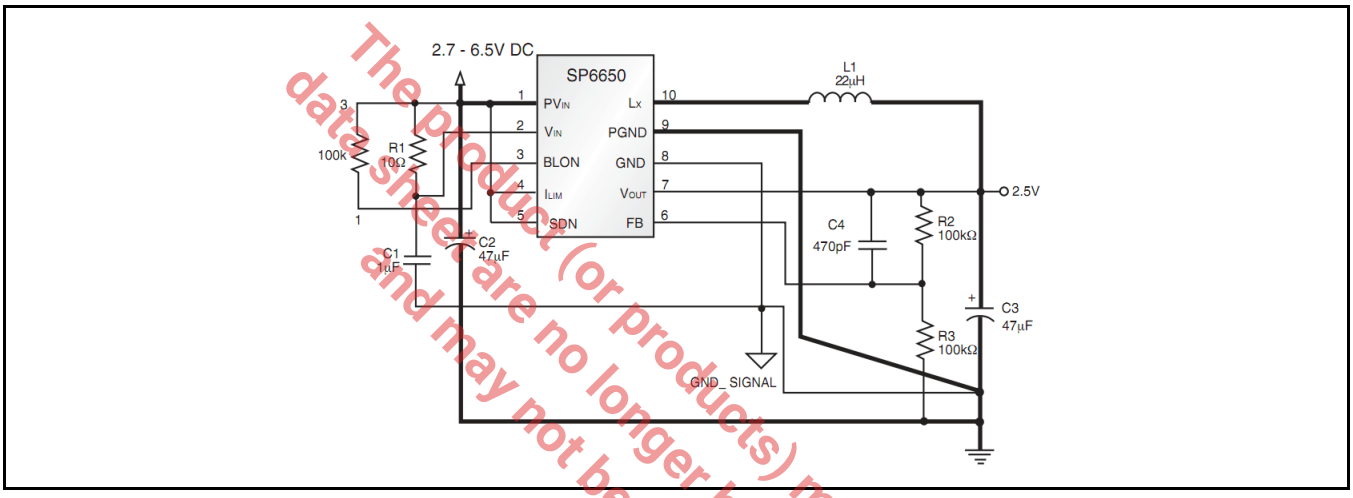
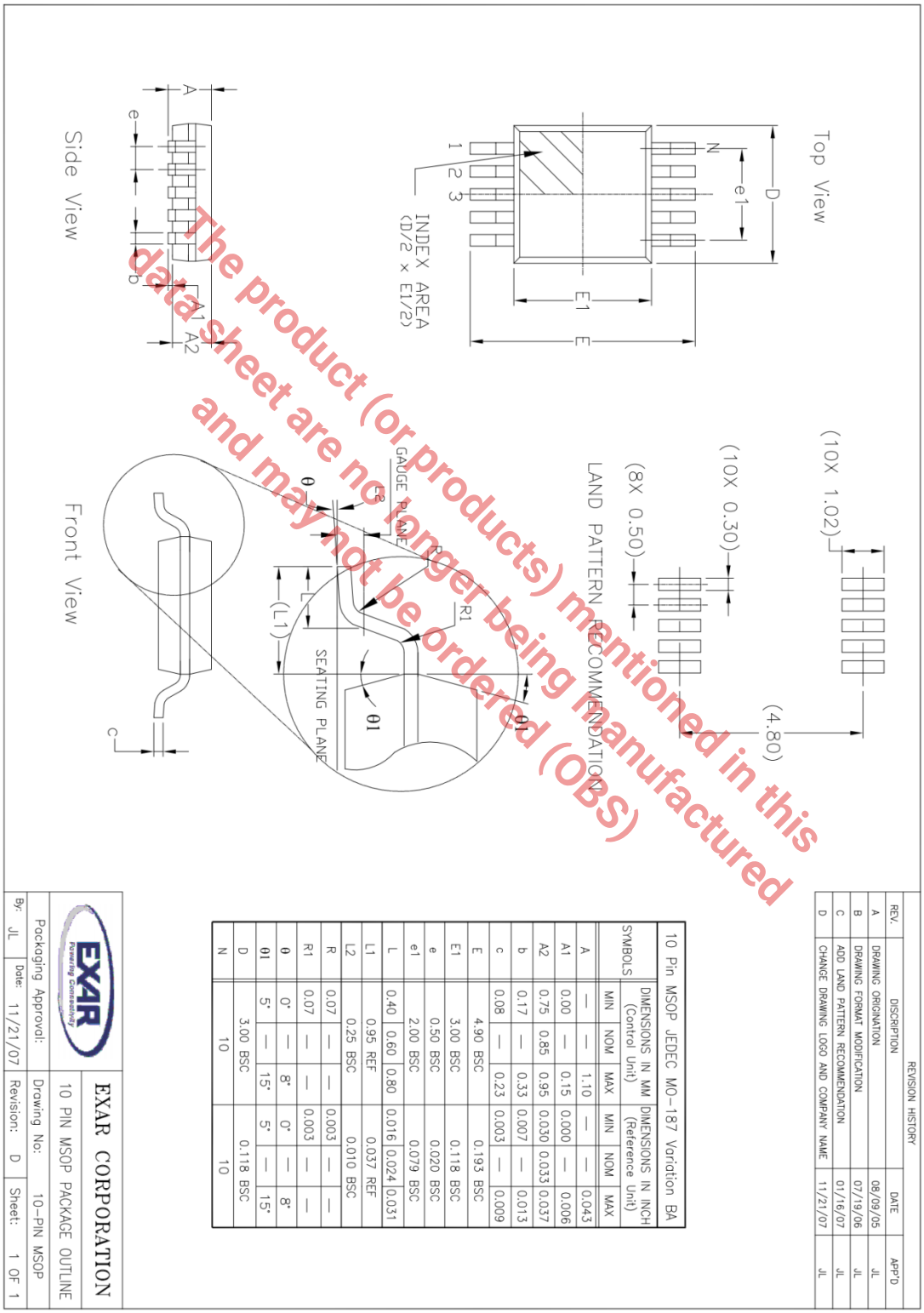


Fig. 24: Application circuit with highlighted power traces.

PACKAGE SPECIFICATION

10 PIN MSOP



REVISION HISTORY

REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/09/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL
C	ADD LAND PATTERN RECOMMENDATION	01/16/07	JL
D	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

10 Pin MSOP JEDEC MO-187 Variation BA

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.00	—	0.15	0.000	—	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.17	—	0.33	0.007	—	0.013
c	0.08	—	0.23	0.003	—	0.009
E	4.90 BSC			0.193 BSC		
E1	3.00 BSC			0.118 BSC		
e	0.50 BSC			0.020 BSC		
e1	2.00 BSC			0.079 BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
L1	0.95 REF			0.037 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
D	3.00 BSC			0.118 BSC		
N	10			10		

EXAR CORPORATION

10 PIN MSOP PACKAGE OUTLINE

Packaging Approval: | Drawing No: 10-PIN MSOP | Revision: D | Sheet: 1 OF 1

By: JL | Date: 11/21/07

REVISION HISTORY

Revision	Date	Description
2.0.0	08/01/2012	Reformat of datasheet

FOR FURTHER ASSISTANCE

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