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# Ethernet Network Connection

# Single Port 2.5G Ethernet PHY

Ethernet Network Connection GPY212 (GPY212B1VC, GPY212C0VC)

# Data Sheet

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Revision 1.3, 2021-04-27
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**Revision History**

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| **Current:** | **Revision 1.3, 2021-04-27** |
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| Page | Major changes since previous revision |
|---|---|
| All | This document covers GPY212C0VC and GPY212B1VC. GPY212C0VC is an enhanced performance version of GPY212B1VC with reduced power consumption. |
| **1** | Added GPY212C0VC on Front Page. |
| **26** | **Figure 4**, **MDIO Access Timing**: Added MDIO access timing. |
| **37** | **Section 3.4.7.1 Enabling SGMII Auto-negotiation Mode**: Corrected SGMII auto-negotiation default setting. |
| **40** | **Section 3.5.3 LED Brightness Control**: Updated LED Brightness Control section. |
| **82** | Removed TPG Control register. |
| **124** | **Table 23**, **Registers Overview**: Updated ANEG_MGBT_AN_CTRL Reset value. |
| **137** | **ANEG_MGBT_AN_CTRL**, **MULTI GBT AN Control Register (Register 7.32)**: Updated Reset value. |
| **144** | **VSPEC1_LED0**, **PULSE**: Updated Pulsing Configuration. |
| **145** | **VSPEC1_LED1**, **PULSE**: Updated Pulsing Configuration. |
| **146** | **VSPEC1_LED2**, **PULSE**: Updated Pulsing Configuration. |
| **148** | **VSPEC1_LED3**, **PULSE**: Updated Pulsing Configuration. |
| **154** | Updated conversion formula in temperature code. |
| **165** | **Table 28**, **Typical Power Consumption (GPY212C0VC)**: Added typical power consumption for GPY212C0VC. |
| **166** | **Table 30**, **Maximum Power Consumption (GPY212C0VC)**: Added maximum power consumption for GPY212C0VC. |
| **187** | **Figure 31**, **Example of Chip Marking**: Updated Chip Marking pattern. |
| **187** | **Table 53**, **Chip Marking Pattern**: Updated Chip Marking Pattern information. |
| **187** | **Table 54**, **Product Naming (GPY212C0VC)**: Added Product Naming for GPY212C0VC, including engineering sample information. |

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# 1 Product Overview

The Ethernet Network Connection GPY212 is a low power Ethernet PHY transceiver integrated circuit. It offers a cost-optimized solution that is well-suited for routers, switches, and home gateways. It performs the data transmission on an Ethernet twisted pair copper cable of category Cat5e or higher. GPY212 supports the following data rates: 2500, 1000, 100, and 10 Mbit/s.

In terms of the Open System Interconnection (OSI) model, the GPY212 implements a layer 1 physical media access device. It can be connected to another chip implementing a layer 2 MAC via a serial SGMII data interface.

On the Ethernet twisted pair interface, the GPY212 is compliant with the following standards from IEEE 802.3 referenced in **[2]** and **[3]**: 2.5GBASE-T (IEEE 802.3bz, NBASE-T), 1000BASE-T (IEEE802.3 Clause 40), 100BASE-TX (IEEE 802.3 Clause 25) and 10BASE-Te (IEEE 802.3 Clause 14). This interface supports the Energy-Efficient Ethernet feature to reduce idle mode power consumption. Power saving at the system level is also possible with the Wake-on-LAN feature. A low-EMI line driver with integrated termination facilitates the PCB design.

On the SGMII interface, connecting to another chip implementing a MAC layer, the GPY212 supports the following standards: IEEE802.3 Clause 36 and 27 **[2]**, and Cisco SGMII **[4]**. This interface also operates at data rates: 2500, 1000, 100, and 10 Mbit/s.

The GPY212 supports the Precision Time Protocol (PTP).

The GPY212 integrates a MAC security engine (MACsec) that can be used to perform wire-speed point to point encryption when the MAC SoC does not support the feature in its MAC layer.

The GPY212 supports a standard MDIO management interface as defined in IEEE 802.3 Clause 22 and Clause 45 **[2]**, **[3]**. The MDIO serial interface can operate with a clock running up to 25 MHz. It allows a management entity (the external chip implementing the MAC) to access standard MDIO / MMD registers to control the GPY212 behavior, or to read the link status. In addition, two vendor specific register banks (VSPEC1 and VSPEC2) allow GPY212 specific configuration of LED, SGMII, and Wake-on-LAN features. The MDIO and MMD registers are documented in **Chapter 5**. The GPY212 is also configurable via pin strapping.

The GPY212 can drive up to four LEDs. Each LED is independently programmable to indicate the link speed, and traffic activities. Several indication schemes can be selected.

A DC/DC converter is integrated within the GPY212. A single external power supply of 3.3 V is sufficient to power the chip, with the internal DC/DC converter generating 1.0 V to supply the low voltage domains. External supply of both 3.3 V and 1.0 V is also an option.

The GPY212 uses a single row package (type PG-VQFN-56, size 7 mm x 7 mm).

## 1.1 Features

This chapter provides an overview of the features supported by the GPY212:

**Communication Interfaces**

- The multiple speed, single-port Ethernet PHY interface to the twisted pair cable supports:
  - Ethernet modes and standards: 2.5GBASE-T (IEEE 802.3bz, NBASE-T), 1000BASE-T (IEEE 802.3), 100BASE-TX (IEEE 802.3) and 10BASE-Te (IEEE 802.3)
  - Ethernet twisted pair copper cable of category CAT5 or higher
  - Low EMI voltage mode line driver with integrated termination resistors
  - Transformerless Ethernet for backplane applications
  - Auto-negotiation (ANEG) with extended next page support
  - Auto-MDIX and polarity correction
  - Auto-downspeed (ADS)
  - Energy-Efficient Ethernet (EEE) and power down mode
  - Wake-on-LAN (WoL)
  - Power-over-Ethernet (POE)
  - Precise time stamping, implementing standard IEEE 1588v2
  - SPI interface supports Secure Field Firmware Upgrade (FFU) of the flash memory

- The SGMII SerDes interface supports:
  - 1000BASE-X IEEE 802.3 Clause 36 and 37 [2]
  - Cisco* Serial-GMII Specification [4] operating at 1.25 Gbaud/s
  - Extension of 1000BASE-X and Cisco Serial-GMII to achieve 3.125 Gbaud/s by overclocking the SerDes to support the 2.5 Gbit/s data rate
  - Clock and Data Recovery (CDR)
  - SGMII power saving when a Low Power Indication (LPI) is active

- The management interface supports the communication between the Station Management (acronym “STA” per IEEE 802.3) and the GPY212 using:
  - An MDIO slave interface that provides access to the standard registers in the MMD as described in IEEE 802.3 Clause 22 and Clause 45 [2] and listed in **Chapter 5**
  - An MDIO interface clock of up to 25 MHz
  - 3 MDIO message frame types as described in IEEE 802.3: Clause 22, Clause 22 Extended, Clause 45 [2]

- The LED interface supports:
  - Up to 4 LEDs
  - Single and dual color LEDs
  - Connection of LED to ground or 3.3 V
  - Several LED indication schemes (link/activity, link speed)
  - Configuration of LED indication via MDIO registers
  - Control of LED brightness via software driver API
  - Alternative configuration of LED pins as GPIO for custom indication

- Supports two external interrupts EXINT0 and EXINT1:
  - Configurable as input from, or output to an external controller

**Clocking, Timing and Time Stamping Features**

- 25 MHz crystal operation
- Supports precise time stamping (PTP) according to standard IEEE 1588v2
- Supports two general purpose clock pins GPC1 and GPC2 shared with GPIO for several usage options, configurable by GPY API:
  – to input or output the precise time stamping signals (PTP)
  – to output the pulse per second signal (PPS)

**Test Features**

- JTAG boundary scan
- Cable diagnostics: cable open/short detection and cable length estimation
- UART

**MACsec Security Feature**

- MACsec Engine (compliant with IEEE 802.1AE, IEEE 802.1AEbn and IEEE 802.1AEbw MAC security standards)
- MACsec Engine is controlled by an API executed on the associated MAC SoC through the slave MDIO interface (GPYAPI)

**Power Supply**

- Single 3.3 V power supply, when using the integrated DC/DC converter to generate the 1.0 V power supply rail
- If the internal integrated DC/DC converter is not used, an additional 1.0 V supply must be provided externally
- Ultra low power mode to reduce the energy consumption down to 10 mW when the Ethernet cable is unplugged, with automatic wake-up upon energy detection from cable

## 1.2 Block Diagram

Figure 2 shows the block diagram of the GPY212. The main interfaces are:

- Data interface to a MAC processor, using SGMII
- Slave control interface driven by a MAC processor, using MDIO slave
- Interrupt signal MDINT allowing the GPY212 to notify the MAC processor about a change of status
- LED control
- Twisted pair interface

The GPY212 product variant supports the MACsec block, which performs encryption and decryption of the MAC frames as indicated in Figure 2.

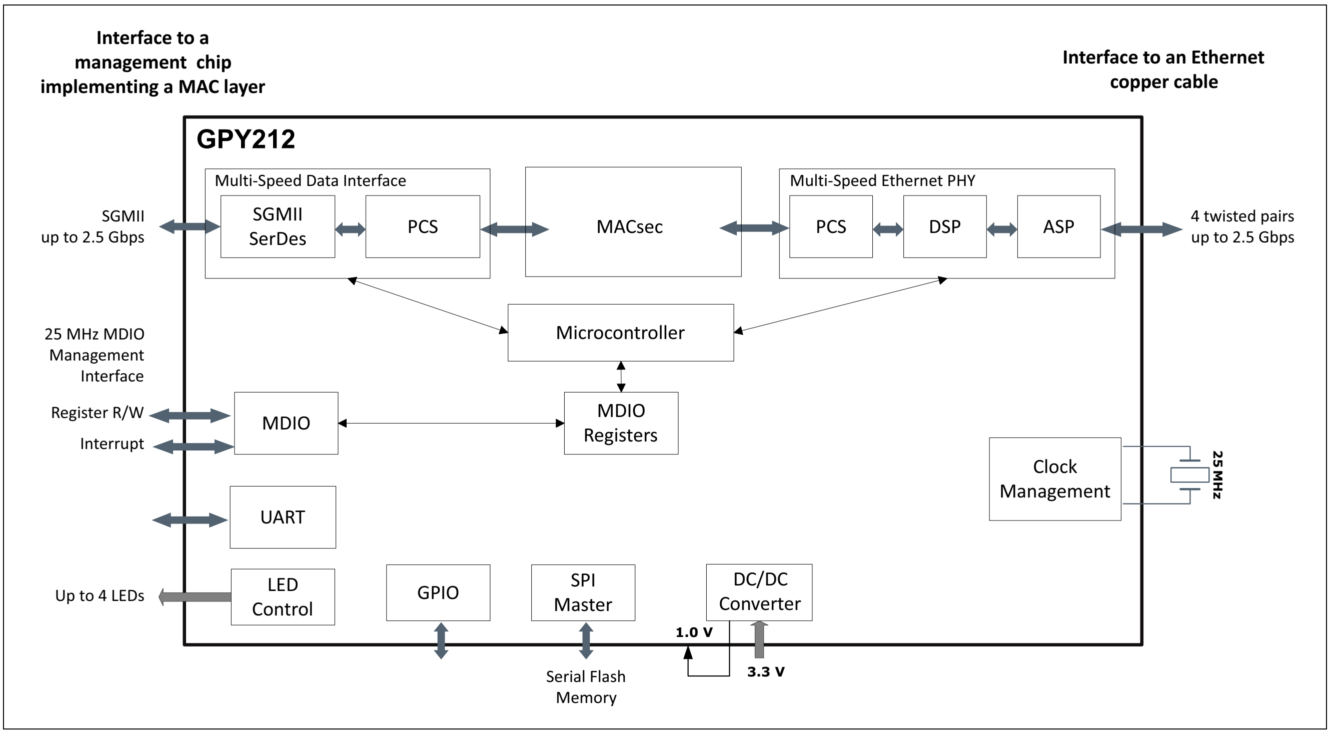



**Figure 1 Ethernet Network Connection GPY212 Block Diagram**

# 2 External Signals

This chapter describes the signal mapping to the package.

## 2.1 Overview

Figure 2 provides an overview of the external interfaces of the GPY212.

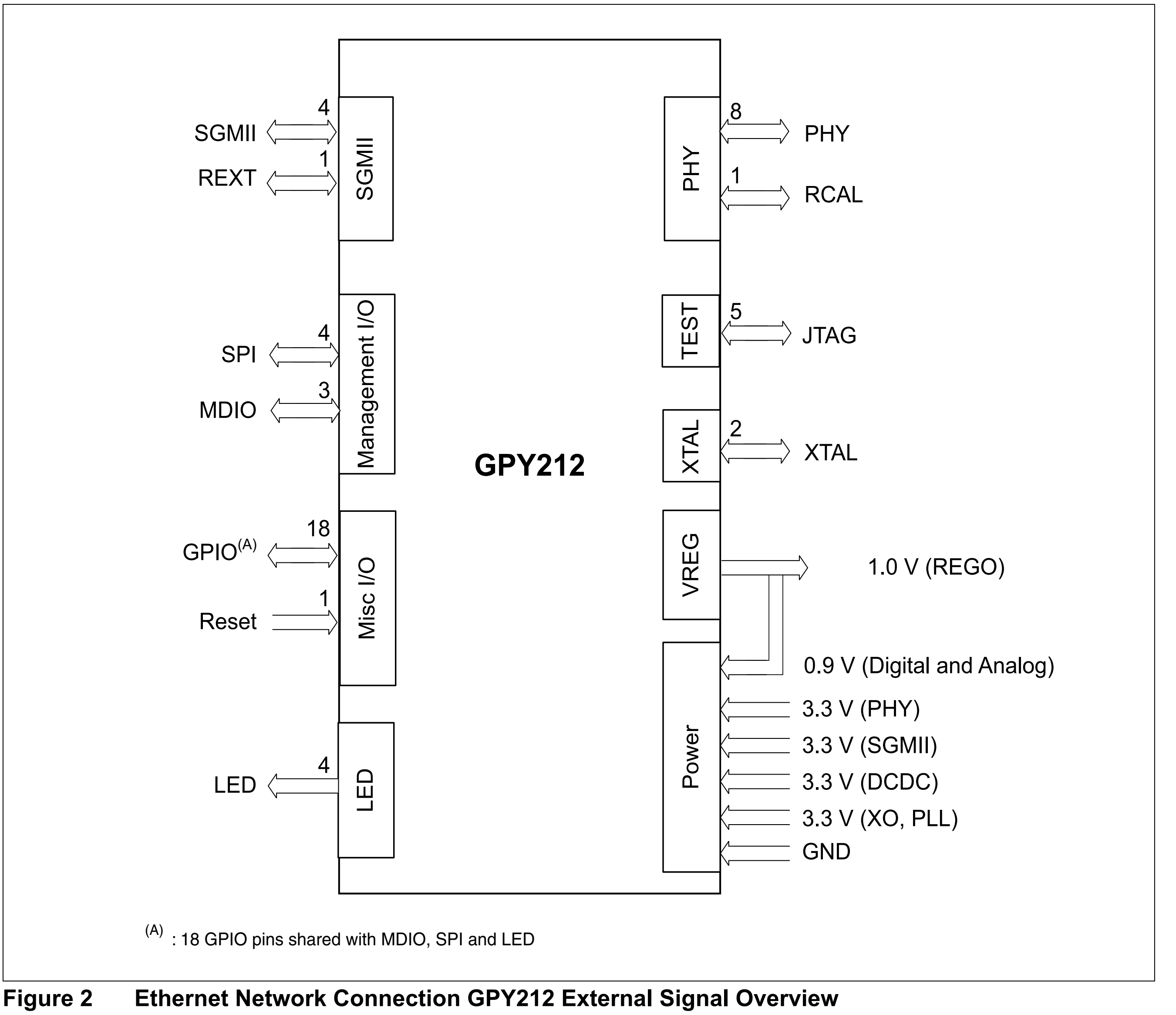



**Figure 2 Ethernet Network Connection GPY212 External Signal Overview**

## 2.2 External Signal Description

This chapter provides the pin diagram, abbreviations for pin types and buffer types, as well as tables describing the input and output signals.

### 2.2.1 Pin Diagram

The pin layout of the package is shown in **Figure 3**.

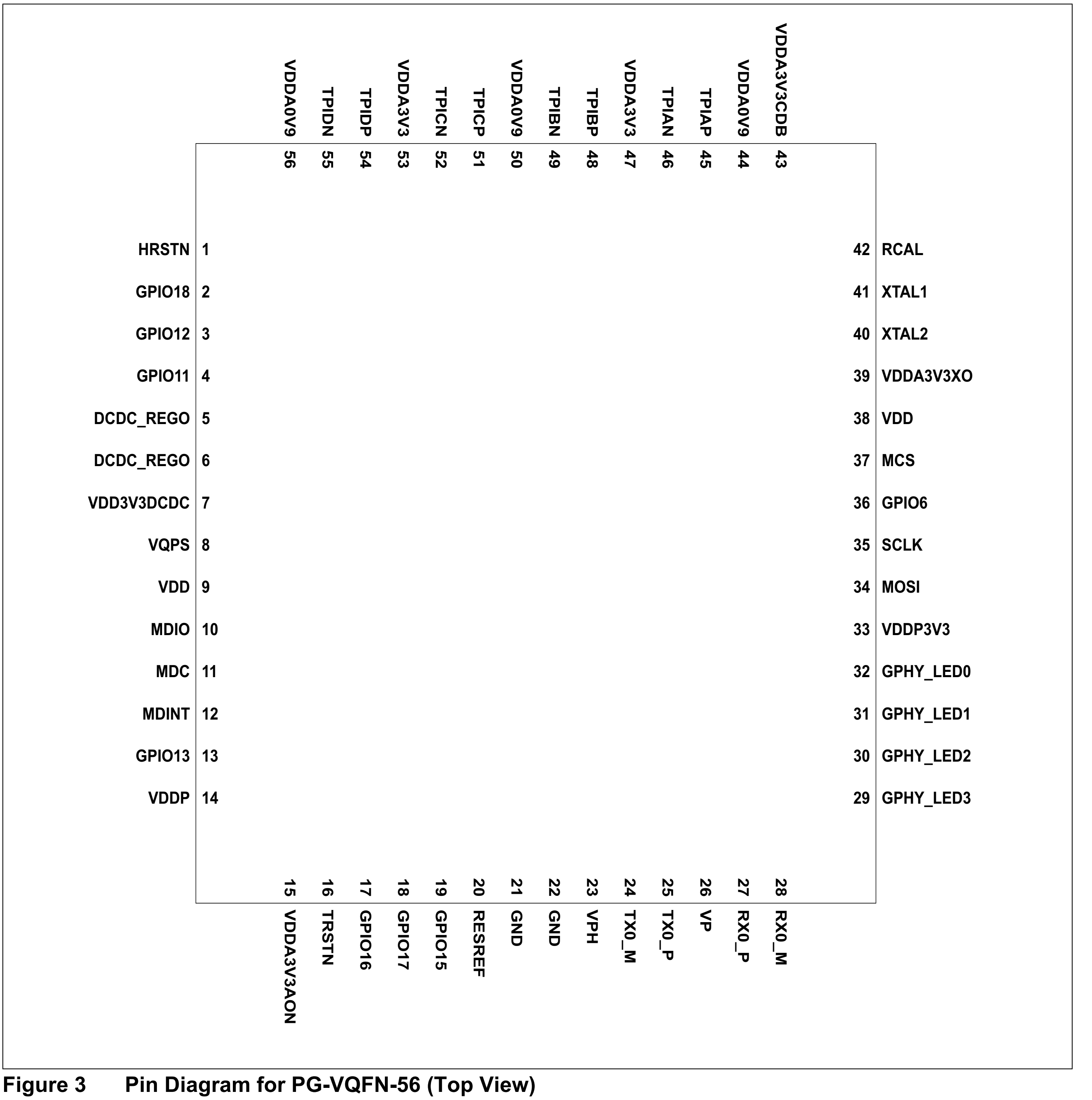



**Figure 3 Pin Diagram for PG-VQFN-56 (Top View)**

### 2.2.2 Abbreviations

Abbreviations that are used in the signal tables are summarized in **Table 1** and **Table 2**.

**Table 1 Abbreviations for Pin Type**

| Abbreviations | Description |
|---|---|
| I | Input only, digital levels |
| O | Output only, digital levels |
| I/O | Bidirectional input/output signal, digital levels |
| Prg | Bidirectional pad, programmable to operate either as input or output, digital levels |
| AI | Input only, analog levels |
| AO | Output only, analog levels |
| AI/O | Bidirectional, analog levels |
| PWR | Power |
| GND | Ground |

**Table 2 Abbreviations for Buffer Type**

| Abbreviations | Description |
|---|---|
| A | Analog characteristics, see the AC/DC specification for more detail |
| GND | Ground |
| Prg | Programmable with an alternate function |

### 2.2.3 Input/Output Signals

A detailed description of all the pins is given in **Table 3** to **Table 8**.

In **Table 5** to **Table 8**, the signal names highlighted in bold are the same as the pin name. The signal names that are not in bold indicate alternate functions.

#### 2.2.3.1 Ethernet Media Interface

**Table 3 Ethernet Media Interface Signals**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **Ethernet Port Ethernet Media Interface** | | | | |
| 45 | **TPIAP** | AI/AO | A | **Twisted Pair Transmit/Receive Positive/Negative** |
| 46 | **TPIAN** | AI/AO | A | |
| 48 | **TPIBP** | AI/AO | A | |
| 49 | **TPIBN** | AI/AO | A | |
| 51 | **TPICP** | AI/AO | A | |
| 52 | **TPICN** | AI/AO | A | |
| 54 | **TPIDP** | AI/AO | A | |
| 55 | **TPIDN** | AI/AO | A | |
| **Ethernet Port Calibration** | | | | |
| 42 | **RCAL** | AI/AO | A | **Calibration of GPHY Ethernet Port**<br>Using a high precision resistor. |

#### 2.2.3.2 SGMII Interface

**Table 4 SGMII Interface Signals**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 28 | **RX0_M** | AI | A | **Differential SGMII Data Input Pair**<br>These are the negative and positive signals respectively of the differential input pair of the SGMII SerDes interface. Due to the integrated CDR, no external transmission of source-synchronous clock is required for SGMII. These pins must be AC coupled. |
| 27 | **RX0_P** | AI | A | |
| 25 | **TX0_P** | AO | A | **Differential SGMII Data Output Pair**<br>These are the negative and positive signals respectively of the differential output pair of the SGMII SerDes interface. |
| 24 | **TX0_M** | AO | A | |
| 20 | **RESREF** | AI/O | A | **Pad to Connect External Tuning Resistor** |
| 21 | **GND** | AI | GND | **Connect to Ground** |
| 22 | **GND** | AI | GND | **Connect to Ground** |

### 2.2.3.3 LED/JTAG/GPIO Interface

The LED interface allows external LEDs to be connected to indicate the status of the Ethernet PHY interfaces. Single and dual color LEDs are supported.

**Table 5 LED Interface Signals**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **LED Signals** | | | | |
| 32 | **GPHY_LED0** | O | | **GPHY LED0**<br>LED control output, freely configurable, drives single color or dual color LEDs. |
| 31 | **GPHY_LED1** | O | | **GPHY LED1**<br>LED control output, freely configurable, drives single color or dual color LEDs. |
| 30 | **GPHY_LED2** | O | | **GPHY LED2**<br>LED control output, freely configurable, drives single color or dual color LEDs. |
| 29 | **GPHY_LED3** | I/O | Prg | **GPHY LED3**<br>LED control output, freely configurable, drives single color or dual color LEDs.<br>This pin is also used for the brightness control switch input. |
| | TCK | I | PU | **JTAG Test Clock**<br>The signals TDI, TDO and TMS are synchronous subject to this JTAG test clock. |
| 16 | **TRSTN** | I | PD | **JTAG Test Reset**<br>The signal TRSTN must be pulled-down to ground. The JTAG is only used in production for boundary scan. |
| 19 | **GPIO15** | Prg | Prg | **General Purpose IO 15**<br>Configurable as input or output.<br>The output characteristic can be selected to be open drain or push-pull. |
| | TDI | I | PU | **JTAG Serial Test Data Input** |
| 17 | **GPIO16** | Prg | Prg | **General Purpose IO 16**<br>Configurable as input or output.<br>The output characteristic can be selected to be open drain or push-pull. |
| | TMS | I | PU | **JTAG Test Mode Select** |
| 18 | **GPIO17** | Prg | Prg | **General Purpose IO 17**<br>Configurable as input or output.<br>The output characteristic can be selected to be open drain or push-pull. |
| | TDO | O | | **JTAG Serial Test Data Output**<br>JTAG test data output. |

#### 2.2.3.4 Management Interfaces

Two types of serial management interface are provided:

- SPI master interface
- MDIO slave interface

**Table 6 Management Interface Signals**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **MDIO Slave Interface** | | | | |
| 4 | **GPIO11** | Prg | Prg | **General Purpose IO 11**<br>Configurable as input or output.<br>The output characteristic can be selected to be open drain or push-pull. |
| | GPC1 | Prg | | **General Purpose Clock 1**<br>General purpose clock. Either input or output mode can be selected. |
| 11 | **MDC** | I | Prg | **MDIO Slave Clock**<br>The external controller host (also called “STA” in IEEE standard) acts as clock master and provides the serial clock of up to 25 MHz on this input. |
| 10 | **MDIO** | I/O | Prg | **MDIO Slave Data Input/Output**<br>The external controller host (also called “STA” in IEEE standard) uses this signal to address internal registers and to transfer data to and from the internal registers. |
| **SPI Master Interface** | | | | |
| 36 | **GPIO6** | Prg | Prg | **General Purpose IO 6**<br>Configurable as input or output.<br>The output characteristic can be selected to be open drain or push-pull. |
| | MISO | I | | **SPI Data Input**<br>SPI interface data input. |
| 34 | **MOSI** | O | Prg | **SPI Data Output**<br>SPI interface data output. |
| 35 | **SCLK** | O | Prg | **SPI Clock**<br>SPI interface clock. |
| 37 | **MCS** | O | Prg | **SPI Chip Select**<br>SPI interface chip select. Active low signal. |

#### 2.2.3.5 Miscellaneous Signals

**Table 7 Miscellaneous Signals**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **Reset and Clocking** | | | | |
| 41 | **XTAL1** | AI | A | **Crystal: Oscillator Input**<br>A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must also tie both pins to GND. |
| | CLK | I | | **Clock: Clock Input**<br>The clock must have a frequency accuracy of ±50 ppm. |
| 40 | **XTAL2** | AO | A | **Crystal: Oscillator Output**<br>A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must also tie both pins to GND. |
| 13 | **GPIO13** | Prg | Prg | **General Purpose IO 13**<br>Configurable as input or output.<br>The output characteristic can be selected to be open drain or push-pull. |
| | EXINT0 | | | **External Interrupt 0**<br>This is an interrupt signal to or from an external host.<br>Configurable as input or output.<br>This is not used in the standard application. |
| 12 | GPIO14 | Prg | Prg | **General Purpose IO 14**<br>Configurable as input or output. |
| | EXINT1 | | | **External Interrupt 1**<br>This is an interrupt signal to or from an external host.<br>Configurable as input or output.<br>This is not used in the standard application. |
| | **MDINT** | O | | **MDIO Interrupt**<br>The MDINT signal is used to send an interrupt to an external MAC SoC acting as station manager (STA). The STA can program its sensitivity to specific events using the PHY_IMASK register. The MDINT event is then raised when the event occurs using the polarity programmed by pin strap. The STA can read which type of event occurred in the PHY_ISTAT register. Upon read of PHY_ISTAT by the STA, the MDINT is deasserted by the GPY212. Refer to **Figure 9** for further details. |
| 3 | **GPIO12** | Prg | Prg | **General Purpose IO 12**<br>Configurable as input or output.<br>The output characteristic can be selected to be open drain or push-pull. |
| | GPC2 | Prg | | **General Purpose Clock 2**<br>General purpose clock. Either input or output mode can be selected. |

**Table 7 Miscellaneous Signals** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 2 | **GPIO18** | Prg | Prg | **General Purpose IO 18**<br>Configurable as input or output.<br>The output characteristic can be selected to be open drain or push-pull. |
| 1 | **HRSTN** | I | PU | **Hardware Reset**<br>Asynchronous active low device reset. If the internal Power-on-Reset (POR) circuit is used to trigger the device power up, this signal can be left unconnected. |

### 2.2.3.6 Power Supply

This section specifies the power supply pins. They are categorized in 2 supply groups $V_{HIGH}$ (3.3 V) and $V_{LOW}$ (1.0 V). The $V_{LOW}$ domain can either be supplied externally, or self-generated by the internal DC/DC SVR converter, which converts the VDD3V3DCDC 3.3 V supply into DCDC_REGO output. In the external supply configuration, the DCDC_REGO output pins are non connected (NC). In the internal DC/DC SVR converter configuration, the DCDC_REGO output pins are connected back to the $V_{LOW}$ supply inputs.

**Table 8 Power Supply Pins**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 47, 53 | **VDDA3V3** | PWR | | **High Voltage Domain Supply $V_{HIGH}$**<br>These are the input power pins for the analog front end in the high voltage domain. They have to be supplied with a nominal voltage of $V_{DDA3V3}$ = 3.3 V. |
| 44, 50, 56 | **VDDA0V9** | PWR | | **Low Voltage Domain Supply $V_{LOW}$**<br>These are the input power supply pins for the low voltage domain. They supply mixed signal blocks in the analog front end and the clock distribution block of the Gigabit Ethernet PHY. These pins have to be supplied with a nominal voltage of $V_{DDA0V9}$ = 1.0 V. When the internal DC/DC SVR converter is used, they have to be connected to the output of the converter DCDC_REGO. |
| 39 | **VDDA3V3XO** | PWR | | **XO Pad Voltage Domain Supply $V_{HIGH}$**<br>This is the input power supply pin for the internal PLL and the internal crystal oscillator (XO). This pin has to be supplied with a nominal voltage of $V_{DDA3V3}$ = 3.3 V. |
| 43 | **VDDA3V3CDB** | PWR | | **CDB High Voltage Domain Supply $V_{HIGH}$**<br>This is the input power supply pin for the internal clock distribution block (CDB). This pin has to be supplied with a nominal voltage of $V_{DDA3V3}$ = 3.3 V. |
| 15 | **VDDA3V3AON** | PWR | | **AON High Voltage Domain Supply $V_{HIGH}$**<br>This is the input power supply pin for the Always On Domain (AON). This pin has to be supplied with a nominal voltage of $V_{DDA3V3}$ = 3.3 V. |

**Table 8 Power Supply Pins**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 26 | **VP** | PWR | | **SGMII Low Voltage Domain Supply $V_{LOW}$**<br>This is the pin for the low voltage domain of the SGMII interface. It supplies mixed signal blocks in the SGMII interface. This pin has to be supplied with a nominal voltage of $V_P$ = 1.0 V. When the internal DC/DC SVR converter is used, these pins have to be connected to the output of the converter DCDC_REGO. |
| 23 | **VPH** | PWR | | **SGMII High Voltage Domain Supply $V_{HIGH}$**<br>This is the pin for the high voltage domain of the SGMII interface. It supplies mixed signal blocks in the PHY of the SGMII interface.<br>This pin has to be supplied with a nominal voltage of $V_{PH}$ = 3.3 V. |
| 14 | **VDDP** | PWR | | **Configurable MDIO Pad Voltage Domain Supply**<br>This is the group of supply pins for the MDIO pins group (pin 10 to 13).<br>This group can be configured in 1.8 V or 3.3 V operation, depending on the option selected by pin strap on pin 19 (PS_MDIO_VOLTAGE).<br>When PS_MDIO_VOLTAGE is LOW, this pin has to be supplied with a nominal voltage of $V_{DDP}$ = 1.8 V.<br>When PS_MDIO_VOLTAGE is HIGH, this pin has to be supplied with a nominal voltage of $V_{DDP}$ = 3.3 V. An internal Pull up on pin 19 drives the pin 19 configuration to HIGH unless the pin is explicitly connected to ground (LOW). |
| 33 | **VDDP3V3** | PWR | | **Pad Voltage Domain Supply $V_{HIGH}$**<br>This is the group of supply pins for the pad supply of GPIO pins (except the MDIO group of pin which is supplied by VDDP)<br>This pin has to be supplied with a nominal voltage of $V_{DDP3V3}$ = 3.3 V. |
| 9, 38 | **VDD** | PWR | | **Core Voltage Domain Supply $V_{LOW}$**<br>This is the group of supply pins for the core digital voltage domain.<br>This pin has to be supplied with a nominal voltage of $V_{DD}$ = 1.0 V.<br>When the internal DC/DC SVR converter is used, these pins have to be connected to the output of the converter DCDC_REGO. |
| 8 | **VQPS** | PWR | | **Ground**<br>This pin is not used in application mode. It must be tied to GND. |
| 7 | **VDD3V3DCDC** | PWR | | **Internal DC/DC SVR Converter Power Supply $V_{HIGH}$**<br>This is the supply pin for the integrated DC/DC converter. This pin has to be supplied with a nominal voltage of $V_{DDA3V3DCDC}$ = 3.3 V.<br>This pin must be connected in all supply configuration including the external $V_{LOW}$ supply option. |
| 5, 6 | **DCDC_REGO** | PWR | | **Internal DC/DC SVR Converter Output**<br>These are the 2 pins supplying the $V_{LOW}$ domain when the internal DC/DC SVR converter is used. In internal SVR mode this pin must be connected back to the $V_{LOW}$ domain to self supply the chip. The connection circuitry for the internal DCDC SVR $V_{LOW}$ supply option and the external $V_{LOW}$ supply option are described in **Figure 28** and **Figure 29**. |

**Table 9 Device Ground**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| EPAD[1)] | VSS | GND | | General Device Ground |

1) The EPAD is the exposed pad on the bottom of the package. This pad must be properly connected to the ground plane of the PCB.

# 3 Functional Description

## 3.1 Power Supply, Clock and Reset

This chapter provides the information required to power up the GPY212.

### 3.1.1 Power Supply

Two power supply options are available:

- A single external power supply of 3.3 V – with this option the internal DC/DC SVR converter generates the required 1.0 V supply.
- Two external power supplies of 3.3 V and 1.0 V – with this option, the internal DC/DC SVR converter is not used.

The detailed power supply connection requirements are documented in **Chapter 7.7**. The differentiation between the two power supply options is done by connecting, or not the pins DCDC_REGO as details in **Figure 28** and **Figure 29**.

### 3.1.2 Clock Generation

An external 25 MHz crystal must be connected to the GPY212. The required crystal specification is documented in **Chapter 7.5.8**. An internal PLL circuit generates all the required internal clocks.

### 3.1.3 Reset Generation

The external hardware reset input (HRSTN pin) resets all the hardware modules, except the DC/DC converter:

- Driving the HRSTN pin low causes an asynchronous reset of the GPY212 system.
- Releasing the HRSTN pin high triggers the power-on sequence and boot-up procedure.

The HRSTN pin is internally connected to a weak internal pull-up resistor.

### 3.1.4 Power-On Sequence

The GPY212 powers on when the power is applied as shown in **Figure 19**. The following steps are executed at power on:

- Locking of internal PLL.
- Calibration of internal voltage using a high precision external reference resistor connected to the RCAL pin.
- Reading of pin strap information, as described in **Chapter 3.1.5**.
- Booting of the microprocessor from internal ROM.
- Auto-negotiation on the Ethernet twisted pair interface and SGMII interface using the speed capability of 2.5 Gbit/s, full-duplex.
- Training and link up in accordance with the IEEE 802.3 [2] and SGMII [4] standards.

### 3.1.5 Configuration by Pin Strapping

The GPY212 device can be configured by means of pin strapping on a number of the GPIO pins. The pin strapping configurations are captured during the chip power-on sequence, until the reset initialization is complete.

The pin strap values can be set to logical high or low by connecting the corresponding pin via an external 1 kΩ resistor to either ground or 3.3 V.

The pin strap mapping is described in Table 10 and Table 11.

**Table 10 Pin Names used for Pin Strapping**

| Pin Name | Pin Number | Configuration Item Description |
|---|---|---|
| MCS | 37 | PS_PHY_MADDR(0) |
| SCLK | 35 | PS_PHY_MADDR(1) |
| MOSI | 34 | PS_PHY_MADDR(2) |
| GPIO12 | 3 | PS_PHY_MADDR(3) |
| GPIO18 | 2 | PS_PHY_MADDR(4) |
| MDINT | 12 | PS_MINT_POL |
| GPIO17 | 18 | PS_RJ45_TAP |
| GPIO15 | 19 | PS_MDIO_VOLTAGE |

**Table 11 Pin Strapping Configuration Description**

| Pin Strapping Signals | Description |
|---|---|
| PS_PHY_MADDR(4:0) | **MDIO PHY Address**<br>A high level means a logical 1 and low level means a logical 0. |
| PS_MINT_POL | **MDIO Interrupt (MDINT) Polarity**<br>$0_B$ **HIGH** MDIO Interrupt (MDINT) is active high and configured in push-pull<br>$1_B$ **LOW** MDIO Interrupt (MDINT) is active low and configured in open-drain |
| PS_MDIO_VOLTAGE | **MDIO Voltage**<br>This is to specify whether the maximum voltage level used by the MDIO signals is 3.3 V or 1.8 V (pin 10 to pin 13).<br>$0_B$ **LOW** MDIO signals pads (pin 10 to pin 13) are supplied with 1.8 V. In this configuration the pin14 (VDDP) must be supplied with 1.8 V.<br>$1_B$ **NORMAL** MDIO signals pads (pin 10 to pin 13) are supplied with 3.3 V. In this configuration pin 14 (VDDP) must be supplied with 3.3 V. |
| PS_RJ45_TAP | **RJ45 Pin Reversal**<br>$1_B$ **DOWN** Tap down<br>$0_B$ **UP** Tap up |

An alternative way to configure the GPY212 after the boot process is to use the MDIO interface and write into various control registers, as detailed in Chapter 3.2.

## 3.2 Configuration via MDIO Management Interface

The external controller (Station Management, STA) can be connected to the chip's slave MDIO interface. This allows access to the MDIO and MMD registers standardized in IEEE 802.3. Thus the STA can control chip configuration and retrieve status information. The MDIO transactions can be of any of the 3 types described in IEEE 802.3 Clause 22, Clause 22 Extended, and Clause 45 **[2]**. The list of MDIO registers is given in **Chapter 4**.

**Figure 4** shows the minimum time required for the MDIO to be available for access.

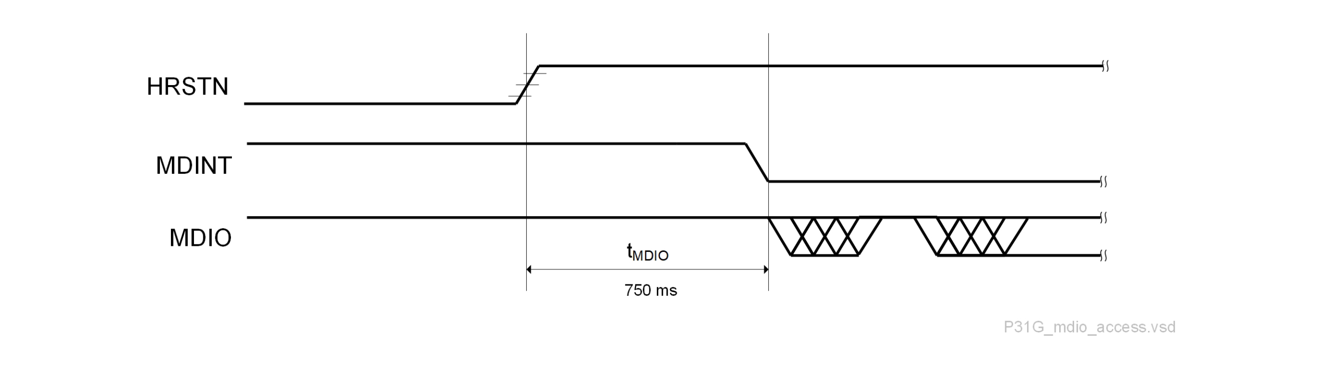



**Figure 4 MDIO Access Timing**

## 3.3 Ethernet PHY Interface

The Ethernet PHY implements the physical layer of the Ethernet standard. It supports digital signal processing (DSP) and analog signal processing (ASP) functions, to transmit data over the twisted pair cable.

### 3.3.1 Twisted Pair Interface

The Twisted Pair Interface (TPI) of the GPY212 is fully compliant with IEEE 802.3. To facilitate low power implementation and reduce PCB costs, the series resistors required to terminate the twisted pair link with a nominal 100 Ω are integrated in the device.

As a consequence, the TPI pins can be connected directly via a transformer to the RJ45 plug. Additional external circuitry is required for common-mode termination and rejection. A schematic of the TPI circuitry taking these components into account is shown in **Figure 5**.

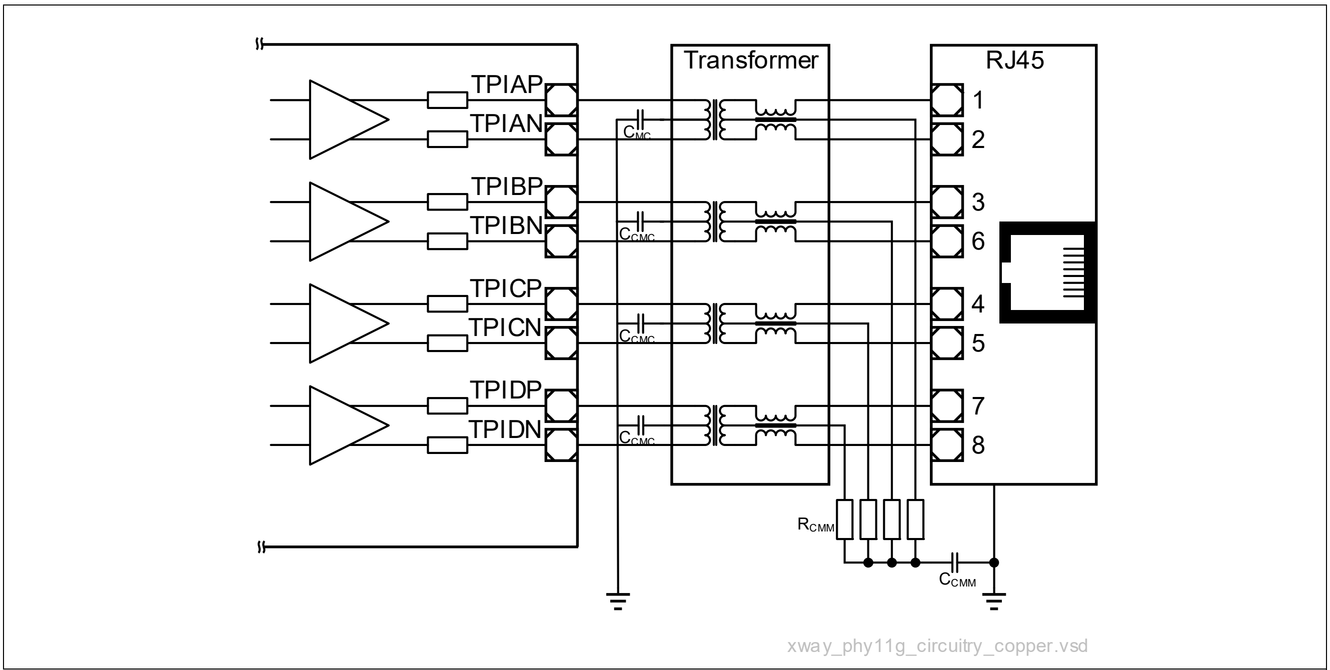



**Figure 5 Twisted-Pair Interface of GPY212 Including Transformer and RJ45 Plug**

### 3.3.2 Transformerless Ethernet (TLE)

Transformerless Ethernet (TLE) is required for backplane applications where the use of a transformer is not necessarily required to fulfill the galvanic decoupling requirements of the isolation specifications. In such applications, removing the transformer reduces both the external bill of material and the space requirements on the PCB.

As the GPY212 incorporates a voltage-mode line driver, the only stringent requirement is to use AC coupling. AC coupling can be achieved using simple SMD type series capacitors. The value of the capacitors is selected so that the high-pass characteristics correspond to an equivalent standard transformer based application (recommended $C_{coupling}$ = 100 nF). **Figure 6** shows the external circuitry for TLE.

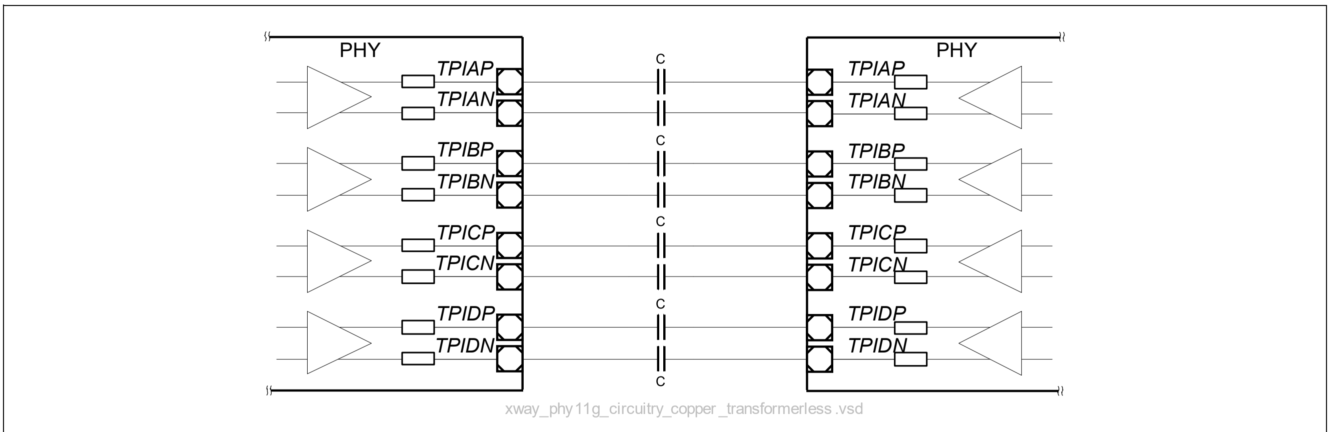



**Figure 6 External Circuitry for the Transformerless Ethernet Application**

### 3.3.3 Auto-negotiation (ANEG)

The GPY212 supports auto-negotiation (ANEG) a part of the startup procedure to exchange capability information with the link partner. ANEG is enabled at GPY212 initialization and its 2.5 Gbit/s speed capability is advertised.

The ANEG procedure is executed according to IEEE 802.3 Clause 28, Clause 40 [2], and IEEE 802.3bz Clause 126 [3].

If the link partner does not support ANEG, the GPY212 extracts the link speed configuration using parallel detection as described in Clause 28.

A STA connected to the MDIO interface can reprogram the GPY212 advertised capability if required. It can also disable ANEG, in which case the system configuration must ensure compatibility between link partners to link up in a compatible mode.

***Attention: STD_CTRL.DPLX takes effect only when the auto-negotiation process is disabled and the GPY TPI is not operating in loop-back mode, that is, bits STD_CTRL.ANEN and STD_CTRL.LB are set to zero. Forced Half Duplex mode (STD_CTRL.DPLX = 0b0) is supported only in 10BT and 100BT speed modes in non-MACsec operations. This field is ignored for higher speeds and MACsec operation.***

### 3.3.4 Auto-downspeed

The auto-downspeed (ADS) feature implements a process to decrease the operating speed of the link when the link quality or cable is insufficient. The feature ensures maximum interoperability even in harsh or inadequate cable infrastructure environments. In particular, ADS is applied during the 2.5GBASE-T/1000BASE-T training phase. The downspeed is necessary when the cable quality or characteristics are inadequate. For example, it is possible to advertise 2.5GBASE-T/1000BASE-T during ANEG when both link partners are connected via a cable that does not support the 4-pair Gigabit Ethernet mode.

The GPY212 detects such configurations to avoid repeating link up failures and clears Gigabit capability in the ANEG advertisement registers. After the resulting link down, the next ANEG procedure no longer advertises 1000BASE-T/2.5GBASE-T. The next link up is done at the next advertised speed below 1000 Mbit/s.

The GPY212 also executes an ADS procedure when the signal quality is not suited to a 1000BASE-T/2.5GBASE-T link up due to increased alien noise or over long cables.

When the GPY212 is configured to advertise no speed capability below 1000 Mbit/s, the ADS feature is disabled automatically.

### 3.3.5 Polarity Reversal Correction

For each of the 4 pairs, the GPY212 automatically detects and corrects any inversion of the signal polarity on the P and N signals. The detection is done during the auto-negotiation phase. The detected polarity is frozen once the link has been established, and remains unchanged until the link is dropped.

The polarity corrections applied are indicated in the following register: PMA_MGBT_POLARITY (register 1.130) and are valid when auto-negotiation is complete.

### 3.3.6 Auto-Crossover Correction

To maximize interoperability, even in inadequate wiring environments, the GPY212 automatically performs cable crossover (MDI-X). The supported pair-mappings detectable and correctable by the device are listed in **Table 12**.

The purpose is to compensate for any non-standard (ANSI TIA/EIA-568-A:1995) cabling, as well as both straight-through and crossover cable connections: the GPY212 automatically detects and corrects any crossed cable configuration (transmit-receive pairing between partners does not match). The auto-crossover function is fully compliant with IEEE 802.3, Clause 40.4.4 [2], in 1000BASE-T and 2500BASE-T mode.

The corrections applied are indicated in the following register: PMA_MGBT_POLARITY (register 1.130) and are valid when auto-negotiation is complete.

**Table 12 Supported Twisted Pair Mappings on a CAT5 or Better Cable**

| Crossover Modes on RJ45[1)] | | RJ45 Pinning | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Mode** | **Description** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** |
| 11 | Straight cable, standard compliant | TPIAP **(A+)** | TPIAN **(A-)** | TPIBP **(B+)** | TPICP **(C+)** | TPICN **(C-)** | TPIBN **(B-)** | TPIDP **(D+)** | TPIDN **(D-)** |
| 00 | Full Gigabit Ethernet MDI-X This is the standard compliant MDI-X with pair A-B swapped and pair C-D swapped | TPIBP **(B+)** | TPIBN **(B-)** | TPIAP **(A+)** | TPIDP **(D+)** | TPIDN **(D-)** | TPIAN **(A-)** | TPICP **(C+)** | TPICN **(C-)** |

1) Pin assignment according to TIA/EIA-568-A/B

### 3.3.7 RJ45 Tap Up or Tap Down Configuration

The RJ45 plug on the system PCB can be soldered with the tap up or down as illustrated in **Figure 7**.

The difference between tap up and tap down is a swap in position between A and D. The pin strap PS_RJ45_TAP allows the system designer to perform this configuration. As a result, a PCB layout does not need to be modified when a RJ45 tap up or down socket needs to be mounted.

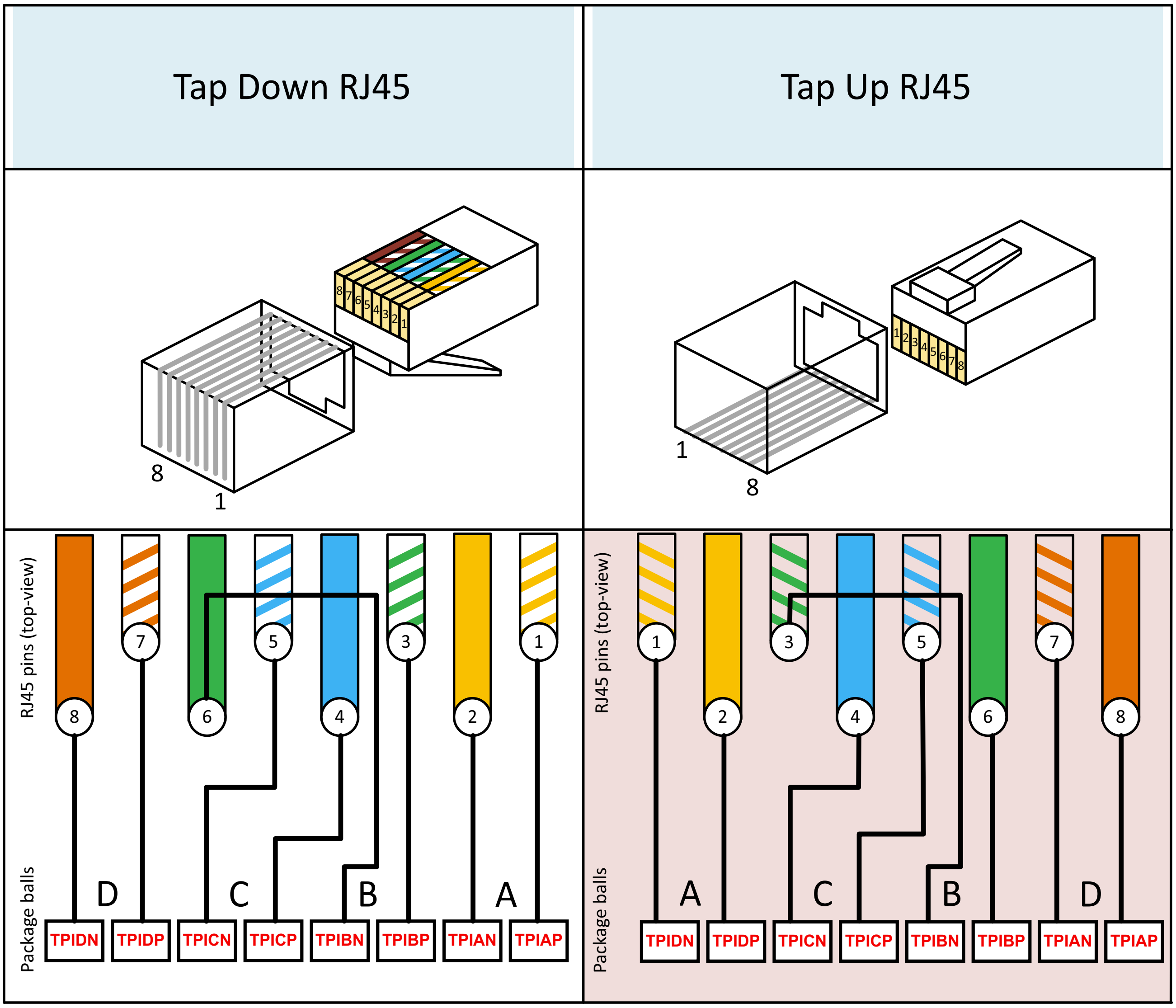



**Figure 7 RJ45 Tap Up or Tap Down Configuration**

### 3.3.8 Wake-on-LAN (WoL)

The GPY212 supports Wake-on-LAN. It generates an interrupt to an external controller when it detects special WoL Ethernet packets. This allows the controller to enter sleep mode if there is no Ethernet traffic to process, and be woken up when traffic starts. WoL packets are detected for all link speeds.This scenario is shown in **Figure 8**.

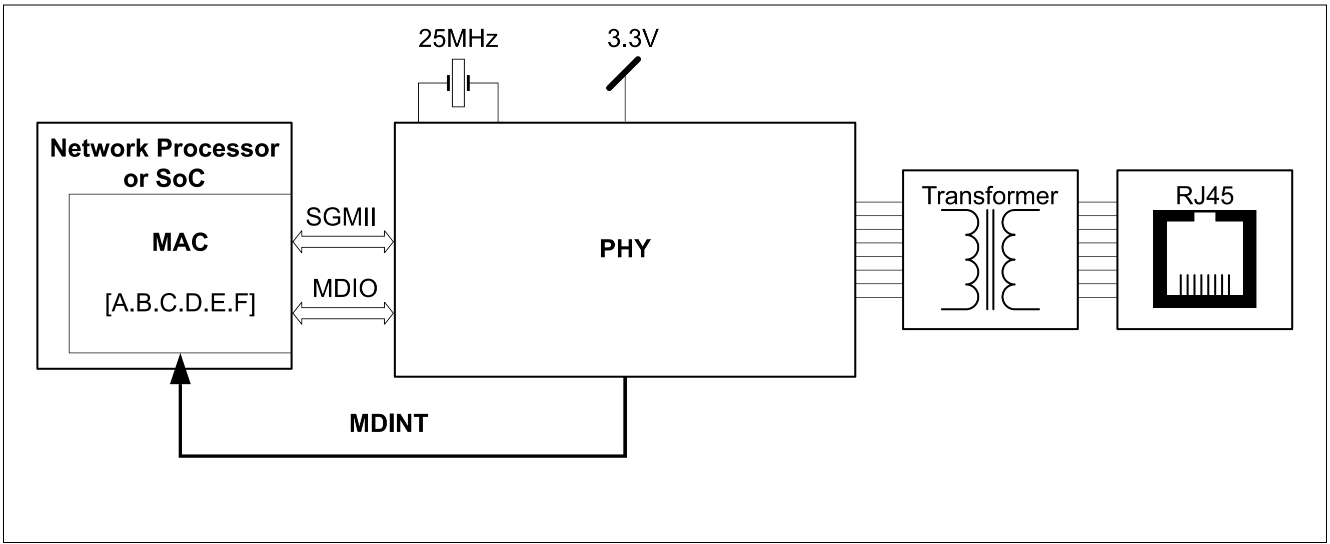



**Figure 8 Block Diagram of WoL Application**

The most commonly used WoL packet is called a magic packet. A magic packet contains the MAC address of the device to be woken up as well as, optionally, a password called SecureON. The MAC address and the optional SecureOn password relevant for the WoL logic inside the GPY212 can be configured in the WOL MDIO registers in “Vendor Specific 2” VSPEC2 MMD device described in **Chapter 4**. When such a configured magic packet is received by the GPY212, an MDINT interrupt is issued.

An example programming sequence for these configuration registers is given in **Table 13**.

**Table 13 Programming Sequence for the Wake-on-LAN Functionality**

| Step | Register Access | Remark |
|---|---|---|
| 1 | `MDIO.MMD.WOLAD01` = $EEFF_H$ | Program the fifth and sixth MAC address bytes |
| 2 | `MDIO.MMD.WOLAD23` = $CCDD_H$ | Program the third and fourth MAC address bytes |
| 3 | `MDIO.MMD.WOLAD45` = $AABB_H$ | Program the first and second MAC address bytes |
| 4 | `MDIO.MMD.WOLPW01` = $4455_H$ | Program the fifth and sixth SecureON password bytes |
| 5 | `MDIO.MMD.WOLPW23` = $2233_H$ | Program the third and fourth SecureON password bytes |
| 6 | `MDIO.MMD.WOLPW45` = $0011_H$ | Program the first and second SecureON password bytes |
| 7 | `MDIO.PHY.IMASK.WOL` = $1_B$ | Enable the Wake-on-LAN interrupt mask |
| 8 | `MDIO.MMD.WOLCTRL.WOL.EN` = $1_B$ | Enable Wake-on-LAN functionality |

## 3.4 SGMII Interface

The GPY212 implements a serial data interface, called SGMII or SerDes, to connect to another chip implementing the MAC layer (MAC SoC). The data rates supported by the SGMII interface are the same as for the TPI (10 Mbit/s, 100 Mbit/s, 1 Gbit/s, or 2.5 Gbit/s). These rates correspond to baud rates of 1.25 Gbaud (for 10/100/1000 Mbit/s using data repetition), and 3.125 Gbaud (for 2.5 Gbit/s).

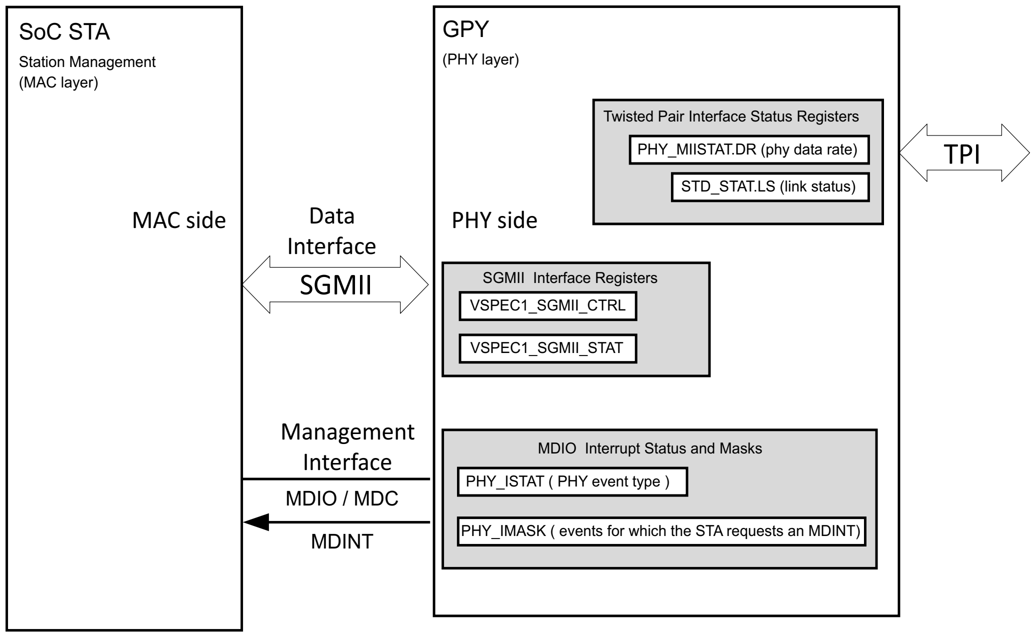
### 3.4.1 SGMII Control and Status Registers

The GPY212 API **[9]** describing the driver software executed on the MAC SoC must be followed to configure the SGMII interface.

The MAC SoC can use MDIO registers to retrieve the GPY212 TPI and SGMII status.

The API controls the SGMII interface using 2 MDIO registers described , as shown in **Figure 9**:

- VSPEC1_SGMII_CTRL is used to enable and configure the SGMI auto-negotiation or force a link configuration. Programming this register is optional as the SGMII interface comes up in a default configuration after reset that does not need any additional control from the STA. The STA can also control the SGMII reset, SGMII powerdown or SGMII loop back using this register. Until SGMII is in powerdown (VSPEC1_SGMII_CTRL.PD = 1) state, programming to other bits on VSPEC1_SGMII_CTRL register is ignored.
- VSPEC1_SGMII_STAT is a read-only register that can be used by the STA to retrieve the SGMII link status, data rate and auto-negotiation completion status.




Overview of SGMII interface between an SoC and GPY, and relevant MDIO/MMD registers

**Operating Procedure**

SoC is responsible for monitoring PHY_ISTAT events, TPI data rate and link status:
LSTC: PHY link status change with new status indicated in STD_STAT.LS
LSPC: PHY link speed change with new TPI speed indicated in PHY_MIISTAT.DR

The GPY PHY side SGMII is set up by the GPY at the same speed as the TPI link.
The MAC SoC is responsible for programming the MAC side SGMII at the matching speed.

**PHY_ISTAT event fields in PHY_ISTAT MDIO register:**

- LSTC: Link state change
- LSPC: Link speed change
- DXMC: Duplex mode change
- MDIXC: MDIX change, polarity change
- ADSC: Auto-downspeed event
- TEMP: PVT Sensor Event
- ULP: Low Power Event
- LOR: Sync E loss of reference
- ANCE: ANEG complete or ANEG Error
- NPRX/NPTX: ANEG Next Page RX or TX
- MSRE: Master Slave Resolution Error
- WOL: Wake-on-LAN event

**Figure 9 GPY212 SGMII Configuration and Status Registers**

### 3.4.2 SGMII Configuration at Power Up

The GPY212 SGMII interface is configured to operate automatically after reset. The STA does not have to change the register VSPEC1_SGMII_CTRL to operate in this default mode:

- SGMII auto-negotiation is enabled
- The TPI configuration after link up defines the SGMII PHY side configuration. The MAC side SoC must configure its SGMII MAC side interface to match the GPY212 PHY side configuration, as explained in **Chapter 3.4.3**, **Chapter 3.4.4**, and **Chapter 3.4.5**

### 3.4.3 SGMII PHY Side Setup According to TPI Setup

The GPY212 PHY side SGMII is set up by the GPY212 at the same speed as the twisted pair interface (TPI) link. To operate the GPY212 in this mode VSPEC1_SGMII_CTRL.FIXED2G5 must be programmed to 0 (default value is 0). This is the default mode.

When a link status changes on the TPI (up/down and speed change), the GPY212 reconfigures its SGMII automatically. In particular, the SGMII clock is changed when the speed changes from 2500 Mbit/s to lower speeds, or vice-versa.

### 3.4.4 SGMII PHY Side Setup Fixed irrespective to TPI Setup

The GPY212 PHY side SGMII is fixed to 2.5G mode irrespective of the twisted pair interface (TPI) link. To operate the GPY212 in this mode VSPEC1_SGMII_CTRL.FIXED2G5 must be programmed to 1 (default value is 0).

When GPY212 intends to operate in this mode, recommendation is to switch to this mode by programming VSPEC1_SGMII_CTRL.FIXED2G5 to 1 when the MDIO interface is available after the power-up. When a link status changes on the TPI (up/down and speed change), the SGMII on GPY212 will be operating on 2.5G speed. To alleviate the packet drops due to rate mismatch on SGMII and TPI link, the host MAC must enable flow control to detect and react to the PAUSE frames generated by PHY. In this mode, an internal buffer path is enabled and hence there will be latency introduced in this mode of operation.

### 3.4.5 SGMII MAC Side Setup by MAC SoC

The MAC SoC (STA) is responsible for monitoring the PHY_STAT events, which indicate TPI data rate and link status. The MAC SoC can monitor link status or link speed changes using the following three possible methods:

- Using the MDIO interface MDINT interrupt and reading the associated event
- Using the MDIO interface polling (reading) of the link status register STD_STAT.LS
- Using the restart of the SGMII ANEG which conveys the new link parameters. In this case, the SGMII Cisco* ANEG must be enabled after power up.

In all three cases:

- The GPY212 reconfigures the PHY side SGMII to match the TPI setup
- The MAC SoC must set up the MAC side SGMII to match the PHY side SGMII

### 3.4.6 SGMII Link Monitoring by MAC SoC

The GPY212 indicates its interface status using the following registers, as indicated in **Figure 9**:

- MDIO register PHY_MIISTAT to indicate the TPI status
- MDIO register SGMII_STAT to indicate the SGMII status

A change of status on the TPI can be indicated by the MDIO interrupt MDINT. MDINT is generated if the STA has programmed the event mask in the PHY_IMASK register corresponding to any of the following events occurring on the TPI:

- LSTC: Link state change
- LSPC: Link speed change
- DXMC: Duplex mode change
- MDIXC: MDIX change, polarity
- ADSC: Auto-downspeed event
- TEMP: PVT Sensor Event
- ULP: Low Power Event
- LOR: Sync E loss of reference
- ANCE: ANEG complete or ANEG error
- NPRX/NPTX: ANEG next page RX or TX
- MSRE: Master Slave Resolution Error
- WOL: Wake-on-LAN

The MDINT signal is deasserted by the GPY212 when the MAC SoC STA performs a READ access to the MDIO register PHY_ISTAT.

The events relevant to the TPI status that are useful for monitoring SGMII are LSTC and LSPC.

#### 3.4.6.1 Actions on TPI Link Down / Link Up Status Change

The GPY212 does not systematically bring the SGMII link down when the TPI link is down.

The STA can read the status on each side (SGMII and TPI) and make the appropriate decision about the SGMII link down.

For example, if the TPI status is in link down for too long, the STA can take the decision to also power down the SGMII.

#### 3.4.6.2 New TPI Link Up at Same Speed

The following scenario describes a transition on TPI that does not require any restart or change of mode on SGMII:

- SGMII is set to a specific speed and SGMII link is up
- TPI goes to link down – and link up
- When TPI is down, the SGMII side is transmitting Idle packets
- TPI links up at the same speed as before

In these cases, the GPY212 does not reprogram the PHY side SGMII.

#### 3.4.6.3 Change of Speed After a New Link Up on TPI

The following scenario describes a transition on TPI that requires a change of mode on SGMII:

As a PHY side SGMII controller, the GPY212 enforces the speed on the MAC side SGMII.

For a change in TPI speed within the [10/100/1000 Mbit/s] rate subset, there is no change in baud speed on SGMII:

- New TPI configuration is reflected in the MDIO status registers and the MDINT interrupt is triggered to indicate the change as explained in **Chapter 3.4.6**.
- GPY212 programs its SGMI to the new speed. In particular, for speeds 10 and 100 Mbit/s, the GPY212 SGMII PCS performs data repetition by 100x and 10 x respectively.

- SGMII lane clock remains unchanged at 1.25 Gbaud clock speed.
- If Cisco ANEG is enabled, the GPY212 conveys the changed speed parameters by restarting SGMII ANEG.
- If Cisco ANEG is disabled, the GPY212 changes the SGMII configuration immediately and expects the MAC SoC to monitor the link change and match the same configuration.

For a change in data speed from the SGMII subset [10/100/100 Mbit/s] to SGMII* subset [2500 Mbit/s], there is a need to change the SGMII lane baud speed to the over clocked 3.125 Gbaud:

- New TPI configuration is reflected in the MDIO status registers and the MDINT interrupt is triggered to indicate the change as explained in **Chapter 3.4.6**.
- GPY212 reprograms its SGMII to the 3.125 Gbaud clock speed.
- If Cisco ANEG is enabled, the GPY212 conveys the changed speed parameters by restarting SGMII ANEG.
- If Cisco ANEG is disabled, the GPY212 changes the SGMII configuration immediately and expects the MAC SoC to monitor the link change and match the same configuration.
- The MAC SoC reconfigure its MAC side SGMII to the new baud rate.

### 3.4.7 Auto-negotiation Modes Supported by SGMII

Two modes are supported for the SGMII auto-negotiation protocol:

- Cisco* Serial-GMII Specification 1.8 [4]
- 1000BX IEEE 802.3 following IEEE Clause 37 [2]

The information exchange mechanism of ANEG is the same in both modes, but the parameters communicated are slightly different. The 1000BX scheme allows for some parameters to be aligned with the highest common capability between the two sides of the SerDes. The Cisco* SGMII scheme uses the protocol to communicate the configuration requested by the PHY side SGMII to the MAC side SGMII (e.g. speed request); it is a one-way request.

The parameters communicated by the Cisco* ANEG protocol [4] from SGMII-PHY to SGMII-MAC are:

- Link Up or Link Down indication (reflects the TPI status)
- Half Duplex or Full Duplex mode
- Data rate (standard only supports 10 Mbit/s to 1000 Mbit/s)
- EEE capability support
- EEE Clock Stop capability support

The parameters exchanged by the 1000BX ANEG protocol [2] are:

- Remote fault
- Pause support and mode (symmetrical or asymmetrical)
- Half Duplex of Full Duplex

The Cisco* ANEG protocol is recommended for a standard application.

#### 3.4.7.1 Enabling SGMII Auto-negotiation Mode

SGMII auto-negotiation is ON at power up. ANEG can be enabled/disabled by setting register field VSPEC1_SGMII_CTRL.ANEN. In the default case:

- GPY212 PHY side SGMII is configured by GPY212 to match the TPI link configuration.
- GPY212 uses ANEG to convey the new link parameters to the MAC SoC.
- MAC SoC MAC side SGMII must be configured by the MAC SoC to match the GPY212 PHY side SGMII configuration.

## 3.5 LED Interface

### 3.5.1 LED

The GPY212 allows 4 LEDs to be used for visual status indication. Each pin can drive a single color LED or dual color LED.

### 3.5.2 LED Configuration

The GPY212 API **[9]** describing the driver software executed on the MAC SoC must be followed to configure this interface.

In single color mode, the external LED can be connected to either the ground or to power as shown in **Figure 10**.

The "power" mode is only supported for single color LEDs.

The connection of single and dual color LEDs, when the pin is also used for pin strapping, is illustrated in **Figure 11** and **Figure 12**.

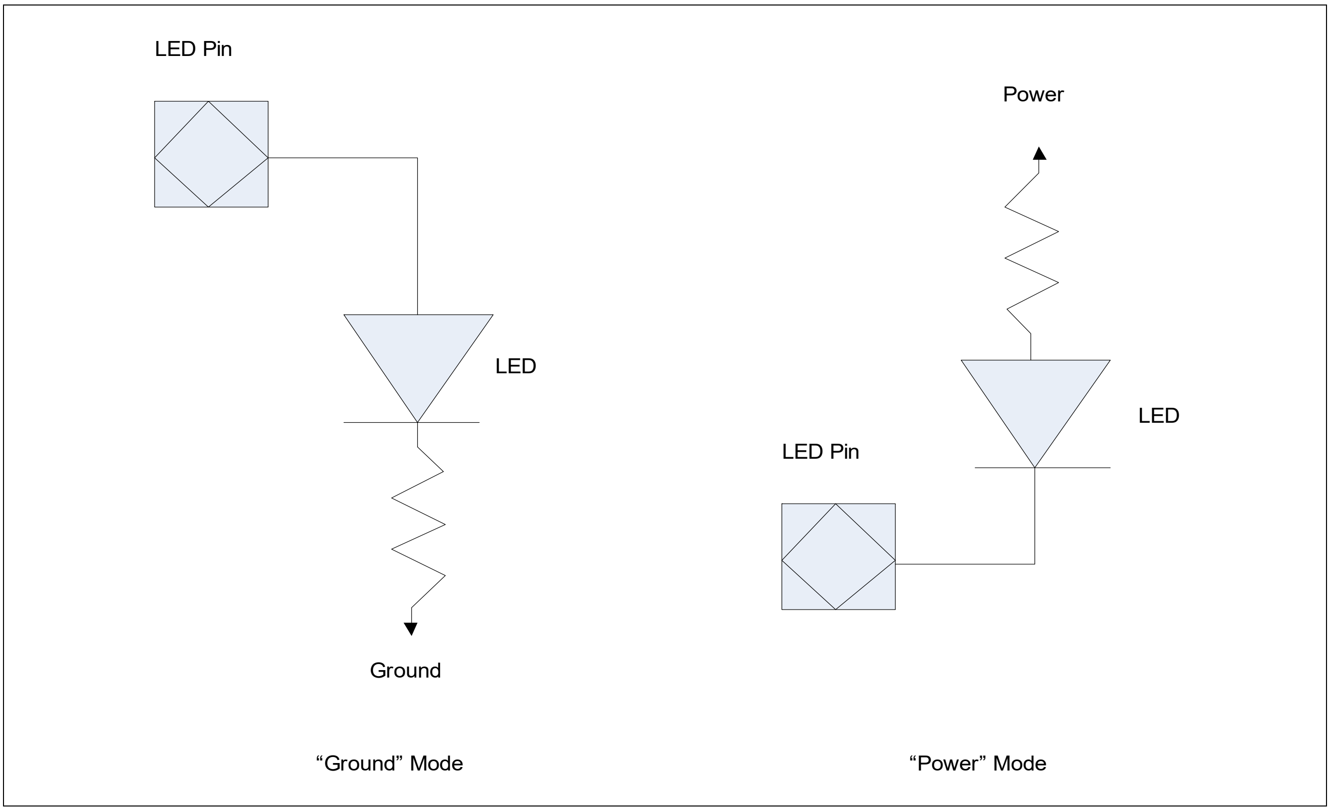



**Figure 10 LED Connection Options to Ground or Power Supply**

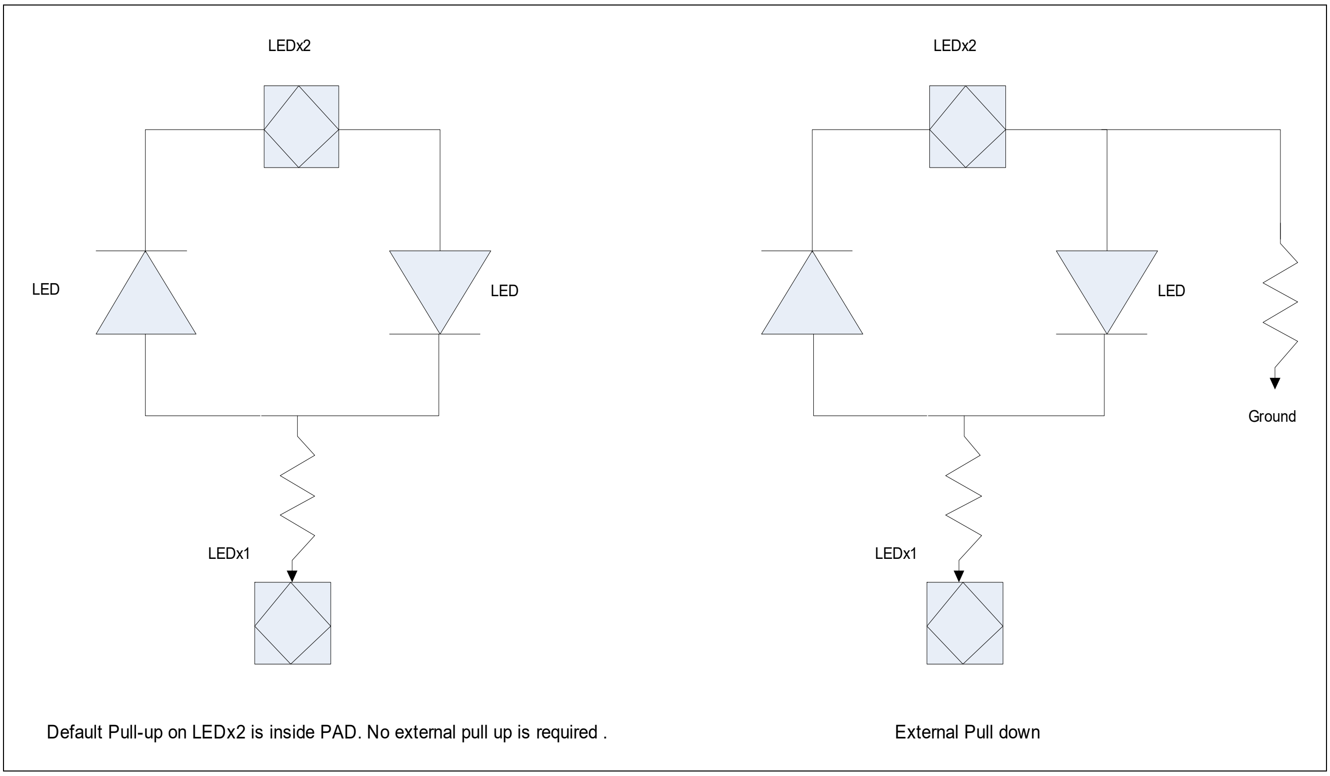



**Figure 11 Connection of a Dual Color LED and Configuring Pin Strap Value**

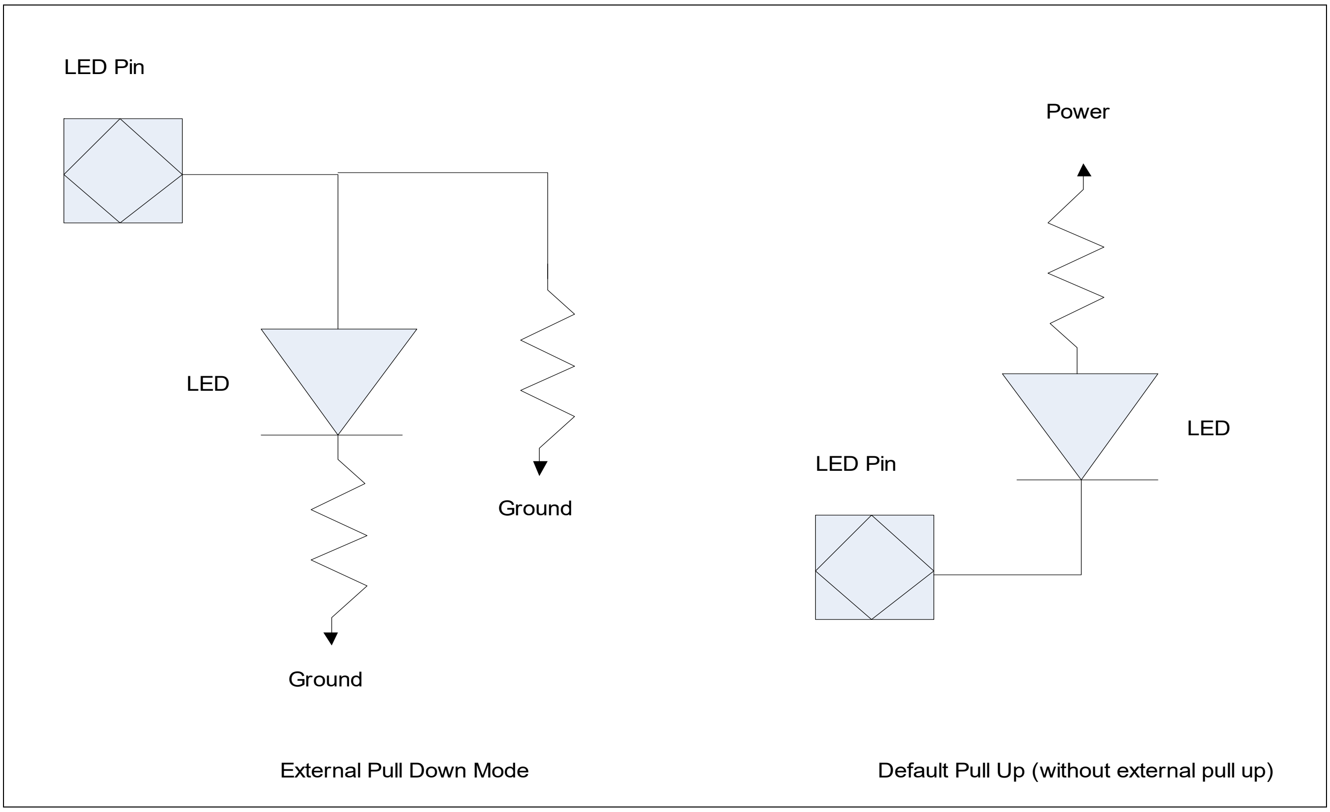



**Figure 12 Connection of a Single Color LED and Configuring Pin Strap Value**

### 3.5.3 LED Brightness Control

There are two LED brightness modes configurable by the GPY API, based on the system requirement.

- LED Brightness Level Max Mode
  Fixed level signal (no pulses) for maximum brightness which can also be used as control signal for other purposes.
- LED Brightness Level Control Mode (Constant Mode)
  Allows the configuration of 16 levels of LED brightness as described in **Brightness Control**.

**Brightness Control**

This block controls the brightness of the LED by way of controlling the time duration the LED is ON/OFF, and due to persistence of the eye, LED brightness will be perceived. When LED is off, the output is disabled. When LED is on, the output is enabled. Brightness control controls the LED output enable directly.

As show in **Figure 13**, brightness control frequency is 100Hz. Each period is divided into 64 slots.

When LED brightness control is disabled, LED is enabled in all 64 slots.

When LED brightness control is enabled, LED is enabled for consecutive n slots. n is determined by brightness level configured. LED output is disabled in the 64th slot.

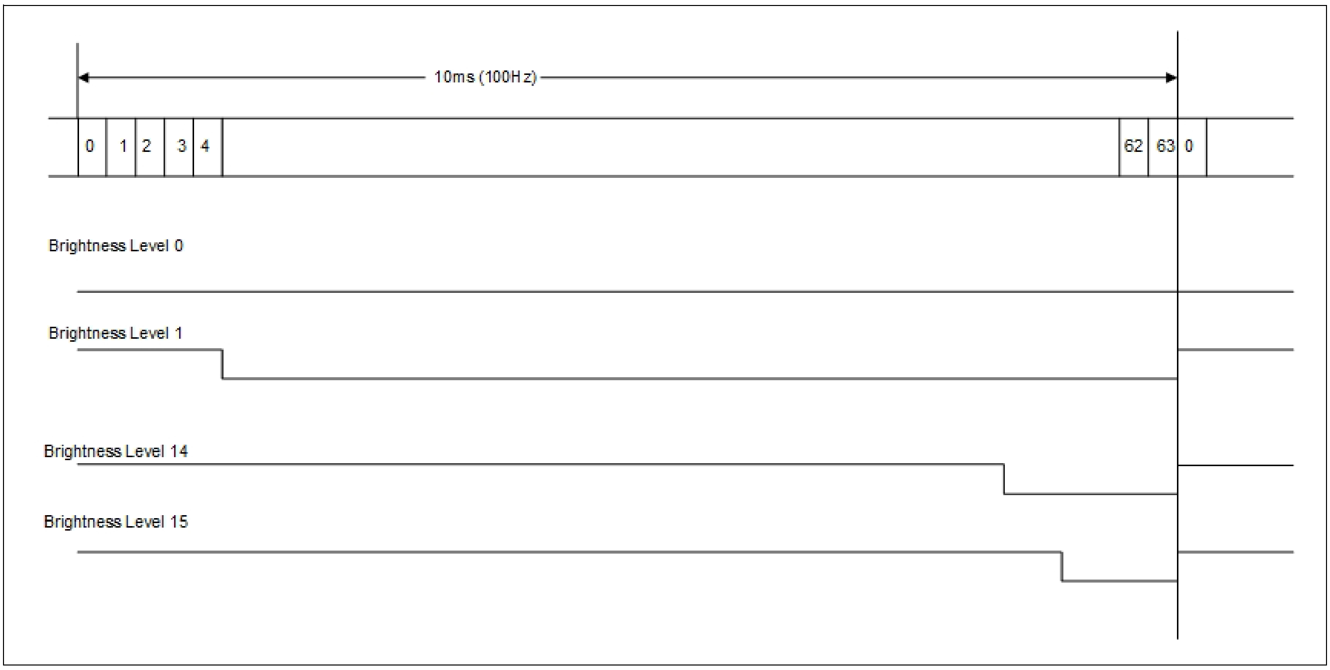



**Figure 13 LED Brightness Control By Controlling LED Output Enable/Disable**

## 3.6 Precision Time Protocol (PTP) Feature

### 3.6.1 PTP Feature Purpose

The GPY212 provides support for Precision Time Protocol (according to PTP Protocol IEEE 1588 Version 2, IEEE 802.1as, and IEEE P802.3bf), which is used to precisely synchronize clocks at the system level. The station manager (STA) can select the GPC1 or GPC2 alternate functions to input a time stamp synchronization request signal (TsSync). For each edge transition on TsSync signal, the GPY212 captures a time stamp. Alternatively, for more precision, the GPY212 supports hardware assisted physical layer time stamping. In this case the TsSync is triggered by the physical layer.

The time stamp is inserted in a PTP event message. The PTP protocol is executed by the STA at the OSI layer above UDP/ IP or MAC layer. The PTP protocol can choose 1-step or 2-step time stamping, and both are supported by the GPY212:

- 2-step time stamping: This scheme uses a Follow_Up message to carry the time stamp of the corresponding sync message. The time stamp is not inserted in the sync message on the fly when the packet is being transmitted, but later in the next PTP message. This scheme allows the GPY212 to perform the hardware assisted precise time stamping capture, using the PHY layer to precisely indicate when the packet Start-of-Frame Delimiter (SFD) symbol is sent out or received on the physical layer. The time stamp, together with the corresponding packet CRC is stored in a memory area on the GPY212. The STA reads this time stamp using the MDIO interface.
- 1-step time stamping: This scheme is used to reduce the number of PTP messages. In this scheme, the GPY212 MAC inserts the time stamp in the sync message on the fly when it passes through the GPY MAC layer. The GPY212 inserts the time stamp in the PTP sync message on the fly.

Special care must be taken at the system level configuration to ensure that the MACsec feature is configured to disable the encryption of PTP time stamp packets, when both PTP and MACsec are enabled concurrently.

### 3.6.2 PTP Feature Configuration

The GPY212 API [9] describing the driver software executed on the MAC SoC must be followed to configure this feature.

The following steps are used by the API to configure and enable the 1588 feature:

- [Optionally] STA selects GPC1 or GPC2 to be used to input the TsSync, using the GPIO configuration API. This is not required if 2-step PTP mode is chosen, because in that case the TsSync is generated internally by the GPY212 physical layer.
- STA selects 1-step or 2-step PTP mode .
- STA enables 1588 feature: this triggers the GPY212 firmware to configure the internal GMAC and Packet Manager to capture the time stamps of the PTP packets.

## 3.7 Pulse Per Second (PPS) Feature

### 3.7.1 PPS Feature Purpose

The GPY212 provides support for PPS signal generation. This can be used at the system level to synchronize various chips. The general purpose clock pins GPC1 and GPC2 can be configured for this purpose.

### 3.7.2 PPS Feature Configuration

The GPY212 API [9] describing the driver software executed on the MAC SoC must be followed to configure this feature.

The following steps are used by the API to configure and enable the PPS feature:

- Optionally, STA uses the configuration API to configure the desired PPS frequency. By default, it is 1 second.
- STA enables the PPS feature . This triggers the GPY212 firmware to configure the GPY212 to output a PPS signal on the selected GPC1 or GPC2.

## 3.8 Smart-AZ Feature

The Smart-AZ feature is relevant when the GPY212 is connected to a MAC SoC that does not implement the EEE feature in its MAC layer. In this case, the MAC SoC cannot initiate a transition to the low-power idle state.

To alleviate the limitation of such a MAC SoC, the GPY212 detects the conditions that may lead to low-power idle and generates the control messages to enter EEE mode in accordance with the IEEE 802.3az standard.

The Smart-AZ feature is always enabled.

## 3.9 MACsec Feature

The GPY212 supports the following MACsec features:

- Compliance to IEEE 802.1AE, IEEE 802.1AEbn and IEEE 802.1AEbw standards
- AES-256 and AES-128 encryption and decryption in both RX and TX directions
- 16 MACsec security channels (SCs) and 32 MACsec associations (SAs)
- The following modes per security association:
  – Integrity check mode only
  – Both confidentiality (data payload encryption) and integrity check mode
- RX non-MACsec packet filtering mode:
  – Forward all packets with Ethernet type different to MACsec type.
- RX MACsec association lookup:
  – If MACsec is enabled, lookup is based on SCI+AN for packets with MACsec tag. If SCI+AN is found, then the packet association is found. The packets with unknown association are forwarded.
  – Unknown association packets are marked with "MACsec unknown" status and counted.
  – There is corresponding MACsec configuration (security mode, key etc) for each association.
  – MACsec tag and ICV (Integrity Check Value) fields are stripped.
- TX MACsec association lookup:
  – With special tag mode, the security channel and MACsec enable/bypass are configurable based on bit 5:0 of the byte 5 in special tag and the packet header.
  – Without special tag mode, the security channel and enable/bypass is based on packet header lookup.
  – There is corresponding MACsec configuration (MACsec enable, security mode etc) for each association.
- MACsec counters:
  – Number of Integrity Check Value (ICV) failed packets
  – Number of MACsec unknown association packets (excluding ICV failed packets)
  – Number of MACsec bypass packets
  – Number of total packets

### 3.9.1 MACsec Purpose

The GPY212 integrates MACsec frame processing engine hardware to execute MACsec frame transformation along with frame classification and statistic counter updates.

The MACsec engine operates in conjunction with a MACsec driver executed on the MAC SoC. The upper layers of the MACsec protocol in charge of key provisioning are under the control of the MAC SoC.

### 3.9.2 MACsec Feature Usage

The feature is relevant when the GPY212 is connected to a MAC SoC that does not support MACsec in its Layer-2. In this case, the GPY212 performs the MACsec data transformations that are normally performed by the SoC.

The MACsec driver is part of the MAC SoC API software documented in the GPY212 API [9]. The MACsec feature is enabled by default in the GPY212 chip variant. It can be disabled by the API.

***Attention: However, to use this feature in GPY212, the host SoC must send the key for MACsec (Secure Association Key - SA Key) in plain text to the GPY212. Hence, this SA Key is exposed on MDIO bus between the host SoC and GPY212. In environments where this plain access to the MACsec SA Key is a concern, it is recommended to use the host SoC to perform the complete end-to-end MACsec encryption/ decryption.***

### 3.9.3 MACsec Engine Control API Executed on MAC SoC

The MACsec engine on the GPY212 is controlled by a MACsec driver executed on the MAC SoC. The control interface is the MDIO.

***Attention:** When using MACsec, the host MAC mustbe configured to accept under-size packets. This includes, for example, control words like ARP, PING with correct CRC, which are per se shorter than 64B prior to encryption.*

## 3.10 Power Management

This chapter describes the power management functions of the GPY212.

### 3.10.1 Power States

Figure 14 illustrates the power states and transition of the GPY212. In this state diagram, the (0.11) syntax corresponds to the value of bit 11 from register 0 in device 0. This is the "PD" power down bit in MDIO STD_CTRL described in Chapter 4. The station management can use this STD_CTRL.PD field to bring the physical interface to SLEEP state.

The other states are automatically entered by the GPY212 depending on the context, and following the Energy Efficient Ethernet protocol. This is done without need for any intervention from STA.

Acronyms "NLP" and "FLP" respectively mean "Normal Link Pulse" an "Fast Link Pulse". These pulses are received on the twisted pair interface from a link partner and used to wake up the GPY212 and enter auto-negotiation.

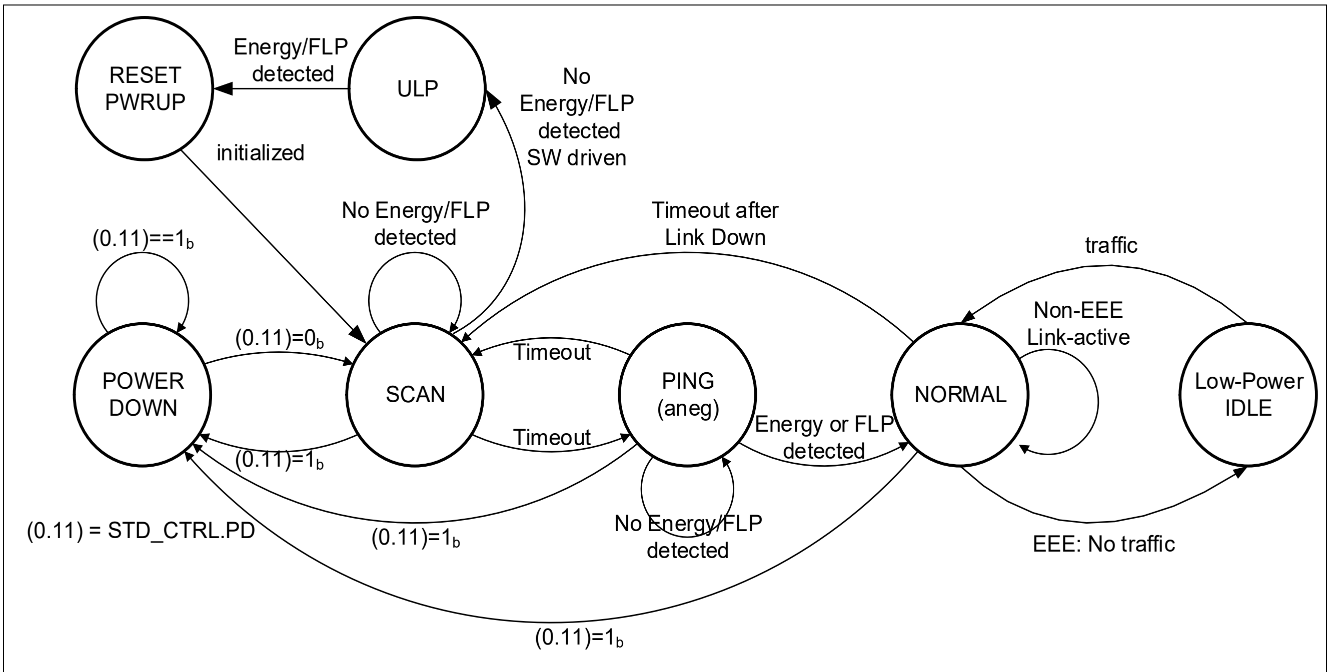



**Figure 14 State Diagram for Power Down State Management**

### 3.10.2 RESET Power Up

This is the state in which the GPY212 starts up after either a hardware reset or power up.

Once initialized, the GPY212 will always transition to SCAN state.

### 3.10.3 SLEEP State

The SLEEP state is entered by setting "power down" bit 11 of the MDIO standard register STD_CTRL (0.11) to logic 1, regardless of the current state of the device. The SLEEP state corresponds to power down as specified in IEEE 802.3, Clause 22.2.4.1.5. Some signal processing blocks are stopped to save energy, but the GPY212 still responds to MDIO messages. The SGMII interface to the MAC SoC is switched off as well.

The SLEEP state exit is triggered by setting the MDIO standard register (0.11), which generates a transition to SCAN state.

### 3.10.4 SCAN State

The SCAN state differs from the SLEEP state because the receiver periodically scans for signal energy or FLP bursts on the twisted pair interface. There is no transmission in this state. If a FLP burst is received, the GPY212 enters the auto-negotiation protocol to exchange capabilities with the link partner and establish a data link in NORMAL state.

### 3.10.5 PING State

The PING state is similar to the SCAN state except that the transceiver transmits an FLP burst onto the TPI for a programmable amount of time. This is used to wake potential link partners from the power down state. This state corresponds to the state of “ANEG” described in Clause 28 of the IEEE standard [2].

### 3.10.6 ULP State

This ultra-low power state is supported in the internal DCDC SVR configuration. This feature is not supported in external supply of the $V_{LOW}$ domain.

Ultra-low power (ULP) state in GPY212 is enabled by configuring MDIO register PHY_CTL2.ULP. The ULP state is entered automatically when there is no Ethernet cable connected to the GPY212. The GPY212 firmware detects this condition when no energy or FLP is present on the twisted pair interface and enters the ULP state. It is intended to set the GPY212 into maximum power saving state. In this state, most digital domains are powered down. Only a minimal amount of circuitry (analog/digital) operates to detect signal energy on the receiver of one twisted pair interface and trigger a wake-up.

When GPY212 is in ULP state, the STA does not have access to the MDIO/MMD registers.

The ULP state is exited upon detection of signal energy on the twisted pair (either NLP or FLP). The GPY212 transitions to the RESET Power Up state automatically. The STA host can also triggers an ULP state exit by applying a reset sequence on the GPY212 using HRSTN pin.

The STA host can be informed of the ULP entry condition and can choose to acknowledge it before granting ULP entry. By setting PHY_IMASK.ULP bit to ACTIVE, the STA requests the MDINT interrupt from GPY212 when the entry conditions are met. If PHY_CTL2.ULP_STA_BLOCK is ON then GPY212 will enter ULP only after STA reads the interrupt status register PHY_ISTAT else the entry to ULP is unconditional. All the ULP related control bits and communication mechanism between STA and GPY is shown in the flowchart in **Figure 15**.

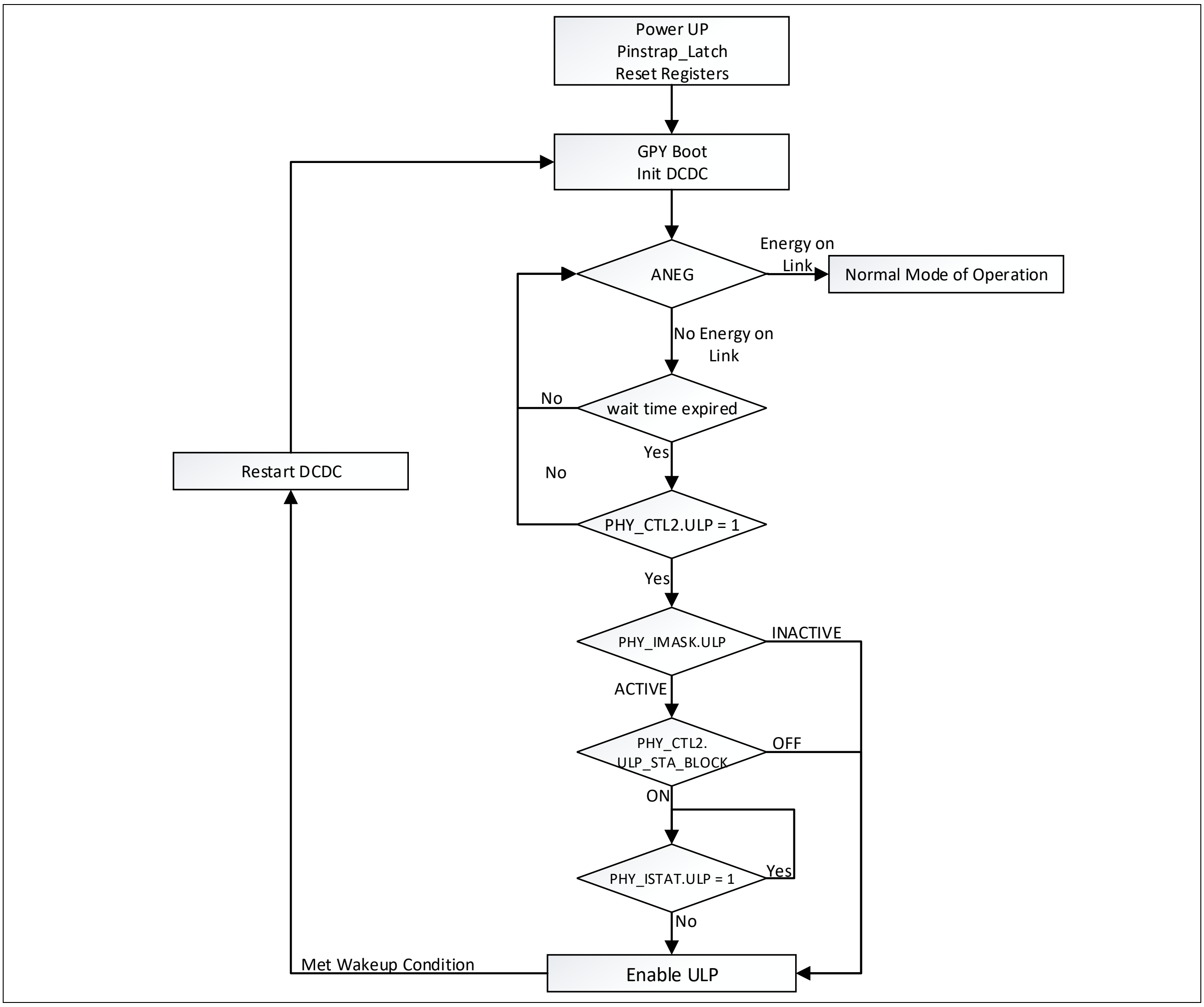



**Figure 15 ULP Sequence**

**Table 14 ULP State Entry and Exit Sequence**

| Step | State | Remark |
|---|---|---|
| 1 | ACTIVE state, the ULP feature is enabled by programming PHY_CTL2.ULP = 1, if the Internal DCDC is used. | Use MDIO register PHY_CTL2.ULP to enable / disable the ULP feature. With External DCDC, PHY_CTL2.ULP must always be disabled. |
| 2 | ANEG, Ability Detect state | The firmware detects that no energy is seen on the cable when no FLP is received for a long period of time. This time can be configured with register: VSPEC1_NBT_DS_C-TRL.NRG_RST_CNT (value to program = time in seconds). Default time is 4 seconds (VSPEC1_NBT_DS_C-TRL.NRG_RST_CNT = 4). |
| 3 | ULP Entry | GPY212 saves MDIO ULP persistent registers.<br>GPY212 Internal DCDC SVR ramps down the VDD. |

**Table 14 ULP State Entry and Exit Sequence** (cont'd)

| Step | State | Remark |
|---|---|---|
| 4 | ULP State | Power consumption is saved in this state.<br>GPY212 listen to energy pulses from Link Partner ANEG as a condition to trigger ULP exit. Only a minimal amount of circuitry operates to detect signal energy on TPI and trigger a wake-up.<br>GPY212 GPIOs, LEDs and MDIO interface are disabled. |
| 5 | ULP Exit, based on Energy detected on cable. (Option 1) | Internal DCDC SVR ramps up the VDD.<br>GPY212 restores the MDIO ULP persistent registers.The STA is responsible to restore any custom MDIO information that were not saved in the group of ULP persistent registers. |
| 6 | ULP Exit, based on HRSTN request from STA. (Option 2) | The STA can also request a ULP exit by sending a reset sequence using HRSTN. In this case, the ULP MDIO persistent registers cannot be used, and the GPY212 re-starts from its default MDIO register configuration. The STA must reprogram any MDIO specific configuration. |
| 7 | ANEG, LINK-UP and ACTIVE | GPY212 operates in Normal Power Modes. |

The list of persistent MDIO register saved and restored during ULP entry-exit is detailed in **Table 15** below:

**Table 15 ULP Persistent Registers**

| S.No | Register/Register Field | S.No | Register/Register Field | S.No | Register/Register Field |
|---|---|---|---|---|---|
| 1 | STD_CTRL.SSM | 16 | PHY_CTL1.POLB | 31 | VSPEC1_SGMII_CTRL.SSM |
| 2 | STD_CTRL.DPLX | 17 | PHY_CTL1.POLC | 32 | VSPEC1_SGMII_CTRL.EEE_CAP |
| 3 | STD_CTRL.ANEN | 18 | PHY_CTL1.POLD | 33 | VSPEC1_SGMII_CTRL.DPLX |
| 4 | STD_CTRL.SSL | 19 | ANEG_CTRL.ANEG_ENAB | 34 | VSPEC1_SGMII_CTRL.RXINV |
| 5 | STD_AN_ADV.TAF | 20 | ANEG_MGBT_AN_CTRL.LDL | 35 | VSPEC1_SGMII_CTRL.ANEN |
| 6 | STD_AN_ADV.XNP | 21 | ANEG_MGBT_AN_CTRL.FR | 36 | VSPEC1_SGMII_CTRL.SSL |
| 7 | STD_GCTRL.MBTHD | 22 | ANEG_MGBT_AN_CTRL.FR2G5BT | 37 | VSPEC1_NBT_DS_CTRL.NO_NRG_RST |
| 8 | STD_GCTRL.MBTFD | 23 | ANEG_MGBT_AN_CTRL.AB2G5BT | 38 | VSPEC1_NBT_DS_CTRL.DOWNSHIFTEN |
| 9 | STD_GCTRL.MS | 24 | ANEG_MGBT_AN_CTRL.PT | 39 | VSPEC1_NBT_DS_CTRL.DOWNSHIFT_THR |
| 10 | STD_GCTRL.MSEN | 25 | ANEG_MGBT_AN_CTRL.MS_MAN_EN | 40 | VSPEC1_NBT_DS_CTRL.NRG_RST_CNT |
| 11 | PHY_IMASK | 26 | ANEG_MGBT_AN_CTRL.MSCV | 41 | VSPEC1_PM_CTRL |
| 12 | PHY_CTL1.AMDIX | 27 | ANEG_EEE_AN_ADV1.EEE_100BTX | 42 | VSPEC1_LED0 |
| 13 | PHY_CTL1.MDIAB | 28 | ANEG_EEE_AN_ADV1.EEE_1000BT | 43 | VSPEC1_LED1 |
| 14 | PHY_CTL1.MDICD | 29 | ANEG_EEE_AN_ADV2.EEE2G5 | 44 | VSPEC1_LED2 |

**Table 15 ULP Persistent Registers**

| S.No | Register/Register Field | S.No | Register/Register Field | S.No | Register/Register Field |
|---|---|---|---|---|---|
| 15 | PHY_CTL1.POLA | 30 | VSPEC1_SGMII_CTRL.ANMODE | 45 | VSPEC1_LED3 |
| | | | | 46 | VSPEC1_SGMII_CTRL.SGMII_FIXED2G5 |

### 3.10.7 NORMAL State

The NORMAL state is used to establish and maintain a link connection. If a connection is dropped, the GPY212 moves back into SCAN state.

### 3.10.8 Low-Power IDLE State: Energy-Efficient Ethernet

The IEEE 802.3 standard [2] describes the Energy-Efficient Ethernet (EEE) operation that is supported by the GPY212. EEE is supported in the various speeds of 10BASE-Te, 100BASE-TX, 1000BASE-T, and 2.5GBASE-T. The general idea of EEE is to save power during periods of low link utilization. Instead of sending active idle data, the transmitters are switched off for a short period of time. This is called the quiet period in the standard. The link is kept active by means of a frequent refresh cycle initiated by the PHY itself during low power state. This sequence is repeated until a wake request is generated by one of the link partner MACs. GPY212 follows the IEEE 802.3 standard regarding EEE. The principle is shown in **Figure 16**. This state is entered automatically when the low-power idle conditions are met.

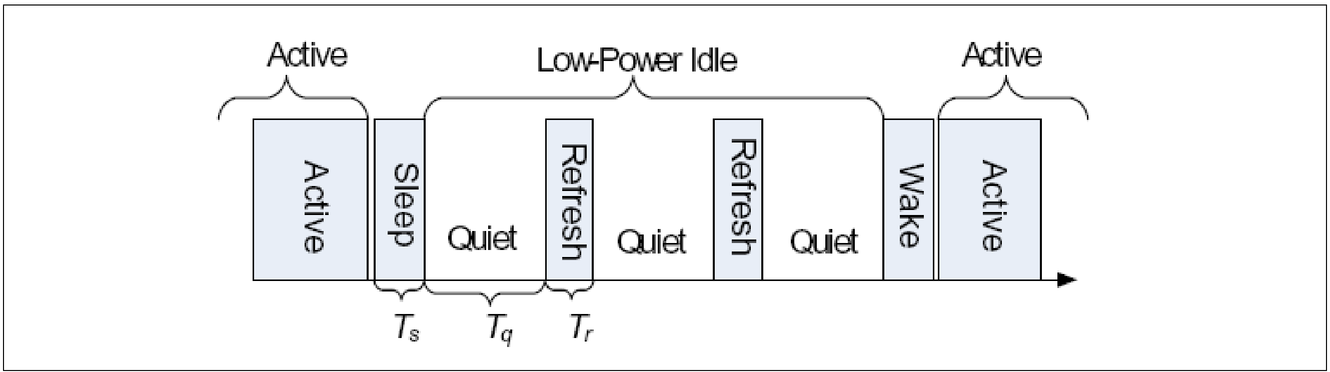



**Figure 16 EEE Low-Power Idle Sequence**

## 3.11 Field Firmware Upgrade (FFU)

The GPY212 provides a Firmware Field Upgrade (FFU) feature, that allows feature and functional enhancements of the GPY212 in the field.

Initially, the GPY212 is provided with a permanent on-chip firmware image in a one-time programmable memory (OTP).

With a low-cost serial flash connected to the GPY212's SPI interface, a new firmware image can be downloaded over the GPY212 to the Flash and the GPY212 can fetch the upgraded firmware from this Flash after a reboot.

For security reasons, the GPY212 will only accept firmware images, which are electronically signed by MaxLinear.

In case a Flash image cannot be authenticated by the GPY212 or a Flash image download is aborted or fails, the GPY212 will default to run from the internal firmware image in OTP.

The GPY API [9] describing the driver software executed on the MAC SoC must be followed to execute this feature. It provides information on the update process and which actions are required in the MAC SoC application.

Security features to prevent rollback of image to a previous version (Flash Anti-Rollback) and to prevent flash wear-out due to too frequent update (Flash Anti-wear out) are not supported within the GPY212. If the system (SoC) to which the GPY212 is attached, mandates such features, they can be supported by the system.

- The host software is expected to verify a firmware before downloading it to the flash, and that the version number of the new firmware is higher than the one installed.
- The system is also expected to ensure that a firmware is only installed when there is a new firmware available and not, for instance, after every reboot.
- Flash memory components typically support a minimum of 100,000 erase/program cycles, so flash wear-out is unlikely. However, ensuring a minimum interval between flash updates decreases the likelihood of wear-out. An interval of 1 hour sets the minimal time of wear-out to more than 11 years.

# 4 MDIO and MMD Register Interface Description

The following sections describe the MDIO and MMD registers, which are standardized by IEEE 802.3 [2] and [3], and available to support the GPY212 feature set. These registers can be accessed by an external management entity (also called STA in IEEE) to control, configure or read the status of the GPY212. After power-on, the GPY212 resets the MDIO and MMD registers to default values that are sufficient to operate without specific programing.

All the register definitions, behaviors and fields are strictly compliant with the IEEE 802.3 [2] and [3]. Refer to IEEE 802.3 for more detailed explanations of the registers. The only registers that are not referenced in IEEE 802.3 are two register groups that are "vendor specific": VSPEC1 and VSPEC2. These allow custom functions related to the GPY212. In the register descriptions, the section or table references refer to the IEEE 802.3 [2] and [3] documents.

## 4.1 Definitions

The following acronyms are used in the IEEE 802.3 standard and commonly used in the Ethernet technical domain:

- **STA**: Station Management. A host connected to the MDIO interface. STAs are generally Media Access Controllers (MACs). The STA drives the MDIO bus as a clock master and the GPY212 is MDIO slave.
- **Host**: Used as a synonym of STA in this document.
- **PHY**: Physical Layer. In the GPY212 this encompasses Analog Signal Processing, Digital Signal Processing, PCS. The PHY contains several sub-layers that are individually manageable entities known as MDIO manageable devices (MMDs).
- **MMD**: MDIO Manageable Device. The list of MMDs available in the GPY212 is in **Chapter 4.3**.
- **Device**: In the context of MDIO/MMD registers, a device is a register bank grouped by logical sub-layers of the PHY layer.
- **Clause**: Refers to a particular section of the IEEE 802.3 standard [2] and [3]. In particular Clause 22 describes MDIO device 0, and Clause 45 describes the other MMDs.
- **MII**: Media Independent Interface. This encompasses the MDIO as well as the (G)MII as described in Clause 22. STD registers in device 0 are also called MII registers.

## 4.2 Register Naming and Numbering

The register numbering convention in this document is similar to that of IEEE 802.3:

The numbering syntax uses 3 numbers “a.b.c” as specified in IEEE 802.3 paragraph 45.1, and the notation is generalized to Clause 22 registers in device 0 “STD”. The alphanumeric syntax also uses the same structure and uses the names of the MMD devices, registers and register fields separated by underscore and dot as described below.

### 4.2.1 Register Numbering

The syntax is as follows, with a, b, c written as decimal numbers:

a.b.c = <DEVICE_NUMBER>.<REGISTER_NUMBER>.<FIELD_NUMBER>

When the last indicator (c) is omitted, the register numbering refers to the full register.

When a field is more than a single bit, the bit range is indicated using a semicolon (e.g. 1:3 is the field of bits 1 to 3). In an MDIO register, the least significant bit is bit 0 and most significant bit is bit 15. All MDIO registers are 16 bit wide.

### 4.2.2 Register Naming

The syntax is as follows, with AA, BB, CC written as alphanumeric strings:

AA.BB.CC = <DEVICE_NAME>_<REGISTER_NAME>.<FIELD_NAME>

When the last indicator (CC) is omitted, the register naming refers to the full register.

The fields named Res, RES1, RES2 refer to reserved fields as per IEEE 802.3 documents.

### 4.2.3 Examples

STD_STAT.ANOK is the name of the field 0.1.5, which indicates auto-negotiation complete.

ANEG_CTRL.ANEG_RESTART is the name of the field 7.0.9, which allows the STA to restart the Ethernet ANEG procedure.

ANEG_PHYID1 is the complete 16-bit register number 7.2, for the PHY identifier 1 number.

VSPEC1_LED1.BLINKS is the 4-bit wide field number 30.2.15:12, which contains LED1 slow blinking configuration.

## 4.3 MMD Devices Present in GPY212

The MMD devices implement groups of standardized registers under the management of the STA. They are defined in IEEE 802.3.

**Table 16 MDIO / MMD Devices Present in GPY212**

| MDIO / MMD Name | Device Number (decimal) | Description |
|---|---|---|
| STD | 0 | MDIO Standard Device as described in Clause 22. This also contains a number of PHY registers that are GPY212 specific. |
| PMAPMD | 1 | Control and status registers related to PMA/PMD signal processing modules. |
| PCS | 3 | Control and status registers related to PCS encoding/decoding device. |
| ANEG | 7 | Control and status registers related to auto-negotiation device. |
| VSPEC1 | 30 | GPY212-specific LED control and GPY212 SGMII control. |
| VSPEC2 | 31 | GPY212-specific Wake-on-LAN control. |

## 4.4 Responsibilities of the STA

The GPY212 responds to all published register addresses for the device and returns a value of zero for undefined and unsupported registers.

As per IEEE 802.3 guidelines, it is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs of the GPY212.

The GPY212 ignores writes to the PMA/PMD speed selection bits that select speeds which are not advertised in the PMA/PMD speed ability register. The PMA/PMD speed selection defaults to a supported ability.

## 4.5 MDIO Access Protocols to Read / Write Registers

All the MDIO/MMD registers can be accessed from an external chip connected to the MDIO bus on the MDIO and MDC pins. The GPY212 supports several MDIO frame protocols:

- Clause 22: To access Device 0
- Clause 22 Extended: To access other devices (Dev 1: PMAPMD, Dev 3: PCS, Dev7: ANEG, Dev 30: VSPEC1, DEV 31: VSPEC2) using the indirection scheme specified by IEEE 802.3.
- Clause 45: to access all devices

Both Clause 22 Extended and Clause 45 can be used to access MMD devices. However, the mechanism implemented in the GPY212 provides faster speeds using Clause 45, so there are some differences in latencies in the MDIO reply:

- Protocol “Clause 22 Extended" involves the GPY212 an indirection mechanism.
- Protocol “Clause 45" provides faster replies.

The Clause 22 registers can be accessed using the Clause 45 electrical interface and the Clause 22 management frame structure [IEEE 802.3 section 45.2].

# 5 MDIO Registers Detailed Description

**Table 17 Register Access Type**

| Mode | Symbol |
|---|---|
| Status Register, (Status, or Ability Register) | RO |
| Read-Write Register, (e.g. MDIO Register) | RW |
| Read-Write, Self-Clearing Register (bit is cleared after read from MDIO) | RWSC |

## 5.1 Standard Management Registers

This section describes the IEEE 802.3 standard management registers corresponding to Clause 22.

**Table 18 Registers Overview**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| STD_CTRL | STD Control (Register 0.0) | $3040_H$ |
| STD_STAT | Status Register (Register 0.1) | $7949_H$ |
| STD_PHYID1 | PHY Identifier 1 (Register 0.2) | $67C9_H$ |
| STD_PHYID2 | PHY Identifier 2 (Register 0.3) | $DC00_H$ 1) |
| STD_AN_ADV | Auto-Negotiation Advertisement (Register 0.4) | $0DE1_H$ |
| STD_AN_LPA | Auto-Negotiation Link Partner Ability (Register 0.5) | $11E0_H$ |
| STD_AN_EXP | Auto-Negotiation Expansion (Register 0.6) | $0064_H$ |
| STD_AN_NPTX | Auto-Negotiation Next Page Transmit Register (Register 0.7) | $2001_H$ |
| STD_AN_NPRX | Auto-Negotiation Link Partner Received Next Page Register (Register 0.8) | $0000_H$ |
| STD_GCTRL | Gigabit Control Register (Register 0.9) | $0200_H$ |
| STD_GSTAT | Gigabit Status Register (Register 0.10) | $0000_H$ |
| STD_MMDCTRL | MMD Access Control Register (Register 0.13) | $0000_H$ |
| STD_MMDDATA | MMD Access Data Register (Register 0.14) | $0000_H$ |
| STD_XSTAT | Extended Status Register (Register 0.15) | $2000_H$ |

1) For the device specific reset value, refer to the Product Naming table in the **Package Outline** chapter.

### 5.1.1 Standard Management Registers

This chapter describes all registers of STD in detail.

**STD Control (Register 0.0)**

This register controls the main functions of the PHY.

IEEE Standard Register=0.0

**STD_CTRL** **Reset Value**

**STD Control (Register 0.0)** **$3040_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 ... 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RST | LB | SSL | ANEN | PD | ISOL | ANRS | DPLX | COL | SSM | RES |
| rwsc | rw | rw | rw | rw | rw | rwsc | rw | rw | rw | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RST | 15 | RWSC | **Reset**<br>Resets the PHY to its default state. Active links are terminated. Note that this is a self-clearing bit which is set to zero by the hardware after reset has been done. See also IEEE 802.3-2008 22.2.4.1.1.<br>$0_B$ **NORMAL** Normal operational mode<br>$1_B$ **RESET** Resets the device |
| LB | 14 | RW | **Loop-Back on GMII**<br>This mode enables looping back of MII data (SGMII) from the transmit to the receive direction. No data is transmitted to the Ethernet PHY.<br>The device operates at the selected speed. The collision signal remains de-asserted unless otherwise forced by the collision test.<br>$0_B$ **NORMAL** Normal operational mode<br>$1_B$ **ENABLE** Closes the loop-back from TX to RX at xMII |
| SSL | 13 | RW | **Forced Speed Selection LSB**<br>This bit only takes effect when the auto-negotiation process is disabled, that is, bit ANEN is set to zero.<br>This is the lower bit (LSB) of the forced speed selection.<br>In conjunction with the higher bit (MSB) , the following encoding is valid:<br>MSB LSB bit values:<br>0 0 = 10 Mbit/s<br>0 1 = 100 Mbit/s<br>1 0 = 1000 Mbit/s<br>1 1 = Reserved, defaults to 2500 Mb/s if the PMA_CTRL register 1.0.5:2 is equal to [0 1 1 0 ]<br>The standard procedure to force the 2500 Mb/s (when ANEG is disabled) is to program PMA_CTRL with 1.0.6 = 1.0.13 = 1 and 1.0.5:2 = [0 1 1 0 ]<br>GPY PHY mirrors 1.0.6, 1.0.13 and 0.0.6 , 0.0.13 |
| ANEN | 12 | RW | **Auto-Negotiation Enable**<br>Allows enabling and disabling of the auto-negotiation process capability of the PHY. If enabled, the force bits for duplex mode (CTRL.DPLX) and the speed selection (CTRL.SSM, CTRL.SSL) become inactive. Otherwise, the force bits define the PHY operation. See also IEEE 802.3-2008 22.2.4.1.4.<br>$0_B$ **DISABLE** Disable the auto-negotiation protocol<br>$1_B$ **ENABLE** Enable the auto-negotiation protocol |
| PD | 11 | RW | **Power Down**<br>Forces the device into a power down state (SLEEP) in which power consumption is the bare minimum required to still maintain the MII management interface communication. When activating the power down functionality, the PHY terminates active data links. The MII interface is also stopped in power down mode. See also IEEE 802.3-2008 22.2.4.1.5.<br>$0_B$ **NORMAL** Normal operational mode<br>$1_B$ **POWERDOWN** Forces the device into power down mode |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| ISOL | 10 | RW | **Isolate**<br>The isolation mode isolates the PHY from the MAC. MAC interface inputs are ignored, whereas MAC interface outputs are set to tristate (high-impedance). See also IEEE 802.3-2008 22.2.4.1.6.<br>$0_B$ **NORMAL** Normal operational mode<br>$1_B$ **ISOLATE** Isolates the PHY from the MAC |
| ANRS | 9 | RWSC | **Restart Auto-Negotiation**<br>Restarts the auto-negotiation process on the MDI. This bit does not take any effect when auto-negotiation is disabled using (CTRL.ANEN). Note that this bit is self-clearing after the auto-negotiation process is initiated. See also IEEE 802.3-2008 22.2.4.1.7.<br>$0_B$ **NORMAL** Stay in current mode<br>$1_B$ **RESTART** Restart auto-negotiation |
| DPLX | 8 | RW | **Forced Duplex Mode**<br>Note that this bit only takes effect when the auto-negotiation process is disabled, that is, bit CTRL.ANEN is set to zero. This bit controls the forced duplex mode. It allows forcing of the PHY into full or half-duplex mode. Note that this bit does not take effect in loop-back mode, that is, when bit CTRL.LB is set to "1". See also IEEE 802.3-2008 22.2.4.1.8.<br>The Duplex mode can only be forced to Half Duplex in 10BT and 100BT speed modes. This field is ignored for higher speeds.<br>$0_B$ **HD** Half duplex<br>$1_B$ **FD** Full duplex |
| COL | 7 | RW | **Collision Test**<br>Allows testing of the COL signal at the xMII interface. When the collision test is enabled, the state of the TX_EN signal is looped back to the COL signal within a minimum latency.<br>See also IEEE 802.3-2008 22.2.4.1.9.<br>$0_B$ **DISABLE** Normal operational mode<br>$1_B$ **ENABLE** Activates the collision test |
| SSM | 6 | RW | **Forced Speed Selection MSB**<br>This bit only takes effect when the auto-negotiation process is disabled, that is, bit ANEN is set to zero.<br>This is the most significant bit (MSB) of the forced speed selection.<br>In conjunction with the lower bit, (LSB), the following encoding is valid:<br>MSB LSB:<br>0 0 = 10 Mbit/s<br>0 1 = 100 Mbit/s<br>1 0 = 1000 Mbit/s<br>1 1 = Reserved, defaults to 2500 Mb/s if the PMA_CTRL (1.0.5:2 = [0 1 1 0 ] )<br>The preferred way to force the 2500 Mb/s (when ANEG is disabled) is to program PMA_CTRL with 1.0.6 = 1.0.13 = 1 and 1.0.5:2 = [0 1 1 0 ]<br>GPY mirrors 1.06, 1.0.13 and 0.0.6 , 0.0.13 |
| RES | 5:0 | RO | **Reserved**<br>Write as zero, ignore on read. |

**Status Register (Register 0.1)**

This register contains status and capability information about the device. Note that all bits are read-only. A write access by the MAC does not have any effect. See also IEEE 802.3-2008 22.2.4.2.

IEEE Standard Register=0.1

**STD_STAT** — **Reset Value**

**Status Register (Register 0.1)** — **$7949_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CBT4** | **CBTXF** | **CBTXH** | **XBTF** | **XBTH** | **CBT2F** | **CBT2H** | **EXT** | **RES** | **MFPS** | **ANOK** | **RF** | **ANAB** | **LS** | **JD** | **XCAP** |
| ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | rolh | ro | roll | rolh | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| CBT4 | 15 | RO | **IEEE 100BASE-T4**<br>Specifies the 100BASE-T4 ability.<br>$0_B$ **DISABLED** PHY does not support this mode<br>$1_B$ **ENABLED** PHY supports this mode |
| CBTXF | 14 | RO | **IEEE 100BASE-TX Full-Duplex**<br>Specifies the 100BASE-TX full-duplex ability.<br>$0_B$ **DISABLED** PHY does not support this mode<br>$1_B$ **ENABLED** PHY supports this mode |
| CBTXH | 13 | RO | **IEEE 100BASE-TX Half-Duplex**<br>Specifies the 100BASE-TX half-duplex ability.<br>$0_B$ **DISABLED** PHY does not support this mode<br>$1_B$ **ENABLED** PHY supports this mode |
| XBTF | 12 | RO | **IEEE 10BASE-T Full-Duplex**<br>Specifies the 10 BASE-T full-duplex ability.<br>$0_B$ **DISABLED** PHY does not support this mode<br>$1_B$ **ENABLED** PHY supports this mode |
| XBTH | 11 | RO | **IEEE 10BASE-T Half-Duplex**<br>Specifies the 10BASE-T half-duplex ability.<br>$0_B$ **DISABLED** PHY does not support this mode<br>$1_B$ **ENABLED** PHY supports this mode |
| CBT2F | 10 | RO | **IEEE 100BASE-T2 Full-Duplex**<br>Specifies the 100BASE-T2 full-duplex ability.<br>$0_B$ **DISABLED** PHY does not support this mode<br>$1_B$ **ENABLED** PHY supports this mode |
| CBT2H | 9 | RO | **IEEE 100BASE-T2 Half-Duplex**<br>Specifies the 100BASE-T2 half-duplex ability.<br>$0_B$ **DISABLED** PHY does not support this mode<br>$1_B$ **ENABLED** PHY supports this mode |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| EXT | 8 | RO | **Extended Status**<br>The extended status registers are used to specify 1000 Mbit/s speed capabilities in the register XSTAT. See also IEEE 802.3-2008 Clause 22.2.4.2.16.<br>$0_B$ **DISABLED** No extended status information available in register 15<br>$1_B$ **ENABLED** Extended status information available in register 15 |
| RES | 7 | RO | **Reserved**<br>Ignore when read. |
| MFPS | 6 | RO | **Management Preamble Suppression**<br>Specifies the MF preamble suppression ability. See also IEEE 802.3-2008 22.2.4.2.9.<br>$0_B$ **DISABLED** PHY requires management frames with preamble<br>$1_B$ **ENABLED** PHY accepts management frames without preamble |
| ANOK | 5 | RO | **Auto-Negotiation Completed**<br>Indicates whether the auto-negotiation process is completed or in progress. See also IEEE 802.3-2008 22.2.4.2.10.<br>$0_B$ **RUNNING** Auto-negotiation process is in progress<br>$1_B$ **COMPLETED** Auto-negotiation process is completed |
| RF | 4 | ROLH | **Remote Fault**<br>Indicates the detection of a remote fault event. See also IEEE 802.3-2008 22.2.4.2.11.<br>$0_B$ **INACTIVE** No remote fault condition detected<br>$1_B$ **ACTIVE** Remote fault condition detected |
| ANAB | 3 | RO | **Auto-Negotiation Ability**<br>Specifies the auto-negotiation ability. See also IEEE 802.3-2008 22.2.4.2.12.<br>$0_B$ **DISABLED** PHY is not able to perform auto-negotiation<br>$1_B$ **ENABLED** PHY is able to perform auto-negotiation |
| LS | 2 | ROLL | **Link Status**<br>Indicates the link status of the PHY to the link partner. See also IEEE 802.3-2008 22.2.4.2.13.<br>$0_B$ **INACTIVE** The link is down. No communication with link partner possible.<br>$1_B$ **ACTIVE** The link is up. Data communication with link partner is possible. |
| JD | 1 | ROLH | **Jabber Detect**<br>Indicates that a jabber event has been detected. See also IEEE 802.3-2008 22.2.4.2.14.<br>$0_B$ **NONE** No jabber condition detected<br>$1_B$ **DETECTED** Jabber condition detected |
| XCAP | 0 | RO | **Extended Capability**<br>Indicates the availability and support of extended capability registers. See also IEEE 802.3-2008 22.2.4.2.15.<br>$0_B$ **DISABLED** Only base registers are supported<br>$1_B$ **ENABLED** Extended capability registers are supported |

**PHY Identifier 1 (Register 0.2)**

This code specifies the Organizationally Unique Identifier (OUI), and the vendor's model and revision number.

IEEE Standard Register=0.2

**STD_PHYID1** — Reset Value

**PHY Identifier 1 (Register 0.2)** — $67C9_H$

| 15 … 0 |
|---|
| **OUI** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | **Organizationally Unique Identifier Bits 3:18** |

**PHY Identifier 2 (Register 0.3)**

IEEE Standard Register=0.3

**STD_PHYID2** — Reset Value

**PHY Identifier 2 (Register 0.3)** — $DC00_H$

| 15 … 10 | 9 … 4 | 3 … 0 |
|---|---|---|
| **OUI** | **LDN** | **LDRN** |
| ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier Bits 19:24** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1)] to distinguish between several products. |
| LDRN | 3:0 | RO | **Device Number**<br>Specifies the device revision number[1)] to distinguish between several versions of this device. |

1) For the device specific reset value, refer to Product Naming table in the **Package Outline** chapter.

**Auto-Negotiation Advertisement (Register 0.4)**

This register contains the advertised abilities of the PHY during auto-negotiation.

IEEE Standard Register=0.4

**STD_AN_ADV** **Reset Value**

**Auto-Negotiation Advertisement (Register 0.4)** **$0DE1_H$**

| 15 | 14 | 13 | 12 | 11:5 | 4:0 |
|---|---|---|---|---|---|
| **NP** | **RES** | **RF** | **XNP** | **TAF** | **SF** |
| rw | ro | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RW | **Next Page**<br>Next page indication is encoded in bit AN_ADV.NP regardless of the selector field value or link code word encoding. The PHY always advertises NP if a 1000BASE-T mode is advertised during auto-negotiation. See also IEEE 802.3-2008 28.2.1.2.6.<br>$0_B$ **INACTIVE** No next page(s) will follow<br>$1_B$ **ACTIVE** Additional next page(s) will follow |
| RES | 14 | RO | **Reserved**<br>Write as zero, ignore on read. |
| RF | 13 | RW | **Remote Fault**<br>The remote fault bit allows indication of a fault to the link partner. See also IEEE 802.3-2008 28.2.1.2.4.<br>$0_B$ **NONE** No remote fault is indicated<br>$1_B$ **FAULT** A remote fault is indicated |
| XNP | 12 | RW | **Extended Next Page**<br>Indicates that GPY supports transmission of Extended Next Pages (XNP).<br>$0_B$ **UNABLE** GPY is XNP unable<br>$1_B$ **ABLE** GPY is XNP able |
| TAF | 11:5 | RW | **Technology Ability Field**<br>The technology ability field is an 8-bit wide field containing information indicating supported technologies. GPY supports 10BASE-T (Half and Full Duplex), 100BASE-TX (Half and Full Duplex) and both symmetric and asymmetric PAUSE.<br>$40_H$ **PS_ASYM** Advertise asymmetric pause<br>$20_H$ **PS_SYM** Advertise symmetric pause<br>$10_H$ **DBT4** Advertise 100BASE-T4<br>$08_H$ **DBT_FDX** Advertise 100BASE-TX full duplex<br>$04_H$ **DBT_HDX** Advertise 100BASE-TX half duplex<br>$02_H$ **XBT_FDX** Advertise 10BASE-T full duplex<br>$01_H$ **XBT_HDX** Advertise 10BASE-T half duplex |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| SF | 4:0 | RW | **Selector Field**<br>The selector field is a 5-bit wide field for encoding 32 possible messages. Selector field encoding definitions are shown in IEEE 802.3-2008 Annex 28A. Combinations not specified are reserved for future use. Reserved combinations of the selector field are not to be transmitted. See also IEEE 802.3-2008 28.2.1.2.1.<br>$00001_B$ **IEEE802DOT3** Select the IEEE 802.3 technology |

**Auto-Negotiation Link Partner Ability (Register 0.5)**

IEEE Standard Register=0.5

When the auto-negotiation is complete, this register contains the advertised ability of the link partner. The bit definitions are a direct representation of the received link code word .

**STD_AN_LPA** **Reset Value**
**Auto-Negotiation Link Partner Ability (Register 0.5)** **$11E0_H$**

| 15 | 14 | 13 | 12 | 11 ... 5 | 4 ... 0 |
|---|---|---|---|---|---|
| **NP** | **ACK** | **RF** | **XNP** | **TAF** | **SF** |
| ro | ro | ro | rw | rw | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RO | **Next Page**<br>Next page request indication from the link partner. See also IEEE 802.3-2008 28.2.1.2.6.<br>$0_B$ **INACTIVE** No next page(s) will follow<br>$1_B$ **ACTIVE** Additional next pages will follow |
| ACK | 14 | RO | **Acknowledge**<br>Acknowledgement indication from the link partner's link code word. See also IEEE 802.3-2008 28.2.1.2.5.<br>$0_B$ **INACTIVE** The device did not successfully receive its link partner's link code word<br>$1_B$ **ACTIVE** The device has successfully received its link partner's link code word |
| RF | 13 | RO | **Remote Fault**<br>Remote fault indication from the link partner. See also IEEE 802.3-2008 28.2.1.2.4.<br>$0_B$ **NONE** Remote fault is not indicated by the link partner<br>$1_B$ **FAULT** Remote fault is indicated by the link partner |
| XNP | 12 | RW | **Extended Next Page**<br>Indicates that GPY supports transmission of Extended Next Pages (XNP).<br>$0_B$ **UNABLE** Link partner is XNP unable<br>$1_B$ **ABLE** Link partner is XNP able |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| TAF | 11:5 | RW | **Technology Ability Field**<br>$40_H$ **PS_ASYM** Advertise asymmetric pause<br>$20_H$ **PS_SYM** Advertise symmetric pause<br>$10_H$ **DBT4** Advertise 100BASE-T4<br>$08_H$ **DBT_FDX** Advertise 100BASE-TX full duplex<br>$04_H$ **DBT_HDX** Advertise 100BASE-TX half duplex<br>$02_H$ **XBT_FDX** Advertise 10BASE-T full duplex<br>$01_H$ **XBT_HDX** Advertise 10BASE-T half duplex |
| SF | 4:0 | RO | **Selector Field**<br>$00001_B$**IEEE802DOT3** Select the IEEE 802.3 technology |

**Auto-Negotiation Expansion (Register 0.6)**

This is the auto-negotiation expansion register indicating the status of the link partner's auto-negotiation. This register is valid only after the auto-negotiation is completed.

See also IEEE 802.3 28.2.4.1.5.

IEEE Standard Register=0.6

**STD_AN_EXP** — **Reset Value**

**Auto-Negotiation Expansion (Register 0.6)** — **$0064_H$**

| 15 … 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **RES** | **RNPLA** | **RNPSL** | **PDF** | **LPNPC** | **NPC** | **PR** | **LPANC** |
| ro | ro | ro | rolh | ro | ro | rolh | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:7 | RO | **Reserved**<br>Write as zero, ignore on read. |
| RNPLA | 6 | RO | **Receive Next Page Location Able**<br>Per 802.3 - 2015, indicate that the Rx NP location is indicated by field RNPSL<br>$0_B$ **UNABLE** Received Next Page storage location is not specified by bit (6.5)<br>$1_B$ **ABLE** Received Next Page storage location is specified by bit (6.5) |
| RNPSL | 5 | RO | **Receive Next Page Storage Location**<br>Per 802.3 - 2015, indicate that Rx NP is in register 0.8 for GPY<br>$0_B$ **FIVE** Link partner Next Pages are stored in Register 5<br>$1_B$ **EIGHT** Link partner Next Pages are stored in Register 8 |
| PDF | 4 | ROLH | **Parallel Detection Fault**<br>$0_B$ **NONE** A fault has not been detected via the parallel detection function<br>$1_B$ **FAULT** A fault has been detected via the parallel detection function |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| LPNPC | 3 | RO | **Link Partner Next Page Capable**<br>$0_B$ **UNABLE** Link partner is unable to exchange next pages<br>$1_B$ **CAPABLE** Link partner is capable of exchanging next pages |
| NPC | 2 | RO | **Next Page Capable**<br>$0_B$ **UNABLE** GPY is unable to exchange next pages<br>$1_B$ **CAPABLE** GPY is capable of exchanging next pages |
| PR | 1 | ROLH | **Page Received**<br>$0_B$ **NONE** A new page has not been received<br>$1_B$ **RECEIVED** A new page has been received |
| LPANC | 0 | RO | **Link Partner Auto-Negotiation Capable**<br>$0_B$ **UNABLE** Link partner is unable to auto-negotiate<br>$1_B$ **CAPABLE** Link partner is auto-negotiation capable |

**Auto-Negotiation Next Page Transmit Register (Register 0.7)**

The auto-negotiation next page transmit register contains the next page link code word to be transmitted when next page ability is supported. See also IEEE 802.3 28.2.4.1.6.

IEEE Standard Register=0.7

**STD_AN_NPTX** **Reset Value**
**Auto-Negotiation Next Page Transmit Register (Register 0.7)** **$2001_H$**

| 15 | 14 | 13 | 12 | 11 | 10 ... 0 |
|---|---|---|---|---|---|
| NP | RES | MP | ACK2 | TOGG | MCF |
| rw | ro | rw | rw | ro | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RW | **Next Page**<br>$0_B$ **INACTIVE** Last page<br>$1_B$ **ACTIVE** Additional next page(s) will follow |
| RES | 14 | RO | **Reserved**<br>Write as zeroes, ignore on read. |
| MP | 13 | RW | **Message Page**<br>Indicates that the content of MCF is either an unformatted page or a formatted message.<br>$0_B$ **UNFOR** Unformatted page<br>$1_B$ **MESSG** Message page |
| ACK2 | 12 | RW | **Acknowledge 2**<br>$0_B$ **INACTIVE** Device cannot comply with message<br>$1_B$ **ACTIVE** Device will comply with message |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| TOGG | 11 | RO | **Toggle**<br>This bit always takes the opposite value of the Toggle bit in the previously exchanged link code word.<br>See also IEEE 802.3-2008 28.2.3.4.<br>$0_B$ **ZERO** Previous value of the transmitted link code word was ONE<br>$1_B$ **ONE** Previous value of the transmitted link code word was ZERO |
| MCF | 10:0 | RW | **Message or Unformatted Code Field**<br>When Message Page bit is set to 1 (0.7.13), this field is the Message Code Field of a message page used in Next Page exchange. The message codes are described in IEEE802.3 Appendix 28C.<br>It is used to indicate the type of message in UCF1 and UCF2.<br>0x0 = Reserved<br>0x1 = Null message<br>0x2 = One Unformated Page (UP) with TAF follows<br>0x3 = Two UPs with TAF follows<br>0x4 = Remote fault details message<br>0x5 = OUI message<br>0x6 = PHY ID message<br>0x7 = 100BASE-T2 message<br>0x8 = 1000BASE-T message<br>0x9 = MULTIGBASE-T message<br>0xA = EEE technology capability follows in next UP<br>0xB = OUI XNP |

**Auto-Negotiation Link Partner Received Next Page Register (Register 0.8)**

The auto-negotiation link partner received next page register contains the next page link code word received from the link partner. See also IEEE 802.3-2008 28.2.4.1.7.

IEEE Standard Register=0.8

**STD_AN_NPRX** — **Reset Value** $0000_H$

**Auto-Negotiation Link Partner Received Next Page Register (Register 0.8)**

| 15 | 14 | 13 | 12 | 11 | 10 … 0 |
|---|---|---|---|---|---|
| **NP** | **ACK** | **MP** | **ACK2** | **TOGG** | **MCF** |
| ro | ro | ro | ro | ro | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RO | **Next Page**<br>See IEEE 802.3-2008 28.2.3.4.<br>$0_B$ **INACTIVE** No next pages to follow<br>$1_B$ **ACTIVE** Additional next page(s) will follow |

| Field | Bits | Type | **Description** (cont'd) |
|---|---|---|---|
| ACK | 14 | RO | **Acknowledge**<br>See also IEEE 802.3-2008 28.2.3.4.<br>$0_B$ **INACTIVE** The device did not successfully receive its link partner's link code word<br>$1_B$ **ACTIVE** The device has successfully received its link partner's link code word |
| MP | 13 | RO | **Message Page**<br>Indicates that the content of MCF is either an unformatted page or a formatted message. See also IEEE 802.3-2008 28.2.3.4.<br>$0_B$ **UNFOR** Unformatted page<br>$1_B$ **MESSG** Message page |
| ACK2 | 12 | RO | **Acknowledge 2**<br>See also IEEE 802.3-2008 28.2.3.4.<br>$0_B$ **INACTIVE** Device cannot comply with message<br>$1_B$ **ACTIVE** Device will comply with message |
| TOGG | 11 | RO | **Toggle**<br>This bit always takes the opposite value of the Toggle bit in the previously exchanged link code word.<br>See also IEEE 802.3-2008 28.2.3.4.<br>$0_B$ **ZERO** Previous value of the transmitted link code word was equal to ONE<br>$1_B$ **ONE** Previous value of the transmitted link code word was equal to ZERO |
| MCF | 10:0 | RW | **Message or Unformatted Code Field**<br>This field is the Message Code Field of a message page used in Next Page exchange.<br>The message codes are described in IEEE802.3 Appendix 28C.<br>It is used to indicate the type of message in UCF1 and UCF2.<br>0x0 = Reserved<br>0x1 = Null message<br>0x2 = One Unformated Page (UP) with TAF follows<br>0x3 = Two UPs with TAF follows<br>0x4 = Remote fault details message<br>0x5 = OUI message<br>0x6 = PHY ID message<br>0x7 = 100BASE-T2 message<br>0x8 = 1000BASE-T message<br>0x9 = MULTIGBASE-T message<br>0xA = EEE technology capability follows in next UP<br>0xB = OUI XNP |

**Gigabit Control Register (Register 0.9)**

This is the control register used to configure the Gigabit Ethernet behavior of the PHY. See also IEEE 802.3-2008 40.5.1.1.

IEEE Standard Register=0.9

**STD_GCTRL** — **Reset Value**

**Gigabit Control Register (Register 0.9)** — **$0200_H$**

| 15–13 | 12 | 11 | 10 | 9 | 8 | 7–0 |
|---|---|---|---|---|---|---|
| **TM** | **MSEN** | **MS** | **MSPT** | **MBTFD** | **MBTHD** | **RES** |
| rw | rw | rw | rw | rw | rw | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| TM | 15:13 | RW | **Transmitter Test Mode**<br>This register field allows enabling of the standard transmitter test modes. See also IEEE 802.3-2008 Table 40-7.<br>$000_B$ **NOP** Normal operation<br>$001_B$ **WAV** Test mode 1 transmit waveform test<br>$010_B$ **JITM** Test mode 2 transmit jitter test in MASTER mode<br>$011_B$ **JITS** Test mode 3 transmit jitter test in SLAVE mode<br>$100_B$ **DIST** Test mode 4 transmitter distortion test |
| MSEN | 12 | RW | **Master/Slave Manual Configuration Enable**<br>See also IEEE 802.3-2008 40.5.1.1.<br>$0_B$ **DISABLED** Disable master/slave manual configuration value<br>$1_B$ **ENABLED** Enable master/slave manual configuration value |
| MS | 11 | RW | **Master/Slave Config Value**<br>Allows forcing of master or slave mode manually when AN_GCTRL.MSEN is set to logical one. See also IEEE 802.3-2008 40.5.1.1.<br>$0_B$ **SLAVE** Configure PHY as SLAVE during master/slave negotiation<br>$1_B$ **MASTER** Configure PHY as MASTER during master/slave negotiation |
| MSPT | 10 | RW | **Master/Slave Port Type**<br>Defines whether the PHY advertises itself as a multi- or single-port device, which in turn impacts the master/slave resolution function. See also IEEE 802.3-2008 40.5.1.1.<br>$0_B$ **SPD** Single-port device<br>$1_B$ **MPD** Multi-port device |
| MBTFD | 9 | RW | **1000BASE-T Full-Duplex**<br>Advertises the 1000BASE-T full-duplex capability; always forced to 1 in converter mode. See also IEEE 802.3-2008 40.5.1.1.<br>$0_B$ **DISABLED** Advertise PHY as not 1000BASE-T full-duplex capable<br>$1_B$ **ENABLED** Advertise PHY as 1000BASE-T full-duplex capable |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| MBTHD | 8 | RW | **1000BASE-T Half-Duplex**<br>Always advertises the 1000BASE-T half-duplex capability as disabled; GPY do not support 1000BASE-T Half-Duplex capability<br>$0_B$ **DISABLED** Advertise PHY as not 1000BASE-T half-duplex capable<br>$1_B$ **ENABLED** Advertise PHY as 1000BASE-T half-duplex capable |
| RES | 7:0 | RO | **Reserved**<br>Write as zero, ignore on read. |

**Gigabit Status Register (Register 0.10)**

This is the status register used to reflect the Gigabit Ethernet status of the PHY. See also IEEE 802.3-2008 40.5.1.1.

IEEE Standard Register=0.10

**STD_GSTAT** **Reset Value**

**Gigabit Status Register (Register 0.10)** **$0000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 8 | 7 ... 0 |
|---|---|---|---|---|---|---|---|
| **MSFAULT** | **MSRES** | **LRXSTAT** | **RRXSTAT** | **MBTFD** | **MBTHD** | **RES** | **IEC** |
| rwsc | ro | ro | ro | ro | ro | ro | rwsc |

| Field | Bits | Type | Description |
|---|---|---|---|
| MSFAULT | 15 | RWSC | **Master/Slave Manual Configuration Fault**<br>This bit will is set if the number of failed MASTER-SLAVE resolutions reaches 7<br>It is cleared upon each read of GSTAT.<br>This bit self clears on auto-negotiation enable or auto-negotiation complete.<br>$0_B$ **OK** Master/slave manual configuration resolved successfully<br>$1_B$ **NOK** Master/slave manual configuration resolved with a fault |
| MSRES | 14 | RO | **Master/Slave Configuration Resolution**<br>$0_B$ **SLAVE** Local PHY configuration resolved to SLAVE<br>$1_B$ **MASTER** Local PHY configuration resolved to MASTER |
| LRXSTAT | 13 | RO | **Local Receiver Status**<br>Indicates the status of the local receiver. See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3.<br>$0_B$ **NOK** Local receiver not OK<br>$1_B$ **OK** Local receiver OK |
| RRXSTAT | 12 | RO | **Remote Receiver Status**<br>Indicates the status of the remote receiver. See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3.<br>$0_B$ **NOK** Remote receiver not OK<br>$1_B$ **OK** Remote receiver OK |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| MBTFD | 11 | RO | **Link Partner Capable of Operating 1000BASE-T Full-Duplex**<br>See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3.<br>$0_B$ **DISABLED** Link partner is not capable of operating 1000BASE-T full-duplex<br>$1_B$ **ENABLED** Link partner is capable of operating 1000BASE-T full-duplex |
| MBTHD | 10 | RO | **Link Partner Capable of Operating 1000BASE-T Half-Duplex**<br>See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3.<br>$0_B$ **DISABLED** Link partner is not capable of operating 1000BASE-T half-duplex<br>$1_B$ **ENABLED** Link partner is capable of operating 1000BASE-T half-duplex |
| RES | 9:8 | RO | **Reserved**<br>Write as zero, ignore on read. |
| IEC | 7:0 | RWSC | **Idle Error Count**<br>Indicates the idle error count. This field contains a cumulative count of the errors detected when the receiver is receiving idles . |

**MMD Access Control Register (Register 0.13)**

The MMD access control register is used in conjunction with the MMDDATA register to access the MMD register space. This uses address directing as specified in IEEE802.3 Clause 22 Extended.

IEEE Standard Register=0.13

**STD_MMDCTRL** **Reset Value**
**MMD Access Control Register (Register 0.13)** **$0000_H$**

| 15 14 | 13 8 | 7 5 | 4 0 |
|---|---|---|---|
| ACTYPE | RESH | RESL | DEVAD |
| rw | ro | ro | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| ACTYPE | 15:14 | RW | **Access Type Function**<br>If the access of register MMDDATA is an address access (ACTYPE=0) then it is directed to the address register within the MMD associated with the value in the DEVAD field. Otherwise, both the DEVAD field and the MMD's address register direct the register MMDDATA data accesses to the appropriate registers within that MMD.<br>$00_B$ **ADDRESS** Accesses to register MMDDATA access the MMD individual address register<br>$01_B$ **DATA** Accesses to register MMDDATA access the register within the MMD selected<br>$10_B$ **DATA_PI** Accesses to register MMDDATA access the register within the MMD selected<br>$11_B$ **DATA_PIWR** Accesses to register MMDDATA access the register within the MMD selected |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| RESH | 13:8 | RO | **Reserved**<br>Write as zero, ignored on read. |
| RESL | 7:5 | RO | **Reserved**<br>Write as zero, ignored on read. |
| DEVAD | 4:0 | RW | **Device Address**<br>The DEVAD field directs any accesses of register MMDDATA to the appropriate MMD as described in IEEE 802.3-2008 Clause 45.2. |

**MMD Access Data Register (Register 0.14)**

The MMD access data register is used in conjunction with the MMD access control (MMDCTRL) register to access the MMD register space. For more information on MMD access, refer to IEEE 802.3-2008 Clause 22.2.4.3.12, Clause 45.2 and Annex 22D.

IEEE Standard Register=0.14

**STD_MMDDATA** — **Reset Value**
**MMD Access Data Register (Register 0.14)** — **$0000_H$**

| 15 … 0 |
|---|
| **ADDR_DATA** |
| rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| ADDR_DATA | 15:0 | RW | **Address or Data Register**<br>This register accesses either a specific MMD address register or the data content of the MMD register to which this address register points. Which of the functions is currently valid is defined by the MMDCTRL register. |

**Extended Status Register (Register 0.15)**

This register contains extended status and capability information about the PHY. Note that all bits are read-only. A write access does not have any effect.

IEEE Standard Register=0.15

**STD_XSTAT** — **Reset Value**
**Extended Status Register (Register 0.15)** — **$2000_H$**

| 15 | 14 | 13 | 12 | 11 … 8 | 7 … 0 |
|---|---|---|---|---|---|
| **MBXF** | **MBXH** | **MBTF** | **MBTH** | **RESH** | **RESL** |
| ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| MBXF | 15 | RO | **1000BASE-X Full-Duplex Capability**<br>Specifies whether the PHY is capable of operating 1000BASE-X full-duplex.<br>$0_B$ **DISABLED** PHY does not support this mode<br>$1_B$ **ENABLED** PHY supports this mode |
| MBXH | 14 | RO | **1000BASE-X Half-Duplex Capability**<br>Specifies whether the PHY is capable of operating 1000BASE-X half-duplex.<br>$0_B$ **DISABLED** PHY does not support this mode<br>$1_B$ **ENABLED** PHY supports this mode |
| MBTF | 13 | RO | **1000BASE-T Full-Duplex Capability**<br>Specifies whether the PHY is capable of operating 1000BASE-T full-duplex.<br>$0_B$ **DISABLED** PHY does not support this mode<br>$1_B$ **ENABLED** PHY supports this mode |
| MBTH | 12 | RO | **1000BASE-T Half-Duplex Capability**<br>GPY do not support 1000BASE-T Half-Duplex capability.<br>$0_B$ **DISABLED** PHY does not support this mode<br>$1_B$ **ENABLED** PHY supports this mode |
| RESH | 11:8 | RO | **Reserved**<br>Ignore when read. |
| RESL | 7:0 | RO | **Reserved**<br>Ignore when read. |

## 5.2 GPY-specific Management Registers

This section describes the GPY specific management registers in device 0.

**Table 19 Registers Overview**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| **PHY_STAT1** | Physical Layer Status 1 (Register 0.17) | $0000_H$ |
| **PHY_CTL1** | Physical Layer Control 1 (Register 0.19) | $0001_H$ |
| **PHY_CTL2** | Physical Layer Control 2 (Register 0.20) | $0006_H$ |
| **PHY_ERRCNT** | Error Counter (Register 0.21) | $0000_H$ |
| **PHY_MIISTAT** | Media-Independent Interface Status (Register 0.24) | $0000_H$ |
| **PHY_IMASK** | Interrupt Mask Register (Register 0.25) | $0000_H$ |
| **PHY_ISTAT** | Interrupt Status Register (Register 0.26) | $0000_H$ |
| **PHY_LED** | LED Control Register (Register 0.27) | $FF00_H$ |
| **PHY_FWV** | Firmware Version Register (Register 0.30) | $0000_H$ |

### 5.2.1 GPY-specific Management Registers

This chapter describes all registers of PHY in detail.

**Physical Layer Status 1 (Register 0.17)**

This register reports PHY link information, for example link-up, polarity reversals and port mapping. The content of this register is only valid when the link is up.

IEEE Standard Register=0.17

**PHY_STAT1** **Reset Value**
**Physical Layer Status 1 (Register 0.17)** **$0000_H$**

| 15 … 9 | 8 | 7 … 4 | 3 … 2 | 1 … 0 |
|---|---|---|---|---|
| **RES2** | **LSADS** | **Res** | **FW_MEM** | **RES1** |
| ro | rosc | | rw | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES2 | 15:9 | RO | **Reserved**<br>Write as zero, ignored on read. |
| LSADS | 8 | ROSC | **Link Speed Auto-Downspeed Status**<br>Monitors the status of the auto-downspeed.<br>$0_B$ **NORMAL** Did not perform any link speed auto-downspeed<br>$1_B$ **DETECTED** Detected an auto-downspeed |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| FW_MEM | 3:2 | RW | **Firmware Memory Location**<br>Indicate memory target used for firmware execution<br>$00_B$ **ROM** Firmware is executed from ROM<br>$01_B$ **OTP** Firmware is executed from OTP<br>$10_B$ **FLASH** Firmware is executed from FLASH<br>$11_B$ **RAM** Firmware is executed from SRAM |
| RES1 | 1:0 | RO | **Reserved**<br>Write as zero, ignored on read. |

**Physical Layer Control 1 (Register 0.19)**

This register controls the PHY functions.

IEEE Standard Register=0.19

**PHY_CTL1** **Reset Value**
**Physical Layer Control 1 (Register 0.19)** **$0001_H$**

| 15–13 | 12 | 11–8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| TLOOP | Res | TXADJ | POLD | POLC | POLB | POLA | MDICD | MDIAB | RES | AMDIX |
| rw | | rw | rw | rw | rw | rw | rw | rw | ro | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| TLOOP | 15:13 | RW | **Test Loop**<br>Configures predefined test loops.<br>$000_B$ **OFF** Test loops are switched off - normal operation.<br>$001_B$ **NETL** Near-end test loop<br>$010_B$ Far-end test loop<br>**Others:** Reserved |
| TXADJ | 11:8 | RW | **Transmit Level Adjustment**<br>Transmit-level adjustment is used to fine tune the transmit amplitude of the PHY. The amplitude adjustment is valid for all supported speed modes. The adjustment is performed in digits. One digit represents 3.125 percent of the nominal amplitude. The scaling factor is gain = 1 + signed(TXADJ)*2^-7. |
| POLD | 7 | RW | **Polarity Inversion Control on Port D**<br>$0_B$ **NORMAL** Polarity normal<br>$1_B$ **INVERTED** Polarity inversion |
| POLC | 6 | RW | **Polarity Inversion Control on Port C**<br>$0_B$ **NORMAL** Polarity normal<br>$1_B$ **INVERTED** Polarity inversion |
| POLB | 5 | RW | **Polarity Inversion Control on Port B**<br>$0_B$ **NORMAL** Polarity normal<br>$1_B$ **INVERTED** Polarity inversion |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| POLA | 4 | RW | **Polarity Inversion Control on Port A**<br>$0_B$ **NORMAL** Polarity normal<br>$1_B$ **INVERTED** Polarity inversion |
| MDICD | 3 | RW | **Mapping of MDI Ports C and D**<br>Used when Auto-MDIX is OFF, to force the MDIX cable crossover configuration<br>$0_B$ **MDI** Normal MDI mode<br>$1_B$ **MDIX** Crossover MDI-X mode |
| MDIAB | 2 | RW | **Mapping of MDI Ports A and B**<br>Used when Auto-MDIX is OFF, to force the MDIX cable crossover configuration<br>$0_B$ **MDI** Normal MDI mode<br>$1_B$ **MDIX** Crossover MDI-X mode |
| RES | 1 | RO | **Reserved** |
| AMDIX | 0 | RW | **PHY Performs Auto-MDI/MDI-X or Uses Manual MDI/MDI-X**<br>$0_B$ **MANUAL** PHY uses manual MDI/MDI-X<br>$1_B$ **AUTO** PHY performs Auto-MDI/MDI-X |

**Physical Layer Control 2 (Register 0.20)**

This register controls the PHY functions.

IEEE Standard Register=0.20

**PHY_CTL2** **Reset Value**
**Physical Layer Control 2 (Register 0.20)** **$0006_H$**

| 15–10 | 9 | 8 | 7–5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Res** | **SDETP** | **STICKY** | **RES1** | **ULP_STA*** | **ULP** | **PSCL** | **ANPD** | **LPI** |
| | rw | rw | ro | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| SDETP | 9 | RW | **Signal Detection Polarity for the 1000BASE-X PHY**<br>Allows specification of the signal detection polarity of the SIGDET input. Although this bit is reset to 0, its actual value depends on the pin-strapping configuration if no EEPROM is detected.<br>$0_B$ **LOWACTIVE** SIGDET input is low active<br>$1_B$ **HIGHACTIVE** SIGDET input is high active |
| STICKY | 8 | RW | **Sticky-Bit Handling**<br>Setting this bit to 1 ensures that all the vendor specific registers (of type RW) in PHY ( device 0 ), VSPEC1 ( device 30) and VSPEC2 ( device 31) are not changed during a MDIO reset or software reset of GPY. This allows the STA to keep the configurations chosen before reset.<br>$0_B$ **OFF** Sticky-bit handling is disabled<br>$1_B$ **ON** Sticky-bit handling is enabled |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| RES1 | 7:5 | RO | **Reserved**<br>Write as zero, ignored on read. |
| ULP_STA_BLOCK | 4 | RW | **Ultra Low Power Mode entry block by acknowledgment from STA**<br>Ultra Low Power Mode entry block by acknowledgment from STA<br>When PHY_IMASK.ULP = ACTIVE, intent to ULP entry is indicated to STA. For the GPY to enter unconditionally without acknowledgement from STA, set PHY_CTL2.ULP_STA_BLOCK = OFF.<br>For blocking ULP entry till the acknowledgement is received from STA, set PHY_CTL2.ULP_STA_BLOCK = ON.<br>This bit has no effect when PHY_IMASK.ULP = INACTIVE.<br>$0_B$ **OFF** ULP Entry without the role of STAGPY will enter ULP unconditionally without acknowledgement from STA<br>$1_B$ **ON** ULP Entry Blocked by STAGPY will enter ULP only after STA reads the ULP interrupt status register PHY_ISTAT |
| ULP | 3 | RW | **Ultra Low Power Mode**<br>Ultra Low Power Mode ( ULP ) allows GPY to save energy by disabling most of the digital logic to reduce power consumption to its lowest level. The entry to ULP is triggered when the PHY does not sense any energy on the cable and that no Link pulses (NLP, FLP, Beacons) are received. After spending VSPEC1_NBT_DS_CTRL.NRG_RST_CNT without energy in the ABILITY_DETECT state defined by IEEE802.3 Clause 28, the PHY enters ULP.<br>$0_B$ **OFF** ULP is DisabledGPY will not never enter ULP.<br>$1_B$ **ON** ULP is EnabledGPY will enter ULP is no energy |
| PSCL | 2 | RW | **Power Consumption Scaling Depending on Link Quality**<br>Allows enabling/disabling of the power consumption scaling dependent on the link quality.<br>$0_B$ **OFF** PSCL is disabled<br>$1_B$ **ON** PSCL is enabled |
| ANPD | 1 | RW | **Auto-Negotiation Power Down**<br>Allows enabling/disabling of the power down modes during auto-negotiation looking for a link partner.<br>$0_B$ **OFF** ANPD is disabled<br>$1_B$ **ON** ANPD is enabled |
| LPI | 0 | RW | **Assert LPI via MDIO**<br>Controls Asserts/de-asserts of LPI by MDIO instead of following (X)GMII LPI<br>Used to force the EEE on the TPI (ignoring the LPI indication from MAC)<br>$0_B$ **DEASSERT** LPI is de-asserted TPI<br>$1_B$ **ASSERT** LPI is asserted on TPI |

### Error Counter (Register 0.21)

This register controls the error counter. It allows the number of errors detected in the PHY to be counted for monitoring purposes.

IEEE Standard Register=0.21

**PHY_ERRCNT** **Reset Value**
**Error Counter (Register 0.21)** **$0000_H$**

| 15 … 12 | 11 … 8 | 7 … 0 |
|---|---|---|
| **RES** | **SEL** | **COUNT** |
| ro | rw | rosc |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:12 | RO | **Reserved**<br>Write as zero, ignored on read. |
| SEL | 11:8 | RW | **Select Error Event**<br>Configures which error type the error counter counts<br>$0000_B$**RXERR** Receive errors are counted<br>$0001_B$**RXACT** Receive frames are counted<br>$0010_B$**ESDERR** ESD errors are counted<br>$0011_B$**SSDERR** SSD errors are counted<br>$0100_B$**TXERR** Transmit errors are counted<br>$0101_B$**TXACT** Transmit frames events get counted<br>$0110_B$**COL** Collision events get counted<br>$1000_B$**NLD** Number of Link Down events get counted<br>$1001_B$**NDS** Number of auto-downspeed events get counted<br>$1010_B$**CRC** CRC counter<br>$1011_B$**TTL** Time to Link |
| COUNT | 7:0 | ROSC | **Counter Value**<br>This counter value is updated each time the selected error event has been detected. The counter value is reset every time a read operation on this register is performed or the error event is changed. The counter saturates at value 0xFF. |

**Media-Independent Interface Status (Register 0.24)**

This register contains status information on the Ethernet link, concatenated in a single register to allow concise status read by the STA in a single register.

IEEE Standard Register=0.24

**PHY_MIISTAT** **Reset Value**

**Media-Independent Interface Status (Register 0.24)** **$0000_H$**

| 15–11 | 10 | 9 | 8 | 7–6 | 5–4 | 3 | 2–0 |
|---|---|---|---|---|---|---|---|
| **RES2** | **LS** | **MSRES** | **EEE** | **RES1** | **PS** | **DPX** | **SPEED** |
| ro | roll | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES2 | 15:11 | RO | **Reserved**<br>Write as zero, ignored on read. |
| LS | 10 | ROLL | **Link Status at which GPY Ethernet PHY Operates**<br>Indicates the link status of the PHY<br>$0_B$ **INACTIVE** The link is down.No communication with link partner possible.<br>$1_B$ **ACTIVE** The link is up.Data communication with link partner is possible. |
| MSRES | 9 | RO | **Master/Slave Configuration**<br>Master/Slave Configuration<br>$0_B$ **SLAVE** Local PHY configuration is SLAVE after ANEG<br>$1_B$ **MASTER** Local PHY configuration is MASTER after ANEG |
| EEE | 8 | RO | **Energy-Efficient Ethernet Mode**<br>$0_B$ **OFF** EEE is disabled after auto-negotiation resolution<br>$1_B$ **ON** EEE is enabled after auto-negotiation resolution |
| RES1 | 7:6 | RO | **Reserved** |
| PS | 5:4 | RO | **Pause Status for Flow Control**<br>$00_B$ **NONE** No PAUSE<br>$01_B$ **TX** Transmit PAUSE<br>$10_B$ **RX** Receive PAUSE<br>$11_B$ **TXRX** Both transmit and receive PAUSE |
| DPX | 3 | RO | **GPY Ethernet PHY Duplex Mode**<br>$0_B$ **HDX** Half duplex<br>$1_B$ **FDX** Full duplex |
| SPEED | 2:0 | RO | **GPY Ethernet PHY Speed**<br>$000_B$ **TEN** 10 Mbit/s<br>$001_B$ **FAST** 100 Mbit/s<br>$010_B$ **GIGA** 1000 Mbit/s<br>$011_B$ **ANEG** Autonegotiation mode<br>$100_B$ **BZ2G5** 2.5GBit/s |

**Interrupt Mask Register (Register 0.25)**

This register defines the mask for the Interrupt Status Register (ISTAT) which contains the event source for the MDINT interrupt sent from GPY to an external chip.

The information about the interrupt source is indicated in the ISTAT register.

IEEE Standard Register=0.25

**PHY_IMASK** **Reset Value**
**Interrupt Mask Register (Register 0.25)** **$0000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **WOL** | **MSRE** | **NPRX** | **NPTX** | **ANE** | **ANC** | **Res** | **LOR** | **ULP** | **TEMP** | **ADSC** | **MDIPC** | **MDIXC** | **DXMC** | **LSPC** | **LSTC** |
| rw | rw | rw | rw | rw | rw | | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| WOL | 15 | RW | **Wake-on-LAN Event Mask**<br>When active and masked in IMASK, the MDINT is activated upon detection of a valid Wake-on-LAN event.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| MSRE | 14 | RW | **Master/Slave Resolution Error Mask**<br>When active, MDINT is activated upon detection of a master/slave resolution error during a 1000BASE-T auto-negotiation.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| NPRX | 13 | RW | **Next Page Received Mask**<br>When active, MDINT is activated upon reception of a next page in STD.AN_NPRX.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| NPTX | 12 | RW | **Next Page Transmitted Mask**<br>When active, MDINT is activated upon transmission of the currently stored next page in STD.AN_NPTX.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| ANE | 11 | RW | **Auto-Negotiation Error Mask**<br>When active, MDINT is activated upon detection of an auto-negotiation error.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| ANC | 10 | RW | **Auto-Negotiation Complete Mask**<br>When active, MDINT is activated upon completion of the auto-negotiation process.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| LOR | 8 | RW | **SyncE Lost Of Reference**<br>When active, MDINT is activated upon loss of SyncE reference clock.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| ULP | 7 | RW | **ULP Entry Indication Mask**<br>$0_B$ **INACTIVE** Interrupt is masked outSTA does not need to be informed of the event<br>$1_B$ **ACTIVE** Interrupt is activatedSTA receives MDINT when PHY is about to enter ULPThen the condition to ULP Entry to is based on PHY_CTL2.ULP_STA_BLOCK. |
| TEMP | 6 | RW | **TEMP**<br>$0_B$ **INACTIVE** Interrupt is masked outSTA does not require to be informed of the event<br>$1_B$ **ACTIVE** Interrupt is activatedInterrupt is raised when temperature goes beyond Normal Operating Range |
| ADSC | 5 | RW | **Link Speed Auto-Downspeed Detect Mask**<br>When active, MDINT is activated upon detection of a link speed auto-downspeed event.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| MDIPC | 4 | RW | **MDI Polarity Change Detect Mask**<br>When active, MDINT is activated upon detection of an MDI polarity change event.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| MDIXC | 3 | RW | **MDIX Change Detect Mask**<br>When active, MDINT is activated upon detection of an MDI/MDIX cross-over change event.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| DXMC | 2 | RW | **Duplex Mode Change Mask**<br>When active, MDINT is activated upon detection of full- or half-duplex change.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| LSPC | 1 | RW | **Link Speed Change Mask**<br>When active, MDINT is activated upon detection of link speed change.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| LSTC | 0 | RW | **Link State Change Mask**<br>When active, MDINT is activated upon detection of link status change.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |

**Interrupt Status Register (Register 0.26)**

This register defines the event source for the MDINT interrupt sent from GPY to an external chip.

PHY_ISTAT is a cleared on read by the STA.

IEEE Standard Register=0.26

**PHY_ISTAT** **Reset Value**
**Interrupt Status Register (Register 0.26)** **$0000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **WOL** | **MSRE** | **NPRX** | **NPTX** | **ANE** | **ANC** | **Res** | **LOR** | **ULP** | **TEMP** | **ADSC** | **MDIPC** | **MDIXC** | **DXMC** | **LSPC** | **LSTC** |
| rosc | rosc | rosc | rosc | rosc | rosc | | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc |

| Field | Bits | Type | Description |
|---|---|---|---|
| WOL | 15 | ROSC | **Wake-on-LAN Interrupt Status**<br>When bit is set, the MDINT is activated upon detection of a valid Wake-on-LAN event.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** WoL event is the source of the interrupt |
| MSRE | 14 | ROSC | **Master/Slave Resolution Error Interrupt Status**<br>When bit is set, the MDINT is activated upon detection of a master/slave resolution error during a 1000BASE-T auto-negotiation.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** MSRE event is the source of the interrupt |
| NPRX | 13 | ROSC | **Next Page Received Interrupt Status**<br>When bit is set, the MDINT is activated upon reception of a next page in STD.AN_NPRX.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** NPTX event is the source of the interrupt |
| NPTX | 12 | ROSC | **Next Page Transmitted Interrupt Status**<br>When bit is set, the MDINT is activated upon transmission of the currently stored next page in STD.AN_NPTX.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** NPTX event is the source of the interrupt |
| ANE | 11 | ROSC | **Auto-Negotiation Error Interrupt Status**<br>When bit is set, the MDINT is activated upon detection of an auto-negotiation error.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** ANEG error event is the source of the interrupt |
| ANC | 10 | ROSC | **Auto-Negotiation Complete Interrupt Status**<br>When bit is set, the MDINT is activated upon completion of the auto-negotiation process.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** ANEG complete event is the source of the interrupt |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| LOR | 8 | ROSC | **SyncE Lost Of Reference**<br>When bit is set, MDINT is activated upon loss of SyncE reference clock.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** LOR Change event is the source of the interrupt |
| ULP | 7 | ROSC | **ULP Entry Indication**<br>$0_B$ **INACTIVE** No indication of ULP entry<br>$1_B$ **ACTIVE** Indication of ULP EntryEntry to ULP is delayed until the STA has read PHY_ISTAT or not is based on PHY_CTL2.ULP_STA_BLOCK. |
| TEMP | 6 | ROSC | **TEMP**<br>Indicate a Thermal Mitigation action must be taken when the temperature goes beyond Operating Range. It is recommended that the SoC initiates a link-down and change speed capability to reduce go back to normal thermal Range. When the temperature reaches the Maximum Absolute Ratings, the GPY resets for safety purpose. Thermal mitigation must ensure that the temperature maximum absolute ratings are never reached.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** TEMP Change event is the source of the interrupt |
| ADSC | 5 | ROSC | **Link Speed Auto-Downspeed Detect Interrupt Status**<br>When bit is set, the MDINT is activated upon detection of a link speed auto-downspeed event.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** ADSC Change event is the source of the interrupt |
| MDIPC | 4 | ROSC | **MDI Polarity Change Detect Interrupt Status**<br>When bit is set, the MDINT is activated upon detection of an MDI polarity change event.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** MDIPC Change event is the source of the interrupt |
| MDIXC | 3 | ROSC | **MDIX Change Detect Interrupt Status**<br>When bit is set, the MDINT is activated upon detection of an MDI/MDIX cross-over change event.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** MDIX Change event is the source of the interrupt |
| DXMC | 2 | ROSC | **Duplex Mode Change Interrupt Status**<br>When bit is set, the MDINT is activated upon detection of a full or half-duplex change.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** Duplex Mode Change event is the source of the interrupt |
| LSPC | 1 | ROSC | **Link Speed Change Interrupt Status**<br>When bit is set, the MDINT is activated upon detection of link speed change.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** Link Speed Change event is the source of the interrupt |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| LSTC | 0 | ROSC | **Link State Change Interrupt Status**<br>When bit is set, the MDINT is activated upon detection of link status change.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** Link State Change event is the source of the interrupt |

**LED Control Register (Register 0.27)**

This register contains control bits for direct access to the LEDs by setting the on/off LEDxA bits ( with x from 0 to 4).

To directly control the LED, the integrated LED functions must be disabled by the LEDxEN bit in this register.

The integrated LED functions are specified in the more sophisticated LED control registers in MMD device VSPEC1.

IEEE Standard Register=0.27

**PHY_LED** **Reset Value**
**LED Control Register (Register 0.27)** **$FF00_H$**

| 15:12 | 11 | 10 | 9 | 8 | 7:4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| INV | LED3EN | LED2EN | LED1EN | LED0EN | RES1 | LED3DA | LED2DA | LED1DA | LED0DA |
| rw | rw | rw | rw | rw | ro | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| INV | 15:12 | RW | **Invert LED Output**<br>This provide a per LED control to invert the output of the LEDs. set to '1' to support LEDs which are driven by VDDs. Set to '0' to support LEDs which are driven by the output pins of this product. |
| LED3EN | 11 | RW | **Enable Integrated Function of LED3**<br>Write a 0 to this bit to disable the pre-configured integrated function for this LED.<br>The LED remains off unless directly accessed via LED3DA.<br>$0_B$ **DISABLE** Disables the integrated LED function<br>$1_B$ **ENABLE** Enables the integrated LED function |
| LED2EN | 10 | RW | **Enable Integrated Function of LED2**<br>Write a 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED2DA.<br>$0_B$ **DISABLE** Disables the integrated LED function<br>$1_B$ **ENABLE** Enables the integrated LED function |
| LED1EN | 9 | RW | **Enable Integrated Function of LED1**<br>Write a 0 to this bit to disable the pre-configured integrated function for this LED.<br>The LED remains off unless directly accessed via LED1DA.<br>$0_B$ **DISABLE** Disables the integrated LED function<br>$1_B$ **ENABLE** Enables the integrated LED function |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| LED0EN | 8 | RW | **Enable Integrated Function of LED0**<br>Write a 0 to this bit to disable the pre-configured integrated function for this LED.<br>The LED remains off unless directly accessed via LED0DA.<br>$0_B$ **DISABLE** Disables the integrated LED function<br>$1_B$ **ENABLE** Enables the integrated LED function |
| RES1 | 7:4 | RO | **Reserved**<br>Write as zero, ignored on read. |
| LED3DA | 3 | RW | **Direct Access to LED3**<br>Write a 1 to this bit to illuminate the LED. Note that LED3EN must be set to zero.<br>$0_B$ **OFF** Switch off the LED<br>$1_B$ **ON** Switch on the LED |
| LED2DA | 2 | RW | **Direct Access to LED2**<br>Write a 1 to this bit to illuminate the LED. Note that LED2EN must be set to zero.<br>$0_B$ **OFF** Switch off the LED<br>$1_B$ **ON** Switch on the LED |
| LED1DA | 1 | RW | **Direct Access to LED1**<br>Write a 1 to this bit to illuminate the LED. Note that LED1EN must be set to zero.<br>$0_B$ **OFF** Switch off the LED<br>$1_B$ **ON** Switch on the LED |
| LED0DA | 0 | RW | **Direct Access to LED0**<br>Write a 1 to this bit to illuminate the LED. Note that LED0EN must be set to zero.<br>$0_B$ **OFF** Switch off the LED<br>$1_B$ **ON** Switch on the LED |

**Firmware Version Register (Register 0.30)**

This register contains the version of the PHY firmware. The version number is initialized at boot time by the firmware with its current software version. This register is read-only by the external STA.

IEEE Standard Register=0.30

**PHY_FWV** **Reset Value**
**Firmware Version Register (Register 0.30)** **$0000_H$**

| 15 | 14 … 8 | 7 … 0 |
|---|---|---|
| **REL** | **MAJOR** | **MINOR** |
| ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| REL | 15 | RO | **Release Indication**<br>This parameter indicates either a test or a release version.<br>$0_B$ **TEST** Indicates a test version<br>$1_B$ **RELEASE** Indicates a released version |
| MAJOR | 14:8 | RO | **Major Version Number**<br>Specifies the main version release number of the firmware. |
| MINOR | 7:0 | RO | **Minor Version Number**<br>Specifies the sub-version release number of the firmware. |

**Internal Test Modes CDIAG and ABIST (Register 0.31)**

This is the control register used to configure the Gigabit Ethernet behavior of the PHY. See also IEEE 802.3-2008 40.5.1.1.

IEEE Standard Register=0.31

**PHY_TEST** **Reset Value**
**Internal Test Modes CDIAG and ABIST (Register 0.31)** **$0000_H$**

| 15–13 | 12–8 | 7 | 6 | 5–4 | 3–0 |
|---|---|---|---|---|---|
| TM | RES | ABUART | ABRET | ABSEL | ABOPT |
| rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| TM | 15:13 | RW | **Proprietary Test Modes ABIST and CDIAG**<br>Enter the test mode. Any value different from 6 or 7 has no effect.<br>$110_B$ **CDIAG** GPY specificCable Diagnostic<br>$111_B$ **ABIST** GPY specificAnalog build in self-test |
| RES | 12:8 | RW | **Reserved** |
| ABUART | 7 | RW | **ABIST UART output for debug**<br>If set to 1, enable detail report on the debug UART output. This is used to debug the feature and not in production mode, because in that case the 2 LED signals are not used to indicate completion or pass fail. An alternative to UART is to read the STB via MDIO commands.<br>$0_B$ **NORMAL** ABIST normal output<br>$1_B$ **UART** ABIST output to UART |
| ABRET | 6 | RW | **ABIST ReTrig**<br>If set to 1, enable restart of the selected ABIST test. This is used to debug the feature and not in production mode<br>$0_B$ **NORMAL** Normal Mode<br>$1_B$ **RETRIG** Restart the current ABIST Test |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| ABSEL | 5:4 | RW | **ABIST sub-mode selection**<br>00B, ABIST Analog Tests<br>01B, ABIST DC tests<br>10B, reserved<br>11B, reserved<br>$00_B$ **ANALOG** ABIST Analog Tests<br>$01_B$ **DC** ABIST DC Tests |
| ABOPT | 3:0 | RW | **ABIST Option for DC test**<br>In ABIST DC test<br>0000, ABIST DC test for 10BT mode LD, max positive differential level<br>0001, ABIST DC test for 1000BT mode LD, max positive differential level<br>0010, ABIST DC test for 10BT mode LD, 0 differential level<br>0011, ABIST DC test for 1000BT mode LD, 0 differential level<br>0100, ABIST DC test for 10BT mode LD, max negative differential level<br>0101, ABIST DC test for 1000BT mode LD, max negative differential level<br>0110, ABIST DC test for 2500BT mode LD, max positive differential level<br>0111, ABIST DC test for 2500BT mode LD, 0 differential level<br>1000, ABIST DC test for 2500BT mode LD, max negative differential level |

# 6 MMD Registers Detailed Description

**Table 20 Register Access Type**

| Mode | Symbol |
|---|---|
| Status Register, (Status, or Ability Register) | RO |
| Read-Write Register, (e.g. MDIO Register) | RW |
| Read-Write, Self-Clearing Register (bit is cleared after read from MDIO) | RWSC |

## 6.1 Standard PMAPMD Registers for MMD=0x01

**Table 21 Registers Overview**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| PMA_CTRL1 | PMA/PMD Control 1 (Register 1.0) | $2058_H$ |
| PMA_STAT1 | PMA/PMD status 1 (Register 1.1) | $0000_H$ |
| PMA_DEVID1 | PHY Identifier 1 (Register 1.2) | $67C9_H$ |
| PMA_DEVID2 | PHY Identifier 2 (Register 1.3) | $DC00_H$ [1)] |
| PMA_SPEED_ABILITY | PMA/PMD speed ability (Register 1.4) | $2070_H$ |
| PMA_DIP1 | Devices in package 1 (Register 1.5) | $008B_H$ |
| PMA_DIP2 | Devices in package 2 (Register 1.6) | $C000_H$ |
| PMA_CTL2 | PMA/PMD control 2 (Register 1.7) | $0030_H$ |
| PMA_STAT2 | PMA/PMD status 2 (Register 1.8) | $8200_H$ |
| PMA_EXT_ABILITY | PMA/PMD Extended Ability (Register 1.11) | $41A0_H$ |
| PMA_PACKID1 | AN package identifier (Register 1.14) | $67C9_H$ |
| PMA_PACKID2 | AN package identifier (Register 1.15) | $DC00_H$ [1)] |
| PMA_MGBT_EXTAB | PMAPMD Extended Ability (Register 1.21) | $0001_H$ |
| PMA_MGBT_STAT | MULTIGBASE-T status (Register 1.129) | $0000_H$ |
| PMA_MGBT_POLARITY | MULTIGBASE-T pair swap and polarity (Register 1.130) | $0003_H$ |
| PMA_MGBT_TX_PBO | MULTIGBASE-T TX power backoff and PHY short reach setting (Register 1.131) | $0000_H$ |
| PMA_MGBT_TEST_MODE | MULTIGBASE-T test mode (Register 1.132) | $0000_H$ |
| PMA_MGBT_SNR_OPMARGIN_A | MULTIGBASE-T SNR Margin Channel A (Register 1.133) | $0000_H$ |
| PMA_MGBT_SNR_OPMARGIN_B | MULTIGBASE-T SNR Margin Channel B (Register 1.134) | $0000_H$ |
| PMA_MGBT_SNR_OPMARGIN_C | MULTIGBASE-T SNR Margin Channel C (Register 1.135) | $0000_H$ |
| PMA_MGBT_SNR_OPMARGIN_D | MULTIGBASE-T SNR Margin Channel D (Register 1.136) | $0000_H$ |
| PMA_MGBT_MINMARGIN_A | MULTIGBASE-T SNR Min Margin Channel A (Register 1.137) | $0000_H$ |
| PMA_MGBT_MINMARGIN_B | MULTIGBASE-T SNR Min Margin Channel B (Register 1.138) | $0000_H$ |
| PMA_MGBT_MINMARGIN_C | MULTIGBASE-T SNR Min Margin Chan C (Register 1.139) | $0000_H$ |
| PMA_MGBT_MINMARGIN_D | MULTIGBASE-T SNR Min Margin Chan D (Register 1.140) | $0000_H$ |
| PMA_MGBT_POWER_A | MULTIGBASE-T Rx Power Channel A (Register 1.141) | $0000_H$ |

**Table 21 Registers Overview** (cont'd)

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| PMA_MGBT_POWER_B | MULTIGBASE-T Rx Power Channel B (Register 1.142) | $0000_H$ |
| PMA_MGBT_POWER_C | MULTIGBASE-T Rx Power Chan C (Register 1.143) | $0000_H$ |
| PMA_MGBT_POWER_D | MULTIGBASE-T Rx Power Chan D (Register 1.144) | $0000_H$ |
| PMA_MGBT_SKEW_DELAY_0 | MULTIGBASE-T skew delay 0 (Register 1.145) | $0000_H$ |
| PMA_MGBT_SKEW_DELAY_1 | MULTIGBASE-T skew delay 1 (Register 1.146) | $0000_H$ |
| PMA_MGBT_FAST_RETRAIN_STA_CTRL | MULTIGBASE-T skew delay 2 (Register 1.147) | $0000_H$ |
| PMA_TIMESYNC_CAP | PMA TimeSync Capability Indication (Register 1.1800) | $0000_H$ |

1) For the device specific reset value, refer to Product Naming table in the **Package Outline** chapter.

### 6.1.1 Standard PMAPMD Registers for MMD=0x01

This chapter describes all registers of PMAPMD in detail.

**PMA/PMD Control 1 (Register 1.0)**

IEEE Standard Register=1.0

**PMA_CTRL1** **Reset Value**
**PMA/PMD Control 1 (Register 1.0)** **$2058_H$**

| 15 | 14 | 13 | 12 | 11 | 10–7 | 6 | 5–2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| RST | Res | SSL | Res | LOW_POW* | Res | SSM | SPEED_SEL | NS1 | NS2 |
| rw | | rw | | rw | | rw | rw | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RST | 15 | RW | **Reset**<br>1 = PMA/PMD reset<br>0 = Normal operation |
| SSL | 13 | RW | **Speed Selection (LSB)**<br>Used in conjunction with field SPEED_SEL_MSB<br>MSB LSB:<br>1 1 = bits 5:2 are used to select speed (SPEED_SEL field)<br>1 0 = 1000 Mb/s<br>0 1 = 100 Mb/s<br>0 0 = 10 Mb/s |
| LOW_POWER | 11 | RW | **Low power**<br>1 = Enter Low power mode<br>0 = Normal operation |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| SSM | 6 | RW | **Speed Selection (MSB)**<br>Used in conjunction with field SPEED_SEL_LSB<br>MSB LSB:<br>1 1 = bits 5:2 select speed (SPEED_SEL field)<br>1 0 = 1000 Mb/s<br>0 1 = 100 Mb/s<br>0 0 = 10 Mb/s |
| SPEED_SEL | 5:2 | RW | **Speed Selection**<br>Bit usage ( from bit 5 to bit 2):<br>1 x x x = Reserved<br>0 1 1 1 = Not supported<br>0 1 1 0 = 2.5 Gb/s<br>0 1 0 0 = Not supported, defaults to 2.5 Gb/s<br>0 0 1 1 = Not supported, defaults to 2.5 Gb/s<br>0 0 1 0 = Not supported, defaults to 2.5 Gb/s<br>0 0 0 1 = Not supported, defaults to 2.5 Gb/s<br>0 0 0 0 = Not supported, defaults to 2.5 Gb/s<br>$0110_B$**S2G5** Forced Speed is 2G5 |
| NS1 | 1 | RO | **Not Supported**<br>PMA remote loop-back mode is not supported by GPY |
| NS2 | 0 | RO | **Not Supported**<br>PMA local loop-back mode is not supported by GPY |

**PMA/PMD status 1 (Register 1.1)**

IEEE Standard Register=1.1

**PMA_STAT1** **Reset Value**
**PMA/PMD status 1 (Register 1.1)** **$0000_H$**

| 15–8 | 7 | 6–3 | 2 | 1 | 0 |
|---|---|---|---|---|---|
| **Res** | **FAULT** | **Res** | **RX_LINK*** | **LOW_POW*** | **Res** |
| | ro | | ro | ro | |

| Field | Bits | Type | Description |
|---|---|---|---|
| FAULT | 7 | RO | **Fault**<br>1 = Fault condition detected<br>0 = Fault condition not detected |
| RX_LINK_STATUS | 2 | RO | **Receive Link Status**<br>1 = PMA/PMD receive link up<br>0 = PMA/PMD receive link down |
| LOW_POWER_ABILITY | 1 | RO | **Low Power Ability**<br>1 = PMA/PMD supports low power mode<br>0 = PMA/PMD does not support low power mode |

**PHY Identifier 1 (Register 1.2)**

IEEE Standard Register=1.2

Bits 31 - 16 of Device ID

**PMA_DEVID1** **Reset Value**
**PHY Identifier 1 (Register 1.2)** **67C9$_H$**

| 15 … 0 |
|---|
| **OUI** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | **Organizationally Unique Identifier**<br>Organizationally Unique Identifier Bits 3:18 |

**PHY Identifier 2 (Register 1.3)**

IEEE Standard Register=1.3

Bits 15 - 0 of Device ID

**PMA_DEVID2** **Reset Value**
**PHY Identifier 2 (Register 1.3)** **DC00$_H$**

| 15 … 10 | 9 … 4 | 3 … 0 |
|---|---|---|
| **OUI** | **LDN** | **LDRN** |
| ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier Bits 19:24** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1)] to distinguish between several products. |
| LDRN | 3:0 | RO | **Device Number**<br>Specifies the device revision number[1)] to distinguish between several versions of this device |

1) For the device specific reset value, refer to Product Naming table in the **Package Outline** chapter.

**PMA/PMD speed ability (Register 1.4)**

IEEE Standard Register=1.4

**PMA_SPEED_ABILITY** **Reset Value**

**PMA/PMD speed ability (Register 1.4)** **$2070_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Res | CAP_5G | CAP_2G5 | RES2 | Res | | CAP_100G | CAP_40G | CAP_10_* | CAP_10M | CAP_100M | CAP_100* | Res | R10PASS* | CAP_2BA* | CAP_10G* |
| | ro | ro | ro | | | ro | ro | ro | ro | ro | ro | | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| CAP_5G | 14 | RO | **Not Supported**<br>1 = PMA/PMD is capable of operating at 5 Gb/s<br>0 = PMA/PMD is not capable of operating as 5 Gb/s |
| CAP_2G5 | 13 | RO | **2.5 G capable**<br>1 = PMA/PMD is capable of operating at 2.5 Gb/s<br>0 = PMA/PMD is not capable of operating as 2.5 Gb/s |
| RES2 | 12 | RO | **Reserved**<br>Value always 0 |
| CAP_100G | 9 | RO | **Not Supported**<br>1 = PMA/PMD is capable of operating at 100 Gb/s<br>0 = PMA/PMD is not capable of operating as 100 Gb/s |
| CAP_40G | 8 | RO | **Not Supported**<br>1 = PMA/PMD is capable of operating at 40 Gb/s<br>0 = PMA/PMD is not capable of operating as 40 Gb/s |
| CAP_10_1G | 7 | RO | **Not Supported**<br>1 = PMA/PMD is capable of operating at 10 Gb/s downstream and 1 Gb/s upstream<br>0 = PMA/PMD is not capable of operating at 10 Gb/s downstream and 1 Gb/s upstream. |
| CAP_10M | 6 | RO | **10M capable**<br>1 = PMA/PMD is capable of operating at 10 Mb/s<br>0 = PMA/PMD is not capable of operating as 10 Mb/s |
| CAP_100M | 5 | RO | **100M capable**<br>1 = PMA/PMD is capable of operating at 100 Mb/s<br>0 = PMA/PMD is not capable of operating at 100 Mb/s |
| CAP_1000M | 4 | RO | **1000M capable**<br>1 = PMA/PMD is capable of operating at 1000 Mb/s<br>0 = PMA/PMD is not capable of operating at 1000 Mb/s |
| R10PASS_TS_CAPABLE | 2 | RO | **Not Supported**<br>1 = PMA/PMD is capable of operating as 10PASS-TS<br>0 = PMA/PMD is not capable of operating as 10PASS-TS |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| CAP_2BASE_TL | 1 | RO | **Not Supported**<br>1 = PMA/PMD is capable of operating as 2BASE-TL<br>0 = PMA/PMD is not capable of operating as 2BASE-TL |
| CAP_10G_CAP | 0 | RO | **Not Supported**<br>1 = PMA/PMD is capable of operating at 10 Gb/s<br>0 = PMA/PMD is not capable of operating at 10 Gb/s |

**Devices in package 1 (Register 1.5)**

IEEE Standard Register=1.5

**PMA_DIP1** **Reset Value**

**Devices in package 1 (Register 1.5)** **008B$_H$**

| 15–12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **RES** | **SEP_PMA*** | **SEP_PMA*** | **SEP_PMA*** | **SEP_PMA*** | **ANEG** | **TC** | **DTE_XS** | **PHY_XS** | **PCS** | **WIS** | **PMD_PMA** | **CLAUSE_*** |
| ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:12 | RO | **Reserved**<br>Ignore on Read |
| SEP_PMA_4 | 11 | RO | **Separate PMA (4)**<br>1 = Separated PMA (4) present in package<br>0 = Separated PMA (4) not present in package |
| SEP_PMA_3 | 10 | RO | **Separate PMA (3)**<br>1 = Separated PMA (3) present in package<br>0 = Separated PMA (3) not present in package |
| SEP_PMA_2 | 9 | RO | **Separate PMA (2)**<br>1 = Separated PMA (2) present in package<br>0 = Separated PMA (2) not present in package |
| SEP_PMA_1 | 8 | RO | **Separate PMA (1)**<br>1 = Separated PMA (1) present in package<br>0 = Separated PMA (1) not present in package |
| ANEG | 7 | RO | **Auto-Negotiation present**<br>This bit is always set to 1 in GPY<br>1 = Auto-Negotiation present in package<br>0 = Auto-Negotiation not present in package |
| TC | 6 | RO | **TC present**<br>1 = TC present in package<br>0 = TC not present in package |
| DTE_XS | 5 | RO | **DTE XS present**<br>1 = DTE XS present in package<br>0 = DTE XS not present in package |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| PHY_XS | 4 | RO | **PHY XS present**<br>1 = PHY XS present in package<br>0 = PHY XS not present in package |
| PCS | 3 | RO | **PCS present**<br>This bit is always set to 1 in GPY<br>1 = PCS present in package<br>0 = PCS not present in package |
| WIS | 2 | RO | **WIS present**<br>1 = WIS present in package<br>0 = WIS not present in package |
| PMD_PMA | 1 | RO | **PMD/PMA present**<br>This bit is always set to 1 in GPY<br>1 = PMA/PMD present in package<br>0 = PMA/PMD not present in package |
| CLAUSE_22 | 0 | RO | **Clause 22 registers present**<br>This bit is always set to 1 in GPY<br>1 = Clause 22 registers present in package<br>0 = Clause 22 registers not present in package |

**Devices in package 2 (Register 1.6)**

IEEE Standard Register=1.6

**PMA_DIP2** **Reset Value**

**Devices in package 2 (Register 1.6)** **$C000_H$**

| 15 | 14 | 13 | 12 … 0 |
|---|---|---|---|
| **VSPEC2** | **VSPEC1** | **CLA_22_*** | **RES** |
| ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| VSPEC2 | 15 | RO | **Vendor-specific device 2**<br>This bit is always set to 1 in GPY<br>1 = Vendor-specific device 2 present in package<br>0 = Vendor-specific device 2 not present in package |
| VSPEC1 | 14 | RO | **Vendor-specific device 1**<br>This bit is always set to 1 in GPY<br>1 = Vendor-specific device 1 present in package<br>0 = Vendor-specific device 1 not present in package |
| CLA_22_EXT | 13 | RO | **Clause 22 extension**<br>1 = Clause 22 extension present in package<br>0 = Clause 22 extension not present in package |
| RES | 12:0 | RO | **Reserved**<br>Ignore on read |

**PMA/PMD control 2 (Register 1.7)**

IEEE Standard Register=1.7

**PMA_CTL2** **Reset Value**
**PMA/PMD control 2 (Register 1.7)** **$0030_H$**

| 15 … 6 | 5 … 0 |
|---|---|
| **Res** | **PMA_PMD_TYPE_SEL** |
| | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| PMA_PMD_TYPE_SEL | 5:0 | RW | **PMA/PMD type selection**<br>5 4 3 2 1 0<br>1 1 0 0 0 1 = unsupported, defaults to 2.5GBASE-T PMA<br>1 1 0 0 0 0 = 2.5GBASE-T PMA<br>1 0 1 1 x x = unsupported, defaults to 2.5GBASE-T PMA<br>1 0 1 0 1 1 = unsupported, defaults to 2.5GBASE-T PMA<br>1 0 1 0 1 0 = unsupported, defaults to 2.5GBASE-T PMA<br>1 0 1 0 0 1 = unsupported, defaults to 2.5GBASE-T PMA<br>1 0 1 0 0 0 = unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 1 1 x = unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 1 0 1 = unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 1 0 0 = unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 0 1 1 = unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 0 1 0 = unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 0 0 1 = unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 0 0 0 = unsupported, defaults to 2.5GBASE-T PMA<br>0 1 1 1 x x = unsupported, defaults to 2.5GBASE-T PMA<br>0 1 1 0 1 1 = unsupported, defaults to 2.5GBASE-T PMA<br>0 1 1 0 1 0 = unsupported, defaults to 2.5GBASE-T PMA<br>0 1 1 0 0 1 = unsupported, defaults to 2.5GBASE-T PMA<br>0 1 1 0 0 0 = unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 1 1 1 = unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 1 1 0 = unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 1 0 1 = unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 1 0 0 = unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 0 1 1 = unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 0 1 0 = unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 0 0 1 = unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 0 0 0 = unsupported, defaults to 2.5GBASE-T PMA<br>0 0 1 1 1 1 = 10BASE-T PMA/PMD<br>0 0 1 1 1 0 = 100BASE-TX PMA/PMD<br>0 0 1 1 0 1 = unsupported, defaults to 2.5GBASE-T PMA<br>0 0 1 1 0 0 = 1000BASE-T PMA/PMD<br>0 0 1 0 1 1 = unsupported, defaults to 2.5GBASE-T PMA<br>0 0 1 0 1 0 = unsupported, defaults to 2.5GBASE-T PMA<br>0 0 1 0 0 1 = unsupported, defaults to 2.5GBASE-T PMA<br>0 0 1 0 0 0 = unsupported, defaults to 2.5GBASE-T PMA<br>0 0 0 1 1 1 = unsupported, defaults to 2.5GBASE-T PMA<br>0 0 0 1 1 0 = unsupported, defaults to 2.5GBASE-T PMA<br>0 0 0 1 0 1 = unsupported, defaults to 2.5GBASE-T PMA<br>0 0 0 1 0 0 = unsupported, defaults to 2.5GBASE-T PMA<br>0 0 0 0 1 1 = unsupported, defaults to 2.5GBASE-T PMA<br>0 0 0 0 1 0 = unsupported, defaults to 2.5GBASE-T PMA<br>0 0 0 0 0 1 = unsupported, defaults to 2.5GBASE-T PMA<br>0 0 0 0 0 0 = unsupported, defaults to 2.5GBASE-T PMA |

**PMA/PMD status 2 (Register 1.8)**

IEEE Standard Register=1.8

**PMA_STAT2** **Reset Value**
**PMA/PMD status 2 (Register 1.8)** **$8200_H$**

| 15–14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **DEVICE_PRESENT** | **TX_FAUL*** | **RX_FAUL*** | **TX_FAULT** | **RX_FAULT** | **EXT_ABI*** | **PMD_TX_*** | **RMGBT_S*** | **RMGBT_L*** | **RMGBT_E*** | **RMGBT_L*** | **RMGBT_S*** | **RMGBT_L*** | **RMGBT_E*** | **PMA_LOC*** |
| ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| DEVICE_PRESENT | 15:14 | RO | **Device present**<br>1 0 = Device responding at this address<br>1 1 = No device responding at this address<br>0 1 = No device responding at this address<br>0 0 = No device responding at this address |
| TX_FAULT_ABILITY | 13 | RO | **Transmit fault ability**<br>1 = PMA/PMD has the ability to detect a fault condition on the transmit path<br>0 = PMA/PMD does not have the ability to detect a fault condition on the transmit path |
| RX_FAULT_ABILITY | 12 | RO | **Receive fault ability**<br>1 = PMA/PMD has the ability to detect a fault condition on the receive path<br>0 = PMA/PMD does not have the ability to detect a fault condition on the receive path |
| TX_FAULT | 11 | RO | **Transmit fault**<br>1 = Fault condition on transmit path<br>0 = No fault condition on transmit path |
| RX_FAULT | 10 | RO | **Receive fault**<br>1 = Fault condition on receive path<br>0 = No fault condition on receive path |
| EXT_ABILITIES | 9 | RO | **Extended abilities**<br>1 = PMA/PMD has extended abilities listed in register 1.11<br>0 = PMA/PMD does not have extended abilities |
| PMD_TX_DISABLE | 8 | RO | **PMD transmit disable**<br>1 = PMD has the ability to disable the transmit path<br>0 = PMD does not have the ability to disable the transmit path |
| RMGBT_SR_ABILITY | 7 | RO | **MULTIGBASE-SR ability**<br>1 = PMA/PMD is able to perform MULTIGBASE-SR<br>0 = PMA/PMD is not able to perform MULTIGBASE-SR |
| RMGBT_LR_ABILITY | 6 | RO | **MULTIGBASE-LR ability**<br>1 = PMA/PMD is able to perform MULTIGBASE-LR<br>0 = PMA/PMD is not able to perform MULTIGBASE-LR |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| RMGBT_ER_ABILITY | 5 | RO | **MULTIGBASE-ER ability**<br>1 = PMA/PMD is able to perform MULTIGBASE-ER<br>0 = PMA/PMD is not able to perform MULTIGBASE-ER |
| RMGBT_LX4_ABILITY | 4 | RO | **MULTIGBASE-LX4 ability**<br>1 = PMA/PMD is able to perform MULTIGBASE-LX4<br>0 = PMA/PMD is not able to perform MULTIGBASE-LX4 |
| RMGBT_SW_ABILITY | 3 | RO | **MULTIGBASE-SW ability**<br>1 = PMA/PMD is able to perform MULTIGBASE-SW<br>0 = PMA/PMD is not able to perform MULTIGBASE-SW |
| RMGBT_LW_ABILITY | 2 | RO | **MULTIGBASE-LW ability**<br>1 = PMA/PMD is able to perform MULTIGBASE-LW<br>0 = PMA/PMD is not able to perform MULTIGBASE-LW |
| RMGBT_EW_ABILITY | 1 | RO | **MULTIGBASE-EW ability**<br>1 = PMA/PMD is able to perform MULTIGBASE-EW<br>0 = PMA/PMD is not able to perform MULTIGBASE-EW |
| PMA_LOCAL_LOOPBACK | 0 | RO | **PMA Local Loop-back**<br>1 = PMA has the ability to perform a local loop-back function<br>0 = PMA does not have the ability to perform a local loop-back function |

**PMA/PMD Extended Ability (Register 1.11)**

IEEE Standard Register=1.11

**PMA_EXT_ABILITY** — **Reset Value**

**PMA/PMD Extended Ability (Register 1.11)** — **$41A0_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Res** | **R2G5_EX*** | **Res** | | | **R40G_10*** | **P2MP_AB*** | **R10BASE*** | **R100BAS*** | **R1000BA*** | **R1000BA*** | **RMGBT_K*** | **RMGBT_K*** | **RMGBT_A*** | **RMGBT_L*** | **RMGBT_C*** |
| | ro | | | | ro | ro | ro | ro | ro | ro | ro | ro | ro | ror | ror |

| Field | Bits | Type | Description |
|---|---|---|---|
| R2G5_EXT_ABILITIES | 14 | RO | **2.5G/5G extended abilities**<br>1 = PMA/PMD has 2.5G/5G extended abilities listed in register 1.21<br>0 = PMA/PMD does not have 2.5G/5G extended abilities |
| R40G_100G_EXT_ABILITIES | 10 | RO | **40G/100G extended abilities**<br>1 = PMA/PMD has 40G/100G extended abilities listed in register 1.13<br>0 = PMA/PMD does not have 40G/100G extended abilities |
| P2MP_ABILITY | 9 | RO | **P2MP ability**<br>1 = PMA/PMD has P2MP abilities listed in register 1.12<br>0 = PMA/PMD does not have P2MP abilities |
| R10BASE_T_ABILITY | 8 | RO | **10BASE-T ability**<br>1 = PMA/PMD is able to perform 10BASE-T<br>0 = PMA/PMD is not able to perform 10BASE-T |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| R100BASE_TX_ABILITY | 7 | RO | **100BASE-TX ability**<br>1 = PMA/PMD is able to perform 100BASE-TX<br>0 = PMA/PMD is not able to perform 100BASE-TX |
| R1000BASE_KX_ABILITY | 6 | RO | **1000BASE-KX ability**<br>1 = PMA/PMD is able to perform 1000BASE-KX<br>0 = PMA/PMD is not able to perform 1000BASE-KX |
| R1000BASE_T_ABILITY | 5 | RO | **1000BASE-T ability**<br>1 = PMA/PMD is able to perform 1000BASE-T<br>0 = PMA/PMD is not able to perform 1000BASE-T |
| RMGBT_KR_ABILITY | 4 | RO | **MULTIGBASE-KR ability**<br>1 = PMA/PMD is able to perform MULTIGBASE-KR<br>0 = PMA/PMD is not able to perform MULTIGBASE-KR |
| RMGBT_KX4_ABILITY | 3 | RO | **MULTIGBASE-KX4 ability**<br>1 = PMA/PMD is able to perform MULTIGBASE-KX4<br>0 = PMA/PMD is not able to perform MULTIGBASE-KX4 |
| RMGBT_ABILITY | 2 | RO | **10GBASE-T ability**<br>1 = PMA/PMD is able to perform MULTIGBASE-T<br>0 = PMA/PMD is not able to perform MULTIGBASE-T |
| RMGBT_LRM_ABILITY | 1 | ROR | **MULTIGBASE-LRM ability**<br>1 = PMA/PMD is able to perform MULTIGBASE-LRM<br>0 = PMA/PMD is not able to perform MULTIGBASE-LRM |
| RMGBT_CX4_ABILITY | 0 | ROR | **MULTIGBASE-CX4 ability**<br>1 = PMA/PMD is able to perform MULTIGBASE-CX4<br>0 = PMA/PMD is not able to perform MULTIGBASE-CX4 |

**AN package identifier (Register 1.14)**

IEEE Standard Register=1.14

**PMA_PACKID1** — **Reset Value**
**AN package identifier (Register 1.14)** — **$67C9_H$**

| 15 … 0 |
|---|
| **OUI** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | **Organizationally Unique Identifier**<br>Organizationally Unique Identifier Bits 3:18 |

**AN package identifier (Register 1.15)**

IEEE Standard Register=1.15

**PMA_PACKID2** **Reset Value**
**AN package identifier (Register 1.15)** **$DC00_H$**

| 15 … 10 | 9 … 4 | 3 … 0 |
|---|---|---|
| **OUI** | **LDN** | **LDRN** |
| ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier Bits 19:24** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1)] to distinguish between several products. |
| LDRN | 3:0 | RO | **Device Number**<br>Specifies the device revision number[1)] to distinguish between several versions of this device |

1) For the device specific reset value, refer to Product Naming table in the **Package Outline** chapter.

**PMAPMD Extended Ability (Register 1.21)**

Read only, write from STA has no effect

IEEE Standard Register=1.21

**PMA_MGBT_EXTAB** **Reset Value**
**PMAPMD Extended Ability (Register 1.21)** **$0001_H$**

| 15 … 2 | 1 | 0 |
|---|---|---|
| **RES** | **AB5G** | **AB2G5** |
| ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:2 | RO | **Reserved**<br>Value always 0 |
| AB5G | 1 | RO | **PMA Ability to perform 5GBT**<br>$0_B$ **UNABLE** PMA is not able to perform 5GBT<br>$1_B$ **ABLE** PMA Able to perform 5GBT |
| AB2G5 | 0 | RO | **PMA Ability to perform 2G5BT**<br>$0_B$ **UNABLE** PMA is not able to perform 2G5BT<br>$1_B$ **ABLE** PMA Able to perform 2G5BT |

**MULTIGBASE-T status (Register 1.129)**

IEEE Standard Register=1.129

Indicates startup in 126.4.2.5 for 2.5G has been completed

When read as a 1, indicates that the startup protocol defined in 126.4.2.5 (for 2.5G/5GBASE-T) has been completed (link_status=OK, pcs_status = OK), and that the contents of bits 1.130.11:0 (Polarity), 1.131.15:10 (PBO), 1.145.14:8 (Skew), 1.146.14:8, and 1.146.6:0 (Skew), which are established during the startup protocol, are valid.

When read as a zero, bit 1.129.0 indicates that the startup process has not been completed, and that the contents of these bits that are established during the startup protocol are invalid. A PMA will return a value of zero in bit 1.129.1 if PMA link_status=FAIL.

**PMA_MGBT_STAT** **Reset Value**

**MULTIGBASE-T status (Register 1.129)** **$0000_H$**

| 15 … 1 | 0 |
|---|---|
| **Res** | **LP_INFO*** |
| | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| LP_INFORMATION_VALID | 0 | RO | **LP information valid**<br>When set this bit indicates the startup protocol (126.4.2.5) has completed.<br>1 = Link partner information is valid<br>0 = Link partner information is invalid |

**MULTIGBASE-T pair swap and polarity (Register 1.130)**

IEEE Standard Register=1.130

**PMA_MGBT_POLARITY** — **Reset Value**

**MULTIGBASE-T pair swap and polarity (Register 1.130)** — **$0003_H$**

| 15–12 | 11 | 10 | 9 | 8 | 7–2 | 1–0 |
|---|---|---|---|---|---|---|
| **Res** | **PAIR_D_*** | **PAIR_C_*** | **PAIR_B_*** | **PAIR_A_*** | **Res** | **MDI_MDI_X** |
| | ro | ro | ro | ro | | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| PAIR_D_POLARITY | 11 | RO | **Pair D polarity**<br>1 = Polarity of pair D is reversed<br>0 = Polarity of pair D is not reversed |
| PAIR_C_POLARITY | 10 | RO | **Pair C polarity**<br>1 = Polarity of pair C is reversed<br>0 = Polarity of pair C is not reversed |
| PAIR_B_POLARITY | 9 | RO | **Pair B polarity**<br>1 = Polarity of pair B is reversed<br>0 = Polarity of pair B is not reversed |
| PAIR_A_POLARITY | 8 | RO | **Pair A polarity**<br>1 = Polarity of pair A is reversed<br>0 = Polarity of pair A is not reversed |
| MDI_MDI_X | 1:0 | RO | **MDI/MDI-X**<br>Indicates the status of pair swaps at the MDI / MD-X<br>$00_B$ **ABCDCROSS** Pair AB and Pair CD crossover<br>$01_B$ **CDCROSS** Pair CD crossover only<br>$10_B$ **ABCROSS** Pair AB crossover only<br>$11_B$ **NORMAL** No crossover |

**MULTIGBASE-T TX power backoff and PHY short reach setting (Register 1.131)**

IEEE Standard Register=1.131

**PMA_MGBT_TX_PBO** — **Reset Value**

**MULTIGBASE-T TX power backoff and PHY short reach setting (Register 1.131)** — **$0000_H$**

| 15–13 | 12–10 | 9–1 | 0 |
|---|---|---|---|
| **LP_TX** | **TX_POWER_BACKOFF** | **Res** | **SHORT_R*** |
| ro | ro | | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| LP_TX | 15:13 | RO | **Link partner TX**<br>The power backoff setting of the link partner<br>Bit number assignment:<br>15 14 13<br>-------------<br>1 1 1 = 14 dB<br>1 1 0 = 12 dB<br>1 0 1 = 10 dB<br>1 0 0 = 8 dB<br>0 1 1 = 6 dB<br>0 1 0 = 4 dB<br>0 0 1 = 2 dB<br>0 0 0 = 0 dB |
| TX_POWER_BACKOFF | 12:10 | RO | **TX power backoff**<br>The power backoff of PHY211 PMA<br>Bit number assignment:<br>12 11 10<br>----------------<br>1 1 1 = 14 dB<br>1 1 0 = 12 dB<br>1 0 1 = 10 dB<br>1 0 0 = 8 dB<br>0 1 1 = 6 dB<br>0 1 0 = 4 dB<br>0 0 1 = 2 dB<br>0 0 0 = 0 dB |
| SHORT_REACH_MODE | 0 | RO | **Short reach mode**<br>1 = PHY is operating in short reach mode (not supported)<br>0 = PHY is not operating in short reach mode |

**MULTIGBASE-T test mode (Register 1.132)**

IEEE Standard Register=1.132

**PMA_MGBT_TEST_MODE** **Reset Value**

**MULTIGBASE-T test mode (Register 1.132)** **$0000_H$**

| 15 … 13 | 12 … 10 | 9 … 0 |
|---|---|---|
| **TEST_MODE_CTL** | **TXTER_TEST** | **Res** |
| rw | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| TEST_MODE_CTL | 15:13 | RW | **Test mode control**<br>1 1 1 = Test mode 7<br>1 1 0 = Test mode 6<br>1 0 1 = Test mode 5<br>1 0 0 = Test mode 4<br>0 1 1 = Test mode 3<br>0 1 0 = Test mode 2<br>0 0 1 = Test mode 1<br>0 0 0 = Normal operation |
| TXTER_TEST | 12:10 | RW | **Transmitter test**<br>Frequencies for tones used in Test Mode 4<br>1 1 1 = Reserved<br>1 1 0 = Dual tone 5<br>1 0 1 = Dual tone 4<br>1 0 0 = Dual tone 3<br>0 1 1 = Reserved<br>0 1 0 = Dual tone 2<br>0 0 1 = Dual tone 1<br>0 0 0 = Reserved |

**MULTIGBASE-T SNR Margin Channel A (Register 1.133)**

Register 1.133 contains the current SNR operating margin measured at the slicer input for channel A for the MULTIGBASE-T PMA.

IEEE Standard Register=1.133

**PMA_MGBT_SNR_OPMARGIN_A** **Reset Value**
**MULTIGBASE-T SNR Margin Channel A (Register 1.133)** **$0000_H$**

| 15 … 0 |
|---|
| **OPMARGIN_A** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OPMARGIN_A | 15:0 | RO | **OPMARGIN_A**<br>SNR operating margin measured at the slicer input for channel A |

**MULTIGBASE-T SNR Margin Channel B (Register 1.134)**

Register 1.134 contains the current SNR operating margin measured at the slicer input for channel B for the MULTIGBASE-T PMA.

IEEE Standard Register=1.134

**PMA_MGBT_SNR_OPMARGIN_B** **Reset Value**
**MULTIGBASE-T SNR Margin Channel B (Register 1.134)** **$0000_H$**

| 15 | | 0 |
|---|---|---|
| | OPMARGIN_B | |
| | ro | |

| Field | Bits | Type | Description |
|---|---|---|---|
| OPMARGIN_B | 15:0 | RO | **OPMARGIN_B**<br>SNR operating margin measured at the slicer input for channel B |

**MULTIGBASE-T SNR Margin Channel C (Register 1.135)**

Register 1.135 contains the current SNR operating margin measured at the slicer input for channel C for the MULTIGBASE-T PMA.

IEEE Standard Register=1.135

**PMA_MGBT_SNR_OPMARGIN_C** — **Reset Value**
**MULTIGBASE-T SNR Margin Channel C (Register 1.135)** — **$0000_H$**

| 15 | | 0 |
|---|---|---|
| | OPMARGIN_C | |
| | ro | |

| Field | Bits | Type | Description |
|---|---|---|---|
| OPMARGIN_C | 15:0 | RO | **OPMARGIN_C**<br>SNR operating margin measured at the slicer input for channel C |

**MULTIGBASE-T SNR Margin Channel D (Register 1.136)**

Register 1.136 contains the current SNR operating margin measured at the slicer input for channel D for the MULTIGBASE-T PMA.

IEEE Standard Register=1.136

**PMA_MGBT_SNR_OPMARGIN_D** — **Reset Value**
**MULTIGBASE-T SNR Margin Channel D (Register 1.136)** — **$0000_H$**

| 15 | | 0 |
|---|---|---|
| | OPMARGIN_D | |
| | ro | |

| Field | Bits | Type | Description |
|---|---|---|---|
| OPMARGIN_D | 15:0 | RO | **OPMARGIN_D**<br>SNR operating margin measured at the slicer input for channel D |

### MULTIGBASE-T SNR Min Margin Channel A (Register 1.137)

The minimum margin channel A register contains a latched copy of the lowest value observed in the SNR operating margin channel A register (1.133) since the last read.

IEEE Standard Register=1.137

**PMA_MGBT_MINMARGIN_A** — **Reset Value**

**MULTIGBASE-T SNR Min Margin Channel A (Register 1.137)** — **$0000_H$**

| 15 ... 0 |
|---|
| **MINMARGIN_A** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| MINMARGIN_A | 15:0 | RO | **MINMARGIN_A**<br>Lowest value observed in the SNR operating margin channel A register (1.133) since the last read |

### MULTIGBASE-T SNR Min Margin Channel B (Register 1.138)

The minimum margin channel A register contains a latched copy of the lowest value observed in the SNR operating margin channel B register (1.134) since the last read.

IEEE Standard Register=1.138

**PMA_MGBT_MINMARGIN_B** — **Reset Value**

**MULTIGBASE-T SNR Min Margin Channel B (Register 1.138)** — **$0000_H$**

| 15 ... 0 |
|---|
| **MINMARGIN_B** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| MINMARGIN_B | 15:0 | RO | **MINMARGIN_B**<br>Lowest value observed in the SNR operating margin channel B register (1.134) since the last read |

### MULTIGBASE-T SNR Min Margin Chan C (Register 1.139)

The minimum margin channel C register contains a latched copy of the lowest value observed in the SNR operating margin channel C register (1.135) since the last read.

IEEE Standard Register=1.139

**PMA_MGBT_MINMARGIN_C** **Reset Value**

**MULTIGBASE-T SNR Min Margin Chan C (Register 1.139)** **$0000_H$**

| 15 … 0 |
|---|
| **MINMARGIN_C** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| MINMARGIN_C | 15:0 | RO | **MINMARGIN_C**<br>Lowest value observed in the SNR operating margin channel C register (1.135) since the last read |

**MULTIGBASE-T SNR Min Margin Chan D (Register 1.140)**

The Minimum margin channel D register contains a latched copy of the lowest value observed in the SNR operating margin channel D register (1.136) since the last read.

IEEE Standard Register=1.140

**PMA_MGBT_MINMARGIN_D** **Reset Value**

**MULTIGBASE-T SNR Min Margin Chan D (Register 1.140)** **$0000_H$**

| 15 … 0 |
|---|
| **MINMARGIN_D** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| MINMARGIN_D | 15:0 | RO | **MINMARGIN_D**<br>Lowest value observed in the SNR operating margin channel D register (1.136) since the last read |

**MULTIGBASE-T Rx Power Channel A (Register 1.141)**

The RX signal power channel A register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.141

**PMA_MGBT_POWER_A** **Reset Value**

**MULTIGBASE-T Rx Power Channel A (Register 1.141)** **$0000_H$**

| 15 … 0 |
|---|
| **POWER_A** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| POWER_A | 15:0 | RO | **POWER_A**<br>Receive signal power measured at the MDI during training |

**MULTIGBASE-T Rx Power Channel B (Register 1.142)**

The RX signal power channel B register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.142

**PMA_MGBT_POWER_B** **Reset Value**
**MULTIGBASE-T Rx Power Channel B (Register 1.142)** **$0000_H$**

| 15 … 0 |
|---|
| **POWER_B** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| POWER_B | 15:0 | RO | **POWER_B**<br>Receive signal power measured at the MDI during training |

**MULTIGBASE-T Rx Power Chan C (Register 1.143)**

The RX signal power channel C register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.143

**PMA_MGBT_POWER_C** **Reset Value**
**MULTIGBASE-T Rx Power Chan C (Register 1.143)** **$0000_H$**

| 15 … 0 |
|---|
| **POWER_C** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| POWER_C | 15:0 | RO | **POWER_C**<br>Receive signal power measured at the MDI during training |

**MULTIGBASE-T Rx Power Chan D (Register 1.144)**

The RX signal power channel D register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.144

**PMA_MGBT_POWER_D** **Reset Value**
**MULTIGBASE-T Rx Power Chan D (Register 1.144)** **$0000_H$**

| 15–0 |
|---|
| **POWER_D** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| POWER_D | 15:0 | RO | **POWER_D**<br>Receive signal power measured at the MDI during training |

**MULTIGBASE-T skew delay 0 (Register 1.145)**

IEEE Standard Register=1.145

The skew delay reports the current skew delay on each of the pairs with respect to physical pair A. It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number is in two?s complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceeds the maximum amount that can be represented by the range (-80 ns to +78.75 ns), the field displays the maximum value.

**PMA_MGBT_SKEW_DELAY_0** **Reset Value**
**MULTIGBASE-T skew delay 0 (Register 1.145)** **$0000_H$**

| 15 | 14–8 | 7–0 |
|---|---|---|
| **Res** | **SKEW_DELAY_B** | **Res** |
| | ro | |

| Field | Bits | Type | Description |
|---|---|---|---|
| SKEW_DELAY_B | 14:8 | RO | **Skew delay B**<br>Skew delay for pair B |

**MULTIGBASE-T skew delay 1 (Register 1.146)**

IEEE Standard Register=1.146

The skew delay reports the current skew delay on each of the pairs with respect to physical pair A. It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number is in two?s complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceeds the maximum amount that can be represented by the range (-80 ns to +78.75 ns), the field displays the maximum value.

**PMA_MGBT_SKEW_DELAY_1** **Reset Value**
**MULTIGBASE-T skew delay 1 (Register 1.146)** **$0000_H$**

| 15 | 14–8 | 7 | 6–0 |
|---|---|---|---|
| Res | SKEW_DELAY_D | Res | SKEW_DELAY_C |
| | ro | | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| SKEW_DELAY_D | 14:8 | RO | **Skew delay D**<br>Skew delay for pair D |
| SKEW_DELAY_C | 6:0 | RO | **Skew delay C**<br>Skew delay for pair C |

**MULTIGBASE-T skew delay 2 (Register 1.147)**

IEEE Standard Register=1.147

**PMA_MGBT_FAST_RETRAIN_STA_CTRL** **Reset Value**
**MULTIGBASE-T skew delay 2 (Register 1.147)** **$0000_H$**

| 15–11 | 10–6 | 5 | 4 | 3 | 2–1 | 0 |
|---|---|---|---|---|---|---|
| LP_FAST_RETRAIN_COUNT | LD_FAST_RETRAIN_COUNT | Res | FAST_RE* | FAST_RE* | FAST_RETRAIN_SI* | FAST_RE* |
| ro | ro | | ro | ro | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| LP_FAST_RETRAIN_COUNT | 15:11 | RO | **LP fast retrain count**<br>Counts the number of fast retrains requested by the link partner |
| LD_FAST_RETRAIN_COUNT | 10:6 | RO | **LD fast retrain count**<br>Counts the number of fast retrains requested by the local device |
| FAST_RETRAIN_ABILITY | 4 | RO | **Fast retrain ability**<br>1 = Fast retrain capability is supported<br>0 = Fast retrain capability is not supported |
| FAST_RETRAIN_NEGOTIATED | 3 | RO | **Fast retrain negotiated**<br>1 = Fast retrain capability was negotiated<br>0 = Fast retrain capability was not negotiated |
| FAST_RETRAIN_SIG_TYPE | 2:1 | RW | **Fast retrain signal type**<br>11 = Reserved<br>10 = PHY signals Link Interruption during fast retrain<br>01 = PHY signals Local Fault during fast retrain<br>00 = PHY signals IDLE during fast retrain |
| FAST_RETRAIN_ENABLE | 0 | RW | **Fast retrain enable**<br>1 = Fast retrain capability is enabled<br>0 = Fast retrain capability is disabled |

**PMA TimeSync Capability Indication (Register 1.1800)**

PMA TimeSync Capability indication Register.

GPY does not support providing data path delay information.

IEEE Standard Register=1.1800

**PMA_TIMESYNC_CAP** **Reset Value**

**PMA TimeSync Capability Indication (Register 1.1800)** **$0000_H$**

| 15 ... 2 | 1 | 0 |
|---|---|---|
| **Res** | **TXDEL** | **RXDEL** |
| | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| TXDEL | 1 | RO | **Transmit Data Path Delay Information**<br>Not supported by GPY<br>$0_B$ **NONE** PHYs do not have this capability<br>$1_B$ **CAPABLE** min and max TX data path delay available |
| RXDEL | 0 | RO | **Receive Data Path Delay Information**<br>Not supported by GPY<br>$0_B$ **NONE** PHYs do not have this capability<br>$1_B$ **CAPABLE** min and max RX data path delay available |

## 6.2 Standard PCS Registers for MMD=0x03

This section describes the PCS registers for MMD device 0x03.

**Table 22 Registers Overview**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| PCS_CTRL1 | PCS control 1 (Register 3.0) | $205C_H$ |
| PCS_STAT1 | PCS status 1 (Register 3.1) | $0000_H$ |
| PCS_DEVID1 | PHY Identifier 1 (Register 3.2) | $67C9_H$ |
| PCS_DEVID2 | PHY Identifier 2 (Register 3.3) | $DC00_H$ [1)] |
| PCS_SPEED_ABILITY | PCS speed ability (Register 3.4) | $0040_H$ |
| PCS_DIP1 | PCS Devices in package 1 (Register 3.5) | $008B_H$ |
| PCS_DIP2 | PCS Devices in package 2 (Register 3.6) | $C000_H$ |
| PCS_CTRL2 | PCS control 2 (Register 3.7) | $000A_H$ |
| PCS_STAT2 | PCS status 2 (Register 3.8) | $9000_H$ |
| PCS_PACKID1 | PCS package identifier 1 (Register 3.14) | $67C9_H$ |
| PCS_PACKID2 | PCS package identifier 2 (Register 3.15) | $DC00_H$ [1)] |
| PCS_EEE_CAP | PCS EEE capability (Register 3.20) | $0006_H$ |
| PCS_EEE_CAP2 | EEE control and capability 2 (Register 3.21) | $0001_H$ |
| PCS_EEE_WAKERR | PCS EEE Status Register 1 (Register 3.22) | $0000_H$ |
| PCS_2G5_STAT1 | BASE-R and 10GBASE-T PCS status 1 (Register 3.32) | $0000_H$ |
| PCS_2G5_STAT2 | MULTIGBASE-T PCS status 2 (Register 3.33) | $0000_H$ |
| PCS_TIMESYNC_CAP | PCS TimeSync capability register (Register 3.1800) | $0000_H$ |

1) For the device specific reset value, refer to Product Naming table in the **Package Outline** chapter.

### 6.2.1 Standard PCS Registers for MMD=0x03

This chapter describes all registers of PCS in detail.

**PCS control 1 (Register 3.0)**

IEEE Standard Register=3.0

**PCS_CTRL1** **Reset Value**
**PCS control 1 (Register 3.0)** **$205C_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 7 | 6 | 5 2 | 1 0 |
|---|---|---|---|---|---|---|---|---|---|
| RST | LOOP BACK | SSL | Res | LOW_ POW* | RXCK ST | Res | SSM | SPEED_SEL | Res |
| rw | rw | rw | | rw | rw | | rw | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| RST | 15 | RW | **Reset**<br>1 = PCS reset - Self Clearing<br>0 = Normal operation |
| LOOPBACK | 14 | RW | **Loopback**<br>1 = Enable loopback mode<br>0 = Disable loopback mode |
| SSL | 13 | RW | **Forced Speed selection (LSB)**<br>This bit is used in conjunction with SPEED_SEL_LSB<br>MSB LSB<br>1 1 = bits 5:2 select speed<br>1 0 = 1000 Mb/s<br>0 1 = 100 Mb/s<br>0 0 = 10 Mb/s |
| LOW_POWER | 11 | RW | **Low power**<br>1 = Low-power mode<br>0 = Normal operation |
| RXCKST | 10 | RW | **Clock stop enable**<br>1 = The GPY will stop the (X)GMII clock during LPI<br>0 = Clock not stoppable<br>The MAC can set this bit to active to allow the GPY to stop the clocking during the LPI_MODE. |
| SSM | 6 | RW | **Forced Speed selection (MSB)**<br>This bit is used in conjunction with SPEED_SEL_MSB<br>MSB LSB<br>1 1 = bits 5:2 select speed<br>1 0 = 1000 Mb/s<br>0 1 = 100 Mb/s<br>0 0 = 10 Mb/s |
| SPEED_SEL | 5:2 | RW | **Forced Speed selection Values**<br>1 1 x x = Reserved<br>0 1 1 1 = 2.5 Gb/s<br>0 1 0 1 = Reserved<br>0 1 0 0 = Unsupported, defaults to 2.5 Gb/s<br>0 0 1 1 = Unsupported, defaults to 2.5 Gb/s<br>0 0 1 0 = Unsupported, defaults to 2.5 Gb/s<br>0 0 0 1 = Unsupported, defaults to 2.5 Gb/s<br>0 0 0 0 = Unsupported, defaults to 2.5 Gb/s<br>$0111_B$**S2G5** Forced Speed is 2G5 |

**PCS status 1 (Register 3.1)**

IEEE Standard Register=3.1

**PCS_STAT1** **Reset Value**

**PCS status 1 (Register 3.1)** **$0000_H$**

| 15–12 | 11 | 10 | 9 | 8 | 7 | 6 | 5–3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Res | TX_LPI_* | RX_LPI_* | TX_LPI_* | RX_LPI_* | FAULT | TXCKST | Res | PCS_RX_* | LOW_POW* | Res |
| | ro | ro | ro | ro | ro | ro | | ro | ro | |

| Field | Bits | Type | Description |
|---|---|---|---|
| TX_LPI_RXD | 11 | RO | **Tx LPI received**<br>1 = Tx PCS has received LPI<br>0 = LPI not received |
| RX_LPI_RXD | 10 | RO | **Rx LPI received**<br>1 = Rx PCS has received LPI<br>0 = LPI not received |
| TX_LPI_INDICATION | 9 | RO | **Tx LPI indication**<br>1 = Tx PCS is currently receiving LPI<br>0 = PCS is not currently receiving LPI |
| RX_LPI_INDICATION | 8 | RO | **Rx LPI indication**<br>1 = Rx PCS is currently receiving LPI<br>0 = PCS is not currently receiving LPI |
| FAULT | 7 | RO | **Fault**<br>1 = Fault condition detected<br>0 = No fault condition detected |
| TXCKST | 6 | RO | **Clock stop capable**<br>1 = The MAC may stop the clock during LPI<br>0 = Clock not stoppable |
| PCS_RX_LINK_STATUS | 2 | RO | **PCS receive link status**<br>1 = PCS receive link up<br>0 = PCS receive link down |
| LOW_POWER_ABILITY | 1 | RO | **Low-power ability**<br>1 = PCS supports low-power mode<br>0 = PCS does not support low-power mode |

**PHY Identifier 1 (Register 3.2)**

IEEE Standard Register=3.2

| **PCS_DEVID1** | **Reset Value** |
|---|---|
| **PHY Identifier 1 (Register 3.2)** | **67C9$_H$** |

| 15–0 |
|---|
| **OUI** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | Organizationally Unique Identifier Bits 3:18 |

**PHY Identifier 2 (Register 3.3)**

Organizationally Unique Identifier Bits 19:24

IEEE Standard Register=3.3

| **PCS_DEVID2** | **Reset Value** |
|---|---|
| **PHY Identifier 2 (Register 3.3)** | **DC00$_H$** |

| 15–10 | 9–4 | 3–0 |
|---|---|---|
| **OUI** | **LDN** | **LDRN** |
| ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier Bits 19:24** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1] to distinguish between several products. |
| LDRN | 3:0 | RO | **Device Number**<br>Specifies the device revision number[1] to distinguish between several versions of this device |

1) For the device specific reset value, refer to Product Naming table in the **Package Outline** chapter.

**PCS speed ability (Register 3.4)**

IEEE Standard Register=3.4

**PCS_SPEED_ABILITY** **Reset Value**
**PCS speed ability (Register 3.4)** **$0040_H$**

| 15–7 | 6 | 5–4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|
| Res | R2G5_CA* | Res | R100G_C* | R40G_CA* | R10PASS* | R10G_CA* |
| | ro | | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| R2G5_CAPABLE | 6 | RO | **2G5 capable**<br>Bit is always set to 1 because PCS is capable of operating at 2.5 Gb/s |
| R100G_CAPABLE | 3 | RO | **100G capable**<br>1 = PCS is capable of operating at 100 Gb/s<br>0 = PCS is not capable of operating at 100 Gb/s |
| R40G_CAPABLE | 2 | RO | **40G capable**<br>1 = PCS is capable of operating at 40 Gb/s<br>0 = PCS is not capable of operating at 40 Gb/s |
| R10PASS_TS_2BASE_TL | 1 | RO | **10PASS-TS/2BASE-TL Capable**<br>1 = PCS is capable of operating as the 10P/2B PCS<br>0 = PCS is not capable of operating as the 10P/2B PCS |
| R10G_CAPABLE | 0 | RO | **10G capable**<br>1 = PCS is capable of operating at 10 Gb/s<br>0 = PCS is not capable of operating at 10 Gb/s |

**PCS Devices in package 1 (Register 3.5)**

IEEE Standard Register=3.5

**PCS_DIP1** **Reset Value**
**PCS Devices in package 1 (Register 3.5)** **$008B_H$**

| 15–12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | SEPARAT* | SEP_PMA* | SEPARAT* | SEPARAT* | ANEG | TC | DTE_XS | PHY_XS | PCS | WIS_PRE* | PMD_PMA | CL22 |
| ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:12 | RO | **Reserved**<br>Ignore on Read |
| SEPARATED_PMA_4 | 11 | RO | **Separate PMA (4)**<br>1 = Separate PMA (4) present in package |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| SEP_PMA_3 | 10 | RO | **Separate PMA (3)**<br>1 = Separate PMA (3) present in package<br>0 = Separate PMA (3) not present in package |
| SEPARATED_PMA_2 | 9 | RO | **Separate PMA (2)**<br>1 = Separate PMA (2) present in package present<br>0 = Separate PMA (2) not present in package |
| SEPARATED_PMA_1 | 8 | RO | **Separate PMA (1)**<br>1 = Separate PMA (1) present in package present<br>0 = Separate PMA (1) not present in package |
| ANEG | 7 | RO | **Auto-Negotiation present**<br>1 = Auto-Negotiation present in package<br>0 = Auto-Negotiation not present in package |
| TC | 6 | RO | **TC present**<br>1 = TC present in package<br>0 = TC not present in package |
| DTE_XS | 5 | RO | **DTE XS present**<br>1 = DTE XS present in package<br>0 = DTE XS not present in package |
| PHY_XS | 4 | RO | **PHY XS present**<br>1 = PHY XS present in package<br>0 = PHY XS not present in package |
| PCS | 3 | RO | **PCS present**<br>1 = PCS present in package<br>0 = PCS not present in package |
| WIS_PRESENT | 2 | RO | **WIS present**<br>1 = WIS present in package<br>0 = WIS not present in package |
| PMD_PMA | 1 | RO | **PMD/PMA present**<br>1 = PMA/PMD present in package<br>0 = PMA/PMD not present in package |
| CL22 | 0 | RO | **Clause 22 registers present**<br>1 = Clause 22 registers present in package<br>0 = Clause 22 registers not present in package |

**PCS Devices in package 2 (Register 3.6)**

IEEE Standard Register=3.6

**PCS_DIP2** **Reset Value**

**PCS Devices in package 2 (Register 3.6)** **$C000_H$**

| 15 | 14 | 13 | 12 … 0 |
|---|---|---|---|
| **VENDOR_*** | **VENDOR_*** | **CLAUSE_*** | **RES** |
| ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| VENDOR_SPECIFIC_DEVICE_2 | 15 | RO | **Vendor-specific device 2**<br>1 = Vendor-specific device 2 present in package<br>0 = Vendor-specific device 2 not present in package |
| VENDOR_SPECIFIC_DEVICE_1 | 14 | RO | **Vendor-specific device 1**<br>1 = Vendor-specific device 1 present in package<br>0 = Vendor-specific device 1 not present in package |
| CLAUSE_22_EXTENSION | 13 | RO | **Clause 22 extension**<br>1 = Clause 22 extension present in package<br>0 = Clause 22 extension not present in package |
| RES | 12:0 | RO | **Reserved**<br>Ignore on read |

**PCS control 2 (Register 3.7)**

IEEE Standard Register=3.7

**PCS_CTRL2** **Reset Value**
**PCS control 2 (Register 3.7)** **$000A_H$**

| 15 … 4 | 3 … 0 |
|---|---|
| **Res** | **PCS_TYPE_SEL** |
| | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| PCS_TYPE_SEL | 3:0 | RW | **PCS type selection**<br>1 0 1 1 = not supported, defaults to 2.5 Gb/s<br>1 0 1 1 = Select 2.5 Gb/s PCS type ( Default)<br>0 1 0 1 not supported, defaults to 2.5 Gb/s<br>0 1 0 0 not supported, defaults to 2.5 Gb/s<br>0 0 1 1 not supported, defaults to 2.5 Gb/s<br>0 0 1 0 not supported, defaults to 2.5 Gb/s<br>0 0 0 1 not supported, defaults to 2.5 Gb/s<br>0 0 0 0 not supported, defaults to 2.5 Gb/s |

**PCS status 2 (Register 3.8)**

IEEE Standard Register=3.8

**PCS_STAT2** **Reset Value**
**PCS status 2 (Register 3.8)** **$9000_H$**

| 15 14 | 13 | 12 | 11 | 10 | 9 ... 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **DEVICE_PRESENT** | **Res** | **R2G5_CA*** | **TX_FAULT** | **RX_FAULT** | **Res** | **R100GBA*** | **R40GBAS*** | **R10GBAS*** | **R10GBAS*** | **R10GBAS*** | **R10GBAS*** |
| ro | | ro | ro | ro | | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| DEVICE_PRESENT | 15:14 | RO | **Device present**<br>1 0 = Device responding at this address<br>1 1 = No device responding at this address<br>0 1 = No device responding at this address<br>0 0 = No device responding at this address |
| R2G5_CAPABLE | 12 | RO | **2G5BASE-T capable**<br>1 = PCS is able to support 2.5GBASE-T PCS Type<br>0 = Not able to support 2.5GBASE-T |
| TX_FAULT | 11 | RO | **Transmit fault**<br>1 = Fault condition on transmit path<br>0 = No fault condition on transmit path |
| RX_FAULT | 10 | RO | **Receive fault**<br>1 = Fault condition on the receive path<br>0 = No fault condition on the receive path |
| R100GBASE_R_CAPABLE | 5 | RO | **100GBASE-R capable**<br>1 = PCS is able to support 100GBASE-R PCS type<br>0 = PCS is not able to support 100GBASE-R PCS type |
| R40GBASE_R_CAPABLE | 4 | RO | **40GBASE-R capable**<br>1 = PCS is able to support 40GBASE-R PCS type<br>0 = PCS is not able to support 40GBASE-R PCS type |
| R10GBASE_T_CAPABLE | 3 | RO | **10GBASE-T capable**<br>1 = PCS is able to support 10GBASE-T PCS type<br>0 = PCS is not able to support 10GBASE-T PCS type |
| R10GBASE_W_CAPABLE | 2 | RO | **10GBASE-W capable**<br>1 = PCS is able to support 10GBASE-W PCS type<br>0 = PCS is not able to support 10GBASE-W PCS type |
| R10GBASE_X_CAPABLE | 1 | RO | **10GBASE-X capable**<br>1 = PCS is able to support 10GBASE-X PCS type<br>0 = PCS is not able to support 10GBASE-X PCS type |
| R10GBASE_R_CAPABLE | 0 | RO | **10GBASE-R capable**<br>1 = PCS is able to support 10GBASE-R PCS types<br>0 = PCS is not able to support 10GBASE-R PCS types |

**PCS package identifier 1 (Register 3.14)**

IEEE Standard Register=3.14

**PCS_PACKID1** **Reset Value**

**PCS package identifier 1 (Register 3.14)** **$67C9_H$**

| 15 ... 0 |
|---|
| **OUI** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | Organizationally Unique Identifier Bits 3:18 |

**PCS package identifier 2 (Register 3.15)**

IEEE Standard Register=3.15

**PCS_PACKID2** **Reset Value**

**PCS package identifier 2 (Register 3.15)** **$DC00_H$**

| 15 ... 10 | 9 ... 4 | 3 ... 0 |
|---|---|---|
| **OUI** | **LDN** | **LDRN** |
| ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier Bits 19:24** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1] to distinguish between several products. |
| LDRN | 3:0 | RO | **Device Number**<br>Specifies the device revision number[1] to distinguish between several versions of this device |

1) For the device specific reset value, refer to Product Naming table in the **Package Outline** chapter.

### PCS EEE capability (Register 3.20)

IEEE Standard Register=3.20

**PCS_EEE_CAP** — Reset Value

**PCS EEE capability (Register 3.20)** — $0006_H$

| 15–7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | R10GBAS* | R10GBAS* | R1000BA* | R10GBAS* | R1000BA* | R100BAS* | Res |
| | ro | ro | ro | ro | ro | ro | |

| Field | Bits | Type | Description |
|---|---|---|---|
| R10GBASE_KR_EEE | 6 | RO | **10GBASE-KR EEE**<br>1 = EEE is supported for 10GBASE-KR<br>0 = EEE is not supported for 10GBASE-KR |
| R10GBASE_KX4_EEE | 5 | RO | **10GBASE-KX4 EEE**<br>1 = EEE is supported for 10GBASE-KX4<br>0 = EEE is not supported for 10GBASE-KX4 |
| R1000BASE_KX_EEE | 4 | RO | **1000BASE-KX EEE**<br>1 = EEE is supported for 1000BASE-KX<br>0 = EEE is not supported for 1000BASE-KX |
| R10GBASE_T_EEE | 3 | RO | **10GBASE-T EEE**<br>1 = EEE is supported for 10GBASE-T<br>0 = EEE is not supported for 10GBASE-T |
| R1000BASE_T_EEE | 2 | RO | **1000BASE-T EEE**<br>1 = EEE is supported for 1000BASE-T<br>0 = EEE is not supported for 1000BASE-T |
| R100BASE_TX_EEE | 1 | RO | **100BASE-TX EEE**<br>1 = EEE is supported for 100BASE-TX<br>0 = EEE is not supported for 100BASE-TX |

### EEE control and capability 2 (Register 3.21)

Read only, write from STA has no effect

IEEE Standard Register=3.21

**PCS_EEE_CAP2** — Reset Value

**EEE control and capability 2 (Register 3.21)** — $0001_H$

| 15–2 | 1 | 0 |
|---|---|---|
| RES | AB5GEEE | AB2G5EEE |
| ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:2 | RO | **Reserved**<br>Value always 0 |
| AB5GEEE | 1 | RO | **EEE supported for 5GBT**<br>$0_B$ **UNABLE** EEE supported for 5GBT<br>$1_B$ **ABLE** EEE supported for 5GBT |
| AB2G5EEE | 0 | RO | **EEE supported for 2G5BT**<br>$0_B$ **UNABLE** EEE not supported for 2G5BT<br>$1_B$ **ABLE** EEE supported for 2G5BT |

**PCS EEE Status Register 1 (Register 3.22)**

IEEE Standard Register=3.22

**PCS_EEE_WAKERR** **Reset Value**
**PCS EEE Status Register 1 (Register 3.22)** **$0000_H$**

| 15–0 |
|---|
| **ERRCNT** |
| rwsc |

| Field | Bits | Type | Description |
|---|---|---|---|
| ERRCNT | 15:0 | RWSC | **EEE Wake Error Counter**<br>This is a 16-bit saturating counter indicating the number of times the GPY PHY fails to wake up within the EEE time. This counter is cleared upon read from the STA. |

**BASE-R and 10GBASE-T PCS status 1 (Register 3.32)**

IEEE Standard Register=3.32

**PCS_2G5_STAT1** **Reset Value**
**BASE-R and 10GBASE-T PCS status 1 (Register 3.32)** **$0000_H$**

| 15–13 | 12 | 11–4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|
| **Res** | **PCS2 G5_*** | **Res** | **PCS2 G5_*** | **Res** | **PCS2 G5_*** | **PCS2 G5_*** |
| | ro | | ro | | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| PCS2G5_LINK _STATUS | 12 | RO | **BASE-R and 10GBase-T RX Link Status**<br>1 = 2G5 PCS receive link up<br>0 = 2G5 PCS receive link down |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| PCS2G5_PAT_TEST_AB | 3 | RO | **10GBASE-R PRBS9 pattern testing ability**<br>1 = PCS is able to support PRBS9 pattern testing<br>0 = PCS is not able to support PRBS9 pattern testing |
| PCS2G5_HI_BER | 1 | RO | **PCS 2G5 high BER**<br>1 = the 64B/65B receiver is detecting a BER above or equal to 10 ^ -4<br>0 = the 64B/65B receiver is detecting a BER below 10 ^ -4<br>This bit is a direct reflection of the state of the hi_lfer variable in 126.3.6.2.2 for 2.5GBASE-T<br>A latch high view of this status is reflected in MDIO register 3.33.14. |
| PCS2G5_BLO_LOCK | 0 | RO | **PCS 2G5 Block Lock**<br>1 = 64B/65B receiver has block lock<br>0 = 64B/65B receiver has no block lock |

**MULTIGBASE-T PCS status 2 (Register 3.33)**

**PCS_2G5_STAT2** **Reset Value**
**MULTIGBASE-T PCS status 2 (Register 3.33)** **$0000_H$**

| 15 | 14 | 13:8 | 7:0 |
|---|---|---|---|
| **LATCHED*** | **LATCHED*** | **BER** | **ERRED_BLK** |
| rwsc | rwsc | rwsc | rwsc |

| Field | Bits | Type | Description |
|---|---|---|---|
| LATCHED_BLOCK_LOCK | 15 | RWSC | **Latched block lock**<br>1 = PCS 2G5 has block lock<br>0 = PCS 2G5 does not have block lock |
| LATCHED_HIGH_BER | 14 | RWSC | **Latched high BER**<br>1 = PCS 2G5 has reported a high BER<br>0 = PCS 2G5 did not report a high BER |
| BER | 13:8 | RWSC | **BER**<br>BER counter |
| ERRED_BLK | 7:0 | RWSC | **Errored blocks**<br>Errored blocks counter |

**PCS TimeSync capability register (Register 3.1800)**

IEEE Standard Register=3.1800

**PCS_TIMESYNC_CAP** **Reset Value**

**PCS TimeSync capability register (Register 3.1800)** **$0000_H$**

| 15 … 2 | 1 | 0 |
|---|---|---|
| **Res** | **TIMESYN*** | **TIMESYN*** |
| | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| TIMESYNC_TX_PATH_DATA_DELAY | 1 | RO | **TimeSync transmit path data delay**<br>1 = PCS provides information on transmit path data delay in registers 3.1801 through 3.1804<br>0 = PCS does not provide information on transmit path data delay - for GPY, the value is always zero |
| TIMESYNC_RX_PATH_DATA_DELAY | 0 | RO | **TimeSync receive path data delay**<br>1 = PCS provides information on receive path data delay in registers 3.1805 through 3.1808<br>0 = PCS does not provide information on receive path data delay - for GPY, the value is always zero |

## 6.3 Standard Auto-Negotiation Registers for MMD=0x07

This register file contains the auto-negotiation registers for MMD device 0x07.

**Table 23 Registers Overview**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| ANEG_CTRL | Auto-Negotiation Control (Register 7.0) | $3000_H$ |
| ANEG_STAT | Auto-Negotiation Status (Register 7.1) | $0008_H$ |
| ANEG_DEVID1 | PHY Identifier 1 (Register 7.2) | $67C9_H$ |
| ANEG_DEVID2 | PHY Identifier 2 (Register 7.3) | $DC00_H$ 1) |
| ANEG_DIP1 | Device in Package 1 (Register 7.5) | $008B_H$ |
| ANEG_DIP2 | Device in Package 2 (Register 7.6) | $C000_H$ |
| ANEG_PACKID1 | AN package identifier (Register 7.14) | $67C9_H$ |
| ANEG_PACKID2 | AN package identifier (Register 7.15) | $DC00_H$ 1) |
| ANEG_ADV | ANEG Adv. for GPY (Register 7.16) | $91E1_H$ |
| ANEG_LP_BP_AB | AN Link Partner Base Page Ability (Register 7.19) | $01E0_H$ |
| ANEG_XNP_TX1 | ANEG Local Dev XNP TX1 (Register 7.22) | $0000_H$ |
| ANEG_XNP_TX2 | ANEG Local Dev XNP TX2 (Register 7.23) | $0000_H$ |
| ANEG_XNP_TX3 | ANEG Local Dev XNP TX3 (Register 7.24) | $0000_H$ |
| ANEG_LP_XNP_AB1 | ANEG Link Partner XNP RX (Register 7.25) | $0000_H$ |
| ANEG_LP_XNP_AB2 | ANEG Link Partner XNP RX (Register 7.26) | $0000_H$ |
| ANEG_LP_XNP_AB3 | ANEG Link Partner XNP RX (Register 7.27) | $0000_H$ |
| ANEG_MGBT_AN_CTRL | MULTI GBT AN Control Register (Register 7.32) | $00A2_H$ |
| ANEG_MGBT_AN_STA | MultiGBASE-T AN Status register (Register 7.33) | $0000_H$ |
| ANEG_EEE_AN_ADV1 | EEE Advertisement 1 (Register 7.60) | $0006_H$ |
| ANEG_EEE_AN_LPAB1 | EEE Link Partner Ability 1 (Register 7.61) | $0000_H$ |
| ANEG_EEE_AN_ADV2 | EEE Advertisement 2 (Register 7.62) | $0001_H$ |
| ANEG_EEE_LP_AB2 | EEE Link Partner Ability 2 (Register 7.63) | $0001_H$ |
| ANEG_MGBT_AN_CTRL2 | MGBT ANEG Control 2 (Register 7.64) | $0008_H$ |

1) For the device specific reset value, refer to Product Naming table in the **Package Outline** chapter.

### 6.3.1 Standard Auto-Negotiation Registers for MMD=0x07

This chapter describes all registers of ANEG in detail.

**Auto-Negotiation Control (Register 7.0)**

The register controls the main function of Auto-Negotiation as defined in Clause 45. See IEEE 802.3 45.2.7.1.

This register mirrors register STD.CTRL from Clause 22.

IEEE Standard Register=7.0

**ANEG_CTRL** **Reset Value**
**Auto-Negotiation Control (Register 7.0)** **$3000_H$**

| 15 | 14 | 13 | 12 | 11 10 | 9 | 8 … 0 |
|---|---|---|---|---|---|---|
| **RST** | **RES3** | **XNP** | **ANEG _EN*** | **RES2** | **ANEG _RE*** | **RES1** |
| rw | ro | rw | rw | ro | rw | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RST | 15 | RW | **Reset**<br>Resets entire PHY to its default state. Active links are terminated. This is a self-clearing bit: GPY firmware sets it to zero by the hardware after reset is completed.<br>$0_B$ **NORMAL** GPY Normal Operation<br>$1_B$ **RESET** GPY Reset |
| RES3 | 14 | RO | **Reserved**<br>Value always zero, writes ignored. |
| XNP | 13 | RW | **Extended Next Page Control**<br>$0_B$ **ZERO** Extended Next Page is disabled<br>$1_B$ **ONE** Extended Next Page is enabled |
| ANEG_ENAB | 12 | RW | **Auto-Negotiation Enable**<br>Enable the Auto-Negotiation process to determine the link configuration. Bit 7.0.12 is a copy of bit 0.12 in register 0 (STD_CTRL) (see 22.2.4.1.4).<br>$0_B$ **ZERO** disable auto-negotiation process<br>$1_B$ **ONE** enable auto-negotiation process |
| RES2 | 11:10 | RO | **Reserved**<br>Value always zero, writes ignored. |
| ANEG_RESTA RT | 9 | RW | **Restart Auto-Negotiation**<br>The Auto-Negotiation process is restarted by setting bit 7.0.9 to one. Bit 7.0.9 is a mirror of bit 0.9 in register 0 (STD_CTRL) (see IEEE 802.3 22.2.4.1.7).<br>Completion of ANEG is indicated in bit 0.1.5 and 7.1.5.<br>$0_B$ **ZERO** Normal Operation<br>$1_B$ **RESTART** Restart Auto-Negotiation process |
| RES1 | 8:0 | RO | **Reserved**<br>Value always zero, writes ignored |

**Auto-Negotiation Status (Register 7.1)**

All the bits in the ANEG_STA status register are read only, and correspond to the outcome or current status of the Auto-Negotiation process.

IEEE Standard Register=7.1

**ANEG_STAT** — **Reset Value**

**Auto-Negotiation Status (Register 7.1)** — **$0008_H$**

| 15:10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| **RES3** | **PDF** | **RES2** | **XNPS** | **PR** | **ANEG_CO*** | **ANEG_RF** | **ANEG_AB*** | **LINKSTA** | **RES1** | **LP_ANEG*** |
| ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES3 | 15:10 | RO | **Reserved**<br>Value always zero, writes ignored. |
| PDF | 9 | RO | **Parallel detection fault**<br>$0_B$ **NOFAULT** No fault was detected.<br>$1_B$ **FAULT** Fault is detected via the parallel detection |
| RES2 | 8 | RO | **Reserved**<br>Value always zero, writes ignored |
| XNPS | 7 | RO | **Extended Next Page Status**<br>When set to 1, bit 7.1.7 indicates that both the GPY and the link partner have indicated support for Extended Next Page. When set to 0, bit 7.1.7 indicates that Extended Next Page will not be used.<br>$0_B$ **ZERO** Extended Next Page is not allowed.<br>$1_B$ **ONE** Extended Next Page format is used. |
| PR | 6 | RO | **Page Received**<br>The page received bit (7.1.6) is set to 1 to indicate that a new link codeword has been received and stored in the AN LP Base Page ability registers 7.19 or AN LP XNP ability registers 7.25 to 7.27.<br>$0_B$ **ZERO** A page has not been received<br>$1_B$ **ONE** A page has been received |
| ANEG_COMPLETE | 5 | RO | **Auto-Negotiation Complete**<br>When read as a 1, bit 7.1.5 indicates that the Auto-Negotiation process has been completed, and that the contents of the Auto-Negotiation registers 7.16 and 7.19 are valid. When read as a zero, bit 7.1.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of 7.19, 7.22 through 7.27, and 7.33 registers are as defined by the current state of the Auto-Negotiation protocol, or as written by manual configuration.<br>$0_B$ **ZERO** Auto-Negotiation process has not completed<br>$1_B$ **ONE** Auto-Negotiation process has completed |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| ANEG_RF | 4 | RO | **Remote Fault**<br>When read as one, bit 7.1.4 indicates that a remote fault condition has been detected. Bit 7.1.4 is a copy of bit 1.4 in register 1, device 0 (see 22.2.4).<br>$0_B$ **NORMAL** No remote fault condition detected<br>$1_B$ **FAULT** Remote fault condition detected |
| ANEG_ABLE | 3 | RO | **Auto-Negotiation Ability**<br>Bit 7.1.3 is a copy of bit 1.3 in register 1 (see 22.2.4). This is the ANEG ability of the GPY.<br>$0_B$ **UNABLE** PHY is not able to perform Auto-Negotiation<br>$1_B$ **ABLE** PHY is able to perform Auto-Negotiation |
| LINKSTA | 2 | RO | **Link Status**<br>When read as a one, bit 7.1.2 indicates that the PMA/PMD has determined that a valid link has been established. This bit is a duplicate of the PMA/PMD link status bit in 1.1.2. This bit latches low, so does not represent the current status but can be used to indicate link drop since the last read from the management interface. Reading this bit from MDIO resets the bit to the current value of the link.<br>$0_B$ **DOWN** Link is down<br>$1_B$ **UP** Link is Up |
| RES1 | 1 | RO | **Value always zero, write ignored** |
| LP_ANEG_ABLE | 0 | RO | **Link partner auto-negotiation ability**<br>$0_B$ **UNABLE** Link partner is not capable of auto-negotiation.<br>$1_B$ **ABLE** Link partner is capable of auto-negotiation |

**PHY Identifier 1 (Register 7.2)**

**ANEG_DEVID1** **Reset Value**
**PHY Identifier 1 (Register 7.2)** **67C9$_H$**

| 15 ... 0 |
|---|
| **OUI** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | **Organizationally Unique Identifier** |

**PHY Identifier 2 (Register 7.3)**

Organizationally Unique Identifier

IEEE Standard Register=7.3

**ANEG_DEVID2** **Reset Value**

**PHY Identifier 2 (Register 7.3)** **DC00$_H$**

| 15 … 10 | 9 … 4 | 3 … 0 |
|---|---|---|
| **OUI** | **LDN** | **LDRN** |
| ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1] to distinguish between several products. |
| LDRN | 3:0 | RO | **Device Number**<br>Specifies the device revision number[1] to distinguish between several versions of this device |

1) For the device specific reset value, refer to Product Naming table in the **Package Outline** chapter.

**Device in Package 1 (Register 7.5)**

IEEE Standard Register=7.5

**ANEG_DIP1** **Reset Value**

**Device in Package 1 (Register 7.5)** **008B$_H$**

| 15 … 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **RES** | **PMA4** | **PMA3** | **PMA2** | **PMA1** | **ANEG** | **TC** | **DTEXS** | **PHYXS** | **PCS** | **WIS** | **PMAPMD** | **CL22** |
| ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:12 | RO | **Reserved**<br>Ignore on Read |
| PMA4 | 11 | RO | **Separate PMA4 present in package**<br>$0_B$ **ABSENT** Separate PMA4 not present in package<br>$1_B$ **PRESENT** Separate PMA4 present in package |
| PMA3 | 10 | RO | **Separate PMA3 present in package**<br>$0_B$ **ABSENT** Separate PMA3 not present in package<br>$1_B$ **PRESENT** Separate PMA3 present in package |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| PMA2 | 9 | RO | **Separate PMA2 present in package**<br>$0_B$ **ABSENT** Separate PMA2 not present in package<br>$1_B$ **PRESENT** Separate PMA2 present in package |
| PMA1 | 8 | RO | **Separate PMA1 present in package**<br>$0_B$ **ABSENT** Separate PMA1 not present inn package<br>$1_B$ **PRESENT** Separate PMA1 present in package |
| ANEG | 7 | RO | **Auto-negotiation present in package**<br>$0_B$ **ABSENT** ANEG not present inn package<br>$1_B$ **PRESENT** ANEG present in package |
| TC | 6 | RO | **TC present in package**<br>$0_B$ **ABSENT** TC registers not present in package<br>$1_B$ **PRESENT** TC registers present in package |
| DTEXS | 5 | RO | **DTE XS present in package**<br>$0_B$ **ABSENT** DTE XS registers not present in package<br>$1_B$ **PRESENT** DTE XS registers present in package |
| PHYXS | 4 | RO | **PHYXS present in package**<br>$0_B$ **ABSENT** PHYXS registers not present in package<br>$1_B$ **PRESENT** PHYXS registers present in package |
| PCS | 3 | RO | **PCS present in package**<br>$0_B$ **ABSENT** PCS registers not present in package<br>$1_B$ **PRESENT** PCS registers present in package |
| WIS | 2 | RO | **WIS present in package**<br>$0_B$ **ABSENT** WIS registers present in package<br>$1_B$ **PRESENT** WIS registers present in package |
| PMAPMD | 1 | RO | **PMA PMD presence in package**<br>$0_B$ **ABSENT** PMA PMD registers not present in package<br>$1_B$ **PRESENT** PMA PMD registers present in package |
| CL22 | 0 | RO | **Clause 22 register present in package**<br>$0_B$ **ABSENT** Clause 22 registers no present in package<br>$1_B$ **PRESENT** Clause 22 registers present in package |

**Device in Package 2 (Register 7.6)**

IEEE Standard Register=7.6

**ANEG_DIP2** — **Reset Value**

**Device in Package 2 (Register 7.6)** — **$C000_H$**

| 15 | 14 | 13 | 12 … 0 |
|---|---|---|---|
| **VSPEC2** | **VSPEC1** | **CL22EXT** | **RES** |
| ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| VSPEC2 | 15 | RO | **Vendor Specific Device 2 present in package**<br>$0_B$ **ABSENT** Vendor Specific Device 2 not present in package<br>$1_B$ **PRESENT** Vendor Specific Device 2 present in package |
| VSPEC1 | 14 | RO | **Vendor Specific Device 1 present in package**<br>$0_B$ **ABSENT** Vendor Specific Device 1 not present in package<br>$1_B$ **PRESENT** Vendor Specific Device 1 present in package |
| CL22EXT | 13 | RO | **Clause 22 extension present in package**<br>$0_B$ **ABSENT** Clause 22 extension not present in package<br>$1_B$ **PRESENT** Clause 22 extension present in package |
| RES | 12:0 | RO | **Reserved**<br>Ignore on read |

**AN package identifier (Register 7.14)**

IEEE Standard Register=7.14

**ANEG_PACKID1** **Reset Value**
**AN package identifier (Register 7.14)** **$67C9_H$**

| 15 … 0 |
|---|
| **OUI** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | **Organizationally Unique Identifier**<br>Organizationally Unique Identifier Bits 3:18 |

**AN package identifier (Register 7.15)**

IEEE Standard Register=7.15

**ANEG_PACKID2** **Reset Value**
**AN package identifier (Register 7.15)** **$DC00_H$**

| 15 … 10 | 9 … 4 | 3 … 0 |
|---|---|---|
| **OUI** | **LDN** | **LDRN** |
| ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier Bits 19:24** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1)] to distinguish between several products. |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| LDRN | 3:0 | RO | **Device Number**<br>Specifies the device revision number[1] to distinguish between several versions of this device |

1) For the device specific reset value, refer to Product Naming table in the **Package Outline** chapter.

### ANEG Adv. for GPY (Register 7.16)

This register is a copy of the Auto-Negotiation advertisement register (Register 4). A read to the AN advertisement register (7.16) reports the value of the Auto-Negotiation advertisement register (Register 4); writes to the AN advertisement register (7.16) cause a write to occur to the Auto-Negotiation advertisement register (Register 4).

IEEE Standard Register=7.16

**ANEG_ADV** — **Reset Value**
**ANEG Adv. for GPY (Register 7.16)** — **$91E1_H$**

| 15 | 14 | 13 | 12 | 11 … 5 | 4 … 0 |
|---|---|---|---|---|---|
| **NP** | **RES** | **RF** | **XNP** | **TAF** | **SF** |
| rw | ro | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RW | **Next Page Able**<br>$0_B$ **INACTIVE** No Next page allowed<br>$1_B$ **ACTIVE** Additional Next Page will follow. |
| RES | 14 | RO | **Reserved**<br>Write as zero, ignore on read. |
| RF | 13 | RW | **Remote Fault**<br>The remote fault bit allows indication of a fault to the link partner. See IEEE 802.3 28.2.1.2.4. |
| XNP | 12 | RW | **Indicates that GPY supports transmission of Extended Next Pages**<br>$0_B$ **UNABLE** GPY is XNP unable<br>$1_B$ **ABLE** GPY is XNP able |
| TAF | 11:5 | RW | **Technology Ability Field**<br>The technology ability field is an 8-bit wide field containing information indicating supported technologies. GPY supports 10BASE-T (Half and Full Duplex), 100BASE-TX (Half and Full Duplex) and both symmetric and asymmetric PAUSE.<br>$40_H$ **PS_ASYM** Advertise asymmetric pause<br>$20_H$ **PS_SYM** Advertise symmetric pause<br>$10_H$ **DBT4** Advertise 100BASE-T4<br>$08_H$ **DBT_FDX** Advertise 100BASE-TX full duplex<br>$04_H$ **DBT_HDX** Advertise 100BASE-TX half duplex<br>$02_H$ **XBT_FDX** Advertise 10BASE-T full duplex<br>$01_H$ **XBT_HDX** Advertise 10BASE-T half duplex |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| SF | 4:0 | RW | **Selector Field**<br>This field is always set to 1 because GPY only supports 802.3 Ethernet standard.<br>$00001_B$**IEEE8023** IEEE802.3Select the IEEE 802.3 technology |

### AN Link Partner Base Page Ability (Register 7.19)

Register 7.19 is a copy of register 5 from Clause 28. It contains the Base Page received from the link partner. All of the bits in the AN LP Base Page ability register are read only.

IEEE Standard Register=7.19

**ANEG_LP_BP_AB** — **Reset Value**

**AN Link Partner Base Page Ability (Register 7.19)** — **$01E0_H$**

| 15 | 14 | 13 | 12 | 11 … 5 | 4 … 0 |
|---|---|---|---|---|---|
| **NP** | **ACK** | **RF** | **XNP** | **TAF** | **SF** |
| ro | ro | ro | ro | rw | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RO | **Link Partner Next Page**<br>Next page request indication from the link partner. See IEEE 802.3 28.2.1.2.6.<br>$0_B$ **INACTIVE** No Next Page to Follow<br>$1_B$ **ACTIVE** Additional Next Page will follow |
| ACK | 14 | RO | **Link Partner Acknowledge**<br>Acknowledgement indication from the link partner's link code word. See IEEE 802.3 28.2.1.2.5.<br>$0_B$ **INACTIVE** Device did not successfully receive its Link Partner's LCW<br>$1_B$ **ACTIVE** The device has successfully received its link partner's link code word |
| RF | 13 | RO | **Link Partner Remote Fault**<br>Remote fault indication from the link partner. See IEEE 802.3 28.2.1.2.4.<br>$0_B$ **NONE** Remote fault is not indicated by the link partner<br>$1_B$ **FAULT** Remote fault is indicated by the link partner |
| XNP | 12 | RO | **Link Partner XNP Ability**<br>$0_B$ **UNABLE** Link Partner is not XNP able<br>$1_B$ **ABLE** Link Partner is XNP able |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| TAF | 11:5 | RW | **Technology Ability Field**<br>Indicate the link partner's supported technologies received in base page.<br>$40_H$ **PS_ASYM** Advertise asymmetric pause<br>$20_H$ **PS_SYM** Advertise symmetric pause<br>$10_H$ **DBT4** Advertise 100BASE-T4<br>$08_H$ **DBT_FDX** Advertise 100BASE-TX full duplex<br>$04_H$ **DBT_HDX** Advertise 100BASE-TX half duplex<br>$02_H$ **XBT_FDX** Advertise 10BASE-T full duplex<br>$01_H$ **XBT_HDX** Advertise 10BASE-T half duplex |
| SF | 4:0 | RO | **Link Partner Selector Field**<br>The selector field represents one of the 32 possible messages with encoding definitions shown in IEEE 802.3 Annex 28A.<br>0x00 = Reserved<br>0x01 = IEEE 802.3<br>0x02 = IEEE 802.9 ISLAN-16T<br>0x03 = IEEE 802.5<br>0x04 = IEEE 1394<br>0x05 -> 0x1F = Reserve<br>$00001_B$**IEEE8023** IEEE802.3Select the IEEE802.3 technology |

**ANEG Local Dev XNP TX1 (Register 7.22)**

**ANEG_XNP_TX1** **Reset Value**
**ANEG Local Dev XNP TX1 (Register 7.22)** **$0000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 … 0 |
|---|---|---|---|---|---|
| NP | RES | MP | ACK2 | TOGG | MCF |
| rw | ro | rw | rw | ro | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RW | **Next Page**<br>When NP bit is set, the GPY requests to transmit one additional page. Next Page transmission ends when both ends of a link segment set their Next Page bits to logic zero, indicating that neither has anything additional to transmit. See IEEE 802.3 28.2.3.4.<br>$0_B$ **INACTIVE** No Next Page to Follow<br>$1_B$ **ACTIVE** Additional next page(s) will follow |
| RES | 14 | RO | **Reserved**<br>Write as zero, ignore on read. |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| MP | 13 | RW | **Message Page**<br>Message Page (MP) is used by the Next Page function to differentiate a Message Page from an Unformatted Page. Only message pages are used by GPY.<br>$0_B$ **UNFOR** Unformatted Page<br>$1_B$ **MESSG** Message Page |
| ACK2 | 12 | RW | **Acknowledge 2**<br>Not used during GPY auto negotiation.<br>$0_B$ **INACTIVE** Device cannot comply with message<br>$1_B$ **ACTIVE** Device will comply with message |
| TOGG | 11 | RO | **Toggle**<br>The Toggle bit is used to ensure proper synchronization between the GPY and the Link Partner. See IEEE 802.3 28.2.3.4.<br>$0_B$ **ZERO** Previous value of the Tx LCW was ONE<br>$1_B$ **ONE** Previous value of the Tx LCW was ZERO |
| MCF | 10:0 | RW | **Message Code Field**<br>When Message Page bit is set to 1 (7.16.1), this field is the Message Code Field of a message page used in Next Page exchange. The message codes are described in IEEE802.3 Appendix 28C.<br>It is used to indicate the type of message in UCF1 and UCF2.<br>0x0 = Reserved<br>0x1 = Null message<br>0x2 = One Unformated Page (UP) with TAF follows<br>0x3 = Two UPs with TAF follows<br>0x4 = Remote fault details message<br>0x5 = OUI message<br>0x6 = PHY ID message<br>0x7 = 100BASE-T2 message<br>0x8 = 1000BASE-T message<br>0x9 = MULTIGBASE-T message<br>0xA = EEE technology capability follows in next UP<br>0xB = OUI XNP |

**ANEG Local Dev XNP TX2 (Register 7.23)**

Unformatted Code field 1 contains Seed information and advertises support of 1GBT full duplex and half duplex. See 28.2.3.4

IEEE Standard Register=7.23

**ANEG_XNP_TX2** **Reset Value**
**ANEG Local Dev XNP TX2 (Register 7.23)** **$0000_H$**

| 15 … 0 |
|---|
| **UCF1** |
| rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| UCF1 | 15:0 | RW | **Unformatted Code Field 1**<br>Transmits Master-Slave Seed bit to facilitate Auto-negotiation resolution, port type and duplex capability. |

**ANEG Local Dev XNP TX3 (Register 7.24)**

Unformatted Code field 2 - Register 7.24

See 28.2.3.4

IEEE Standard Register=7.24

**ANEG_XNP_TX3** **Reset Value**
**ANEG Local Dev XNP TX3 (Register 7.24)** **$0000_H$**

| 15 ... 0 |
|---|
| **UCF2** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| UCF2 | 15:0 | RO | **Unformatted Code Field 2**<br>2.5 GBASE-T ability is advertised by default |

**ANEG Link Partner XNP RX (Register 7.25)**

IEEE Standard Register=7.25

**ANEG_LP_XNP_AB1** **Reset Value**
**ANEG Link Partner XNP RX (Register 7.25)** **$0000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 ... 0 |
|---|---|---|---|---|---|
| **NP** | **ACK** | **MP** | **ACK2** | **TOGG** | **MCF** |
| ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RO | **Link Partner Next Page**<br>See 28.2.3.4.3<br>Next Page (NP) is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted.<br>$0_B$ **INACTIVE** Last Page<br>$1_B$ **ACTIVE** Additional next page(s) will follow |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| ACK | 14 | RO | **Link Partner Acknowledge**<br>As defined in 28.2.1.2.5.<br>Acknowledge (Ack) is used by the Auto-Negotiation function to indicate that GPY has successfully received its Link Partner's link codeword. |
| MP | 13 | RO | **Link Partner Message Page**<br>Indicates that the content of MCF is either an unformatted page or a formatted message. See IEEE 802.3 28.2.3.4.<br>$0_B$ **UNFOR** Unformatted Page<br>$1_B$ **MESSG** Message Page |
| ACK2 | 12 | RO | **Link Partner Acknowledge 2**<br>See IEEE 802.3 28.2.3.4.<br>$0_B$ **INACTIVE** Device cannot comply with message<br>$1_B$ **ACTIVE** Device will comply with message |
| TOGG | 11 | RO | **Link Partner Toggle**<br>See IEEE 802.3 28.2.3.4.<br>Set to the opposite of TOGG bit in previous page.<br>$0_B$ **ZERO** Previous value of the TX LCW was ONE<br>$1_B$ **ONE** Previous value of the TX LCW was ZERO |
| MCF | 10:0 | RO | **Link Partner Message Code Field**<br>Indicate the type of Message Code. See IEEE802.3 28.2.3.4<br>$009_H$ **MC_2G5BT** Message Code for 2G5BT |

**ANEG Link Partner XNP RX (Register 7.26)**

IEEE Standard Register=7.26

**ANEG_LP_XNP_AB2** **Reset Value**
**ANEG Link Partner XNP RX (Register 7.26)** **$0000_H$**

| 15 … 0 |
|---|
| **UCF1** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| UCF1 | 15:0 | RO | **Unformatted Code Field 1**<br>See 28.2.3.4 |

### ANEG Link Partner XNP RX (Register 7.27)

IEEE Standard Register=7.27

**ANEG_LP_XNP_AB3** — **Reset Value**
**ANEG Link Partner XNP RX (Register 7.27)** — **0000$_H$**

| 15 … 0 |
|---|
| **UCF2** |
| ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| UCF2 | 15:0 | RO | **Unformatted Code Field 2**<br>See 28.2.3.4 |

### MULTI GBT AN Control Register (Register 7.32)

Advertise the GPY Capabilities

IEEE Standard Register=7.32

**ANEG_MGBT_AN_CTRL** — **Reset Value**
**MULTI GBT AN Control Register (Register 7.32)** — **00A2$_H$**

| 15 | 14 | 13 | 12 | 11:9 | 8 | 7 | 6 | 5 | 4:3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **MS_MAN_*** | **MSCV** | **PT** | **AB_10GBT** | **RES2** | **AB_5GBT** | **AB_2G5BT** | **FR_5GBT** | **FR_2G5BT** | **RES1** | **LDPMA** | **FR** | **LDL** |
| rw | rw | rw | ro | ro | ro | rw | ro | rw | ro | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| MS_MAN_EN | 15 | RW | **Master Slave Config Manual Config Enable**<br>$0_B$ **ANEG** ANEG is used to determine Master-Slave selection<br>$1_B$ **MAN** Manual Config, MSCV bit determines Master-Slave |
| MSCV | 14 | RW | **Master Slave Config Value**<br>$0_B$ **SLAVE** Manual set to SLAVE<br>$1_B$ **MASTER** Manual set to MASTER |
| PT | 13 | RW | **Port Type**<br>$0_B$ **MASTER** Preference as Master - Single Port Device<br>$1_B$ **SLAVE** Preference as Slave - Multiport Device |
| AB_10GBT | 12 | RO | **10GBASE-T Ability**<br>Not Supported - always 0 |
| RES2 | 11:9 | RO | **Reserved**<br>Value always zero, writes ignored. |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| AB_5GBT | 8 | RO | **5GBASE-T ability**<br>Not supported by GPY<br>$0_B$ **UNABLE** Do not Advertise PHY as 5GBASE-T capable<br>$1_B$ **ABLE** Advertise PHY as 5GBASE-T capableNot supported |
| AB_2G5BT | 7 | RW | **2.5 G BASE-T ability**<br>$0_B$ **UNABLE** Do not Advertise PHY as 2.5GBASE-T capable<br>$1_B$ **ABLE** Advertise PHY as 2.5GBASE-T capable |
| FR_5GBT | 6 | RO | **5 G BASE-T Fast Retrain Ability**<br>Not supported by GPY. See 45.2.7.10 bz<br>$0_B$ **UNABLE** Do not Advertise PHY as 5GBT Fast retrain able<br>$1_B$ **ABLE** Advertise PHY as 5GBASE-T Fast Retrain capableNot supported |
| FR_2G5BT | 5 | RW | **2.5 G BASE-T Fast Retrain Ability**<br>$0_B$ **UNABLE** Do not Advertise PHY as 2.5G Fast Retrain Able<br>$1_B$ **ABLE** Advertise PHY as 2.5G Fast retrain able |
| RES1 | 4:3 | RO | **Reserved**<br>Value always zero, writes ignored. |
| LDPMA | 2 | RW | **GPY PMA training reset request**<br>If set to one the GPY expects the link partner to reset the PMA training PRBS for every PMA training frame.<br>If bit is zero then the GPY expects link partner to run PMA training PRBS continuously through every PMA training frame |
| FR | 1 | RW | **Fast Retrain Ability** |
| LDL | 0 | RW | **GPY Loop Timing Ability** |

**MultiGBASE-T AN Status register (Register 7.33)**

IEEE Standard Register=7.33

**ANEG_MGBT_AN_STA** **Reset Value**
**MultiGBASE-T AN Status register (Register 7.33)** **$0000_H$**

| 15–7 | 6 | 5 | 4 | 3 | 2–0 |
|---|---|---|---|---|---|
| **Res** | **AB_5GBT** | **AB_2G5BT** | **FR_5GBT** | **FR_2G5BT** | **Res** |
| | ro | ro | ro | ro | |

| Field | Bits | Type | Description |
|---|---|---|---|
| AB_5GBT | 6 | RO | **5G BASE-T Ability of Link Partner**<br>This bit is only valid after link is established and ANEG completed.<br>$0_B$ **UNABLE** Link partner is not capable of 5GBASE-T<br>$1_B$ **ABLE** Link partner is capable of 5GBASE-T |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| AB_2G5BT | 5 | RO | **2.5 G BASE-T Ability of Link Partner**<br>This bit is only valid after link is established and ANEG completed ( bit 7.1.5 is set to 1).<br>$0_B$ **UNABLE** Link partner is not capable of 2.5GBASE-T<br>$1_B$ **ABLE** Link partner is capable of 2.5GBASE-T |
| FR_5GBT | 4 | RO | **5 G BASE-T Fast Retrain Ability of Link Partner**<br>This bit is only valid after link is established and ANEG completed.<br>$0_B$ **UNABLE** Link partner is not capable of 5GBT fast retrain<br>$1_B$ **ABLE** Link partner is capable of 5GBASE-T fast retrain |
| FR_2G5BT | 3 | RO | **2.5 G BASE-T Fast Retrain Ability of Link Partner**<br>This bit is only valid after link is established and ANEG completed ( bit 7.1.5 is set to 1).<br>$0_B$ **UNABLE** Link partner is not capable of 2.5GBT fast retrain<br>$1_B$ **ABLE** Link partner is capable of 2.5GBASE-T fast retrain |

**EEE Advertisement 1 (Register 7.60)**

IEEE Standard Register=7.60

**ANEG_EEE_AN_ADV1** **Reset Value**
**EEE Advertisement 1 (Register 7.60)** **$0006_H$**

| 15 … 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **Res** | **EEE_10G*** | **EEE_10G*** | **EEE_100*** | **EEE_10G*** | **EEE_100*** | **EEE_100*** | **Res** |
| | ro | ro | ro | ro | rw | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| EEE_10GBKR | 6 | RO | **Support of 10GBASE-KR EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE<br>$1_B$ **ENABLE** This PHY mode is supported for EEE |
| EEE_10GBKX4 | 5 | RO | **Support of 10GBASE-KX4 EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE<br>$1_B$ **ENABLE** This PHY mode is supported for EEE |
| EEE_1000BKX | 4 | RO | **Support of 1000BASE-KX EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE<br>$1_B$ **ENABLE** This PHY mode is supported for EEE |
| EEE_10GBT | 3 | RO | **Support of 10GBASE-T EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE<br>$1_B$ **ENABLE** This PHY mode is supported for EEE |
| EEE_1000BT | 2 | RW | **Support of 1000BASE-T EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE<br>$1_B$ **ENABLE** This PHY mode is supported for EEE |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| EEE_100BTX | 1 | RW | **Support of 100BASE-TX EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE<br>$1_B$ **ENABLE** This PHY mode is supported for EEE |

**EEE Link Partner Ability 1 (Register 7.61)**

After the AN process is completed, this register reflects the contents of the link partner's EEE advertisement register. The definitions are the same as for the EEE AN advertisement 1 register.

IEEE Standard Register=7.61

All of the bits in the EEE LP ability 1 register are read only. A write operation to the EEE LP advertisement register has no effect.

**ANEG_EEE_AN_LPAB1** — **Reset Value**
**EEE Link Partner Ability 1 (Register 7.61)** — **$0000_H$**

| 15–7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **Res** | **EEE_10G*** | **EEE_10G*** | **EEE_100*** | **EEE_10G*** | **EEE_100*** | **EEE_100*** | **Res** |
| | ro | ro | ro | ro | ro | ro | |

| Field | Bits | Type | Description |
|---|---|---|---|
| EEE_10GBKR | 6 | RO | **Support of 10GBASE-KR EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE<br>$1_B$ **ENABLE** This PHY mode is supported for EEE |
| EEE_10GBKX4 | 5 | RO | **Support of 10GBASE-KX4 EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE<br>$1_B$ **ENABLE** This PHY mode is supported for EEE |
| EEE_1000BKX | 4 | RO | **Support of 1000BASE-KX EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE<br>$1_B$ **ENABLE** This PHY mode is supported for EEE |
| EEE_10GBT | 3 | RO | **Support of 10GBASE-T EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE<br>$1_B$ **ENABLE** This PHY mode is supported for EEE |
| EEE_1000BT | 2 | RO | **Support of 1000BASE-T EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE<br>$1_B$ **ENABLE** This PHY mode is supported for EEE |
| EEE_100BTX | 1 | RO | **Support of 100BASE-TX EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE<br>$1_B$ **ENABLE** This PHY mode is supported for EEE |

**EEE Advertisement 2 (Register 7.62)**

EEE advertisement 2 register is a continuation of EEE advertisement 1 register.

IEEE Standard Register=7.62

**ANEG_EEE_AN_ADV2** — **Reset Value**

**EEE Advertisement 2 (Register 7.62)** — **$0001_H$**

| 15 … 1 | 0 |
|---|---|
| **RES** | **EEE2G5** |
| ro | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:1 | RO | **Reserved** |
| EEE2G5 | 0 | RW | **Advertise 2G5BT EEE capability**<br>$0_B$ **DISABLED** This PHY mode does not advertise 2G5BT EEE<br>$1_B$ **ENABLE** This PHY mode does advertise 2G5BT EEE |

**EEE Link Partner Ability 2 (Register 7.63)**

When the AN and training processes is completed, this register reflects the contents of the link partner's EEE advertisement 2 register.

IEEE Standard Register=7.63

All of the bits in the EEE LP ability 2 register are read-only. A write to the EEE LP ability 2 register will have no effect.

**ANEG_EEE_LP_AB2** — **Reset Value**

**EEE Link Partner Ability 2 (Register 7.63)** — **$0001_H$**

| 15 … 1 | 0 |
|---|---|
| **RES** | **EEE2G5** |
| ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:1 | RO | **Reserved** |
| EEE2G5 | 0 | RO | **Link Partner advertised 2G5BT EEE capability**<br>$0_B$ **DISABLED** LP not 2G5BT EEE capable<br>$1_B$ **ENABLE** LP 2G5BT EEE capable |

**MGBT ANEG Control 2 (Register 7.64)**

This register is an extension of ANEG Control Register for Multi GBT. Used for 2.5 G ANEG configuration.

IEEE Standard Register=7.64

Bit 7.64.3 is valid only if 7.32.5 is set to one advertising fast retrain ability, and is used to request the link partner whether to initially reset the THP during fast retrain. THP Bypass Request is exchanged during link training, see 126.4.2.5.10. If bit 7.64.3 is set to zero the GPY requests link partner not to reset THP during fast retrain. If bit 7.64.3 is set to one the GPY requests link partner to initially reset THP during fast retrain.

**ANEG_MGBT_AN_CTRL2** — **Reset Value**

**MGBT ANEG Control 2 (Register 7.64)** — **$0008_H$**

| 15 | 14 ... 4 | 3 | 2 ... 0 |
|---|---|---|---|
| **Res** | **RES** | **THPBYP2*** | **Res** |
| | ro | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 14:4 | RO | **Reserved** |
| THPBYP2G5 | 3 | RW | **GPY Requests a THP bypass during fast retrain.**<br>$0_B$ **NORST** GPY requests partner NOT to initially reset THP during fast retrain<br>$1_B$ **RST** GPY requests partner to initially reset THP during fast retrain |

## 6.4 Vendor Specific 1 Device for MMD=0x1E

This register file contains GPY specific register for MMD=30 (decimal)

**Table 24 Registers Overview**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| VSPEC1_LED0 | Configuration for LED Pin 0 (Register 30.1) | $0310_H$ |
| VSPEC1_LED1 | Configuration for LED Pin 1 (Register 30.2) | $0320_H$ |
| VSPEC1_LED2 | Configuration for LED Pin 2 (Register 30.3) | $0340_H$ |
| VSPEC1_LED3 | Configuration for LED Pin 3 (Register 30.4) | $0380_H$ |
| VSPEC1_SGMII_CTRL | Chip Level SGMII control register (Register 30.8) | $34DA_H$ |
| VSPEC1_SGMII_STAT | Chip Level SGMII status register (Register 30.9) | $8008_H$ |
| VSPEC1_NBT_DS_CTRL | NBASE-T Downshift Control Register (Register 30.10) | $0400_H$ |
| VSPEC1_NBT_DS_STA | NBASE-T Downshift Status Register (Register 30.11) | $0000_H$ |
| VSPEC1_PM_CTRL | Packet Manager Control (Register 30.12) | $0003_H$ |
| VSPEC1_TEMP_STA | Temperature code (Register 30.14) | $0000_H$ |
| VSPEC1_IMASK | MACSec Interrupt Mask Register (Register 30.17) | $0000_H$ |
| VSPEC1_ISTAT | MACSec Interrupt Mask Register (Register 30.18) | $0000_H$ |
| VSPEC1_LANE_ASP_MAP | ASP Mapping to Physical Lanes(Register 30.20) | $00E4_H$ |

### 6.4.1 Vendor Specific 1 Device for MMD=0x1E

This chapter describes all registers of VSPEC1 in detail.

**Configuration for LED Pin 0 (Register 30.1)**

This register configures the behavior of the LED0 depending on pre-defined states or events the PHY has entered into or raised. Since more than one event/state can be active at the same time, more than one function might apply simultaneously. The priority from highest to lowest is given by the order PULSE, BLINKS, BLINKF, CON.

IEEE Standard Register=30.1

**VSPEC1_LED0** **Reset Value**
**Configuration for LED Pin 0 (Register 30.1)** **$0310_H$**

| 15 … 12 | 11 … 8 | 7 … 4 | 3 … 0 |
|---|---|---|---|
| **BLINKS** | **PULSE** | **CON** | **BLINKF** |
| rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| BLINKS | 15:12 | RW | **Slow Blinking Configuration**<br>The Blink-S field selects in which PHY states the LED blinks with the pre-defined slow frequency. Each bit mask indicates a link speed. Combinations of the bit mask below can be used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not Active<br>$0001_B$**LINK10** Blink when Link is 10 Mbit/s<br>$0010_B$**LINK100** Blink when Link is 100 Mbit/s<br>$0100_B$**LINK1000** Blink when Link is 1000 Mbit/s<br>$1000_B$**LINK2500** Blink when Link is 2500 Mbit/s |
| PULSE | 11:8 | RW | **Pulsing Configuration**<br>The pulse field is a mask field in which certain events can be combined, e.g. TXACT\|RXACT, to generate a pulse on the LED when such an event is detected.<br>$0000_B$**NONE** No pulsing<br>$0001_B$**TXACT** Transmit activity<br>$0010_B$**RXACT** Receive activity<br>$0100_B$**COL** Collision<br>$1000_B$**NO_CON** Constant ON behavior is switched off |
| CON | 7:4 | RW | **Constant On Configuration**<br>The Constant-ON field selects in which PHY states the LED is constantly on. Each bit mask indicates a link speed. Combinations of the bit mask below can be used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not Active<br>$0001_B$**LINK10** On when Link is 10 Mbit/s<br>$0010_B$**LINK100** On when Link is 100 Mbit/s<br>$0100_B$**LINK1000** On when Link is 1000 Mbit/s<br>$1000_B$**LINK2500** On when Link is 2500 Mbit/s |
| BLINKF | 3:0 | RW | **Fast Blinking Configuration**<br>The Blink-F Field selects in which PHY states the LED blinks with the pre-defined fast frequency. Each bit mask indicates a link speed. Combinations of the bit mask below can be used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** No Active<br>$0001_B$**LINK10** Blink when Link is 10 Mbit/s<br>$0010_B$**LINK100** Blink when Link is 100 Mbit/s<br>$0100_B$**LINK1000** Blink when Link is 1000 Mbit/s<br>$1000_B$**LINK2500** Blink when Link is 2500 Mbit/s |

**Configuration for LED Pin 1 (Register 30.2)**

Configuration Register for LED Pin 1

IEEE Standard Register=30.2

**VSPEC1_LED1** **Reset Value**
**Configuration for LED Pin 1 (Register 30.2)** **$0320_H$**

| 15 … 12 | 11 … 8 | 7 … 4 | 3 … 0 |
|---|---|---|---|
| **BLINKS** | **PULSE** | **CON** | **BLINKF** |
| rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| BLINKS | 15:12 | RW | **Slow Blinking Configuration**<br>The Blink-S field selects in which PHY states the LED blinks with the pre-defined slow frequency. Each bit mask indicates a link speed. Combinations of the bit mask below can be used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not Active<br>$0001_B$**LINK10** Blink when Link is 10 Mbit/s<br>$0010_B$**LINK100** Blink when Link is 100 Mbit/s<br>$0100_B$**LINK1000** Blink when Link is 1000 Mbit/s<br>$1000_B$**LINK2500** Blink when Link is 2500 Mbit/s |
| PULSE | 11:8 | RW | **Pulsing Configuration**<br>The pulse field is a mask field by which certain events can be combined, e.g. TXACT\|RXACT, to generate a pulse on the LED when such an event is detected.<br>$0000_B$**NONE** No pulsing<br>$0001_B$**TXACT** Transmit activity<br>$0010_B$**RXACT** Receive activity<br>$0100_B$**COL** Collision<br>$1000_B$**NO_CON** Constant ON behavior is switched off |
| CON | 7:4 | RW | **Constant On Configuration**<br>The Constant-ON field selects in which PHY states the LED is constantly on. Each bit mask indicates a link speed. Combinations of the bit mask below can be used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not Active<br>$0001_B$**LINK10** On when Link is 10 Mbit/s<br>$0010_B$**LINK100** On when Link is 100 Mbit/s<br>$0100_B$**LINK1000** On when Link is 1000 Mbit/s<br>$1000_B$**LINK2500** On when Link is 2500 Mbit/s |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| BLINKF | 3:0 | RW | **Fast Blinking Configuration**<br>The Blink-F Field selects in which PHY states the LED blinks with the pre-defined fast frequency. Each bit mask indicates a link speed. Combinations of the bit mask below can be used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not Active<br>$0001_B$**LINK10** Blink when Link is 10 Mbit/s<br>$0010_B$**LINK100** Blink when Link is 100 Mbit/s<br>$0100_B$**LINK1000** Blink when Link is 1000 Mbit/s<br>$1000_B$**LINK2500** Blink when Link is 2500 Mbit/s |

**Configuration for LED Pin 2 (Register 30.3)**

Configuration Register for LED Pin 2

IEEE Standard Register=30.3

**VSPEC1_LED2** **Reset Value**
**Configuration for LED Pin 2 (Register 30.3)** **$0340_H$**

| 15 ... 12 | 11 ... 8 | 7 ... 4 | 3 ... 0 |
|---|---|---|---|
| **BLINKS** | **PULSE** | **CON** | **BLINKF** |
| rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| BLINKS | 15:12 | RW | **Slow Blinking Configuration**<br>The Blink-S field selects in which PHY states the LED blinks with the pre-defined slow frequency. Each bit mask indicates a link speed. Combinations of the bit mask below can be used to provide combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not Active<br>$0001_B$**LINK10** Blink when Link is 10 Mbit/s<br>$0010_B$**LINK100** Blink when Link is 100 Mbit/s<br>$0100_B$**LINK1000** Blink when Link is 1000 Mbit/s<br>$1000_B$**LINK2500** Blink when Link is 2500 Mbit/s |
| PULSE | 11:8 | RW | **Pulsing Configuration**<br>The pulse field is a mask field by which certain events can be combined, e.g. TXACT\|RXACT, to generate a pulse on the LED when such an event is detected.<br>$0000_B$**NONE** No pulsing<br>$0001_B$**TXACT** Transmit activity<br>$0010_B$**RXACT** Receive activity<br>$0100_B$**COL** Collision<br>$1000_B$**NO_CON** Constant ON behavior is switched off |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| CON | 7:4 | RW | **Constant On Configuration**<br>The Constant-ON field selects in which PHY states the LED is constantly on. Each bit mask indicates a link speed. Combinations of the bit mask below can be used to provide combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not Active<br>$0001_B$**LINK10** On when Link is 10 Mbit/s<br>$0010_B$**LINK100** On when Link is 100 Mbit/s<br>$0100_B$**LINK1000** On when Link is 1000 Mbit/s<br>$1000_B$**LINK2500** On when Link is 2500 Mbit/s |
| BLINKF | 3:0 | RW | **Fast Blinking Configuration**<br>The Blink-F Field selects in which PHY states the LED blinks with the pre-defined fast frequency. Each bit mask indicates a link speed. Combinations of the bit mask below can be used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not Active<br>$0001_B$**LINK10** Blink when Link is 10 Mbit/s<br>$0010_B$**LINK100** Blink when Link is 100 Mbit/s<br>$0100_B$**LINK1000** Blink when Link is 1000 Mbit/s<br>$1000_B$**LINK2500** Blink when Link is 2500 Mbit/s |

**Configuration for LED Pin 3 (Register 30.4)**

Configuration Register for LED Pin 3

IEEE Standard Register=30.4

**VSPEC1_LED3** — **Reset Value**

**Configuration for LED Pin 3 (Register 30.4)** — **$0380_H$**

| 15 … 12 | 11 … 8 | 7 … 4 | 3 … 0 |
|---|---|---|---|
| BLINKS | PULSE | CON | BLINKF |
| rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| BLINKS | 15:12 | RW | **Slow Blinking Configuration**<br>The Blink-S field selects in which PHY states the LED blinks with the pre-defined slow frequency. Each bit mask indicates a link speed. Combinations of the bit mask below can be used to provide combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not Active<br>$0001_B$**LINK10** Blink when Link is 10 Mbit/s<br>$0010_B$**LINK100** Blink when Link is 100 Mbit/s<br>$0100_B$**LINK1000** Blink when Link is 1000 Mbit/s<br>$1000_B$**LINK2500** Blink when Link is 2500 Mbit/s |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| PULSE | 11:8 | RW | **Pulsing Configuration**<br>The pulse field is a mask field by which certain events can be combined, e.g. TXACT\|RXACT, to generate a pulse on the LED when such an event is detected.<br>$0000_B$**NONE** No pulsing<br>$0001_B$**TXACT** Transmit activity<br>$0010_B$**RXACT** Receive activity<br>$0100_B$**COL** Collision<br>$1000_B$**NO_CON** Constant ON behavior is switched off |
| CON | 7:4 | RW | **Constant On Configuration**<br>The Constant-ON field selects in which PHY states the LED is constantly on. Each bit mask indicates a link speed. Combinations of the bit mask below can be used to provide combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not Active<br>$0001_B$**LINK10** On when Link is 10 Mbit/s<br>$0010_B$**LINK100** On when Link is 100 Mbit/s<br>$0100_B$**LINK1000** On when Link is 1000 Mbit/s<br>$1000_B$**LINK2500** On when Link is 2500 Mbit/s |
| BLINKF | 3:0 | RW | **Fast Blinking Configuration**<br>The Blink-F Field selects in which PHY states the LED blinks with the pre-defined fast frequency. Each bit mask indicates a link speed. Combinations of the bit mask below can be used to provide combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not Active<br>$0001_B$**LINK10** Blink when Link is 10 Mbit/s<br>$0010_B$**LINK100** Blink when Link is 100 Mbit/s<br>$0100_B$**LINK1000** Blink when Link is 1000 Mbit/s<br>$1000_B$**LINK2500** Blink when Link is 2500 Mbit/s |

**Chip Level SGMII control register (Register 30.8)**

SGMII control register to set up SGMII modes.

IEEE Standard Register=30.8

**VSPEC1_SGMII_CTRL** — **Reset Value**

**Chip Level SGMII control register (Register 30.8)** — **$34DA_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 8 | 7 | 6 | 5 | 4 2 | 1 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **RST** | **LB** | **Res** | **ANEN** | **PD** | **RXINV** | **Res** | **EEE_CAP** | **Res** | **SGMII_F*** | **Res** | **ANMODE** |
| rw | rw | | rw | rw | rw | | rw | | rw | | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| RST | 15 | RW | **Reset SGMII**<br>SGMII reset<br>$0_B$ **NORM** Normal Operation SGMII<br>$1_B$ **RST** Reset SGMII |
| LB | 14 | RW | **Loopback**<br>SGMII loopback<br>$0_B$ **OFF** SGMII Loopback is disabled<br>$1_B$ **ON** SGMII Loopback Enabled |
| ANEN | 12 | RW | **ANEG Enable**<br>If bit 12 is set to a logic one, ANMODE field determines the Auto-Negotiation protocol. If bit 12 is cleared to a logic zero, speed is set to maximum in full duplex mode. Once the TPI link is up, the SGMII speed is automatically forced to match the TPI speed. This bit has no effect when SGMII_FIXED2G5 is ‘1’.<br>$0_B$ **OFF** SGMII ANEG DisabledSpeed is set to maximum in full duplex mode until TPI is linkup.<br>$1_B$ **ON** SGMII ANEG EnabledThe negotiation style is configured by the field ANMODE |
| PD | 11 | RW | **Power Down**<br>SGMII Power Down<br>$0_B$ **OFF** Normal Operation SGMII<br>$1_B$ **ON** SGMII Power Down. In this state, other bits on VSPEC1_SGMII_CTRL register has no effect. |
| RXINV | 10 | RW | **Inversion of RX0_M and RX0_P**<br>The purpose of inverting RxM and RxP is to simplify PCB layout ( not crossing of lanes, allows 1 layer)<br>$0_B$ **NORMAL** No Inversion Pin 28 is RX0_P, pin 27 is RX0_M<br>$1_B$ **INVERT** Invert RX SGMII Pin 28 is RX0_M, pin 27 is RX0_P |
| EEE_CAP | 7 | RW | **EEE SGMII ANEG**<br>EEE SGMII Capability is advertised in ANEG<br>Used only when ANMODE = AN_CIS_PHY<br>$0_B$ **OFF** EEE is not advertised<br>$1_B$ **ON** EEE is advertised |
| SGMII_FIXED 2G5 | 5 | RW | **Force control the SGMII interface to remain in 2.5G speed or TPI link speed.**<br>Irrespective of TPI link speed, SGMII operates at 2.5G speed if this bit is enabled. The GPY packet manager perform the rate adaptation and Flow Control is used to backpressure the MAC SoC if required.<br>$0_B$ **NO_FORCE** SGMII speed is reconfigured by GPY based on TPI link speed.<br>$1_B$ **FORCE** SGMII speed is forced to 2.5G speed. |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| ANMODE | 1:0 | rw | **SGMII ANEG Mode**<br>Defines the type of ANEG protocol when ANEG is enabled<br>$00_B$ **RES** ReservedDo not use, will default to AN_CIS_PHY<br>$01_B$ **AN_1000BX** IEEE 1000Bx SGMII ANEGClause 37 SGMII 1000Bx ANEG is used<br>$10_B$ **AN_CIS_PHY** CISCO SGMII ANEG mode with GPY acting as a PHYANEG is done as defined by CISCO SGMII standard, as a PHY-side SGMII.This is the default configuration.<br>$11_B$ **AN_CIS_MAC** CISCO SGMII ANEG mode with GPY acting as a MACANEG is done as defined by CISCO SGMII standard, as a MAC-side SGMII. |

**Chip Level SGMII status register (Register 30.9)**

SGMII Status register.

All of the bits in the Status register are read only, a write has no effect.

IEEE Standard Register=30.9

**VSPEC1_SGMII_STAT** **Reset Value**
**Chip Level SGMII status register (Register 30.9)** **$8008_H$**

| 15 | 14 … 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 … 0 |
|---|---|---|---|---|---|---|---|---|
| **MACSEC_*** | **Res** | **RES** | **Res** | **ANOK** | **RF** | **ANAB** | **LS** | **DR** |
| ro | | ro | | ro | rolh | ro | roll | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| MACSEC_CAP | 15 | RO | **MACSEC Capability in the product**<br>$0_B$ **DISABLED** Product is not MACSEC capable<br>$1_B$ **ENABLED** Product is MACSEC capable |
| RES | 7 | RO | **Reserved**<br>Ignore when read. |
| ANOK | 5 | RO | **Auto-Negotiation Completed**<br>Indicates whether the auto-negotiation process is completed or not.<br>$0_B$ **RUNNING** Auto-negotiation process is in progress or not started<br>$1_B$ **COMPLETED** Auto-negotiation process is completed |
| RF | 4 | ROLH | **Remote Fault**<br>Indicates the detection of a remote fault event.<br>$0_B$ **INACTIVE** No remote fault condition detected<br>$1_B$ **ACTIVE** Remote fault condition detected |
| ANAB | 3 | RO | **Auto-Negotiation Ability**<br>Specifies the auto-negotiation ability.<br>$0_B$ **DISABLED** PHY is not able to perform auto-negotiation<br>$1_B$ **ENABLED** PHY is able to perform auto-negotiation |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| LS | 2 | ROLL | **Link Status**<br>Indicates the link status of the SGMII<br>$0_B$ **INACTIVE** The link is down. No communication with link partner possible.<br>$1_B$ **ACTIVE** The link is up. Data communication with link partner is possible. |
| DR | 1:0 | RO | **SGMII Data Rate**<br>This field indicates the operating data rate of SGMII when link is up<br>$00_B$ **DR_10** SGMII link rate is 10 Mbit/s<br>$01_B$ **DR_100** SGMII link rate is 100 Mbit/s<br>$10_B$ **DR_1G** SGMII link rate is 1000 Mbit/s<br>$11_B$ **DR_2G5** SGMII link rate is 2500 Mbit/s |

**NBASE-T Downshift Control Register (Register 30.10)**

IEEE Standard Register=30.10

**VSPEC1_NBT_DS_CTRL** — **Reset Value**
**NBASE-T Downshift Control Register (Register 30.10)** — **$0400_H$**

| 15 … 8 | 7 | 6 … 2 | 1 | 0 |
|---|---|---|---|---|
| **NRG_RST_CNT** | **FORCE_R*** | **DOWNSHIFT_THR** | **DOWNSHI*** | **NO_NRG_*** |
| rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| NRG_RST_CNT | 15:8 | RW | **Timer to Reset the Downshift process**<br>If energy is zero for a duration equal to NRG_RST_CNT seconds approximately, then resets the ANEG advertised capabilities to the maximum GPY capabilities.<br>Default is 4 seconds |
| FORCE_RST | 7 | RW | **Force Reset of Downwshift Process**<br>Setting this bit to 1 immediately resets the ANEG advertised capabilities to the maximum GPY capabilities. |
| DOWNSHIFT_THR | 6:2 | RW | **NBASE-T Downshift Training Counter Threshold**<br>dsh_thr variable in NBASE-T specification<br>Counter from 0 to 15 implemented on 4 bits controlling the number of training cycles allowed for linkup, otherwise downshift |
| DOWNSHIFT_EN | 1 | RW | **NBASE-T Downshift Enable**<br>dsh_en variable in NBASE-T specification<br>$0_B$ **DISABLE** Disable NBT downshift<br>$1_B$ **ENABLE** Enable NBT downshift |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| NO_NRG_RST | 0 | RW | **Advertise all Speeds if No Energy Detected**<br>If no energy is detected, resets to advertise all speeds<br>energy variable in NBASE-T specification<br>$0_B$ **DISABLE** Do not reset speeds adv when no energy detected<br>$1_B$ **ENABLE** Reset speed adv when no energy detected |

**NBASE-T Downshift Status Register (Register 30.11)**

IEEE Standard Register=30.11

**VSPEC1_NBT_DS_STA** — **Reset Value**
**NBASE-T Downshift Status Register (Register 30.11)** — **$0000_H$**

| 15–9 | 8 | 7 | 6 | 5 | 4–0 |
|---|---|---|---|---|---|
| Res | DOWNSHI* | DOWNSHI* | DOWNSHI* | DOWNSHI* | DOWNSHIFT_CNT |
| | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| DOWNSHIFT_1G | 8 | RO | **Downshift from 1G to lower speed** |
| DOWNSHIFT_2G5 | 7 | RO | **Downshift from 2.5 G to lower speed** |
| DOWNSHIFT_5G | 6 | RO | **Downshift 5G to lower speed**<br>Not supported by GPY |
| DOWNSHIFT_10G | 5 | RO | **Downshift 10G to lower speed**<br>Not supported by GPY |
| DOWNSHIFT_CNT | 4:0 | RO | **Training attempt counter**<br>Counts training attempts to select the operating speed<br>dsh_cnt state variable in NBASE-T specification |

**Packet Manager Control (Register 30.12)**

IEEE Standard Register=30.12

Control the Packet Manager Configuration

**VSPEC1_PM_CTRL** — **Reset Value**
**Packet Manager Control (Register 30.12)** — **$0003_H$**

| 15–7 | 6–5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|
| Res | SYNCE_CLK | SYNCE_EN | PTP_158* | PTP_158* | MACSEC_* | PM_EN |
| | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| SYNCE_CLK | 6:5 | RW | **Configure the Sync E clock frequency class.**<br>$00_B$ **PSTN** Sync E clock frequency is PSTN class: 8 kHz<br>$01_B$ **EEC1** Sync E clock frequency is EEC-1 class: 2.048 MHz<br>$10_B$ **EEC2** Sync E clock frequency is EEC-2 class: 1.544 MHz<br>$11_B$ **RES** Reserved |
| SYNCE_EN | 4 | RW | **Enable Sync E feature**<br>$0_B$ **DISABLE** Disable Sync E<br>$1_B$ **ENABLE** Enable Sync E |
| PTP_1588_STEP | 3 | RW | **Configure 1588 time stamping mode**<br>$0_B$ **TWO_STEP** Two steps time stamping<br>$1_B$ **ONE_STEP** One step time stamping |
| PTP_1588_EN | 2 | rw | **Enable Sync 1588 PTP feature**<br>$0_B$ **DISABLE** Disable<br>$1_B$ **ENABLE** Enable |
| MACSEC_EN | 1 | RW | **Disable MACsec (Applicable to MACsec capable devices only)**<br>On MACsec capable products, the MACsec feature is enabled at power up. This option allows to disable MACsec feature programmatically. On non-MACsec capable products, this option has no effect and is always DISABLE. The MACsec capability is indicated a power up in VSPEC1_SGMII_STAT.MACSEC_CAP.<br>$0_B$ **DISABLE** Disable<br>$1_B$ **ENABLE** Enableno effect on GPY |
| PM_EN | 0 | RW | **Enable Packet Manager**<br>Enable LPI generation within the GPY<br>Packet Manager on GPY supports the Smart AZ and PTP features.<br>$0_B$ **DISABLE** DisablePM is bypassed<br>$1_B$ **ENABLE** Enable |

**Temperature code (Register 30.14)**

Junction Temperature Code that can be converted to T Celsius by the GPY API.

IEEE Standard Register=30.14

**VSPEC1_TEMP_STA** — **Reset Value**

**Temperature code (Register 30.14)** — **$0000_H$**

| 15–10 | 9–0 |
|---|---|
| **Res** | **TEMP_DATA** |
| | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| TEMP_DATA | 9:0 | RO | **Code for Junction Temperature**<br>This code can be converted to Temperature in Celsius Degrees by the GPY API driver. The STA is expected to take thermal mitigation measures when the junction temperature exceeds Normal Operating Range.<br>The code is invalid when the value is 0x0000.<br>Conversion formula: T in Celsius = ( -2.5761E-11)*N^4 + (9.7332E-8)*N^3+ (-1.9165E-04)*N^2+(3.0762E-1)*N +(-5.2156E+1) , with N = decimal value of the code TEMP_DATA<br>For Tj = -40 deg C, TEMP_DATA = 40.5 (decimal)<br>For Tj= +125 degC, TEMP_DATA = 912 (decimal) |

**MACSec Interrupt Mask Register (Register 30.17)**

This register defines the mask for the Interrupt Status Register (ISTAT) which contains the event source for the MDINT interrupt sent from GPY to an external chip.

The information about the interrupt source is indicated in the VSPEC1_ISTAT register.

IEEE Standard Register=30.17

**VSPEC1_IMASK** — **Reset Value**

**MACSec Interrupt Mask Register (Register 30.17)** — **$0000_H$**

| 15–5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|
| **Res** | **MACSEC** | **TS_FIFO** | **MCI** | **PM_LPI** | **GMAC L_TS** |
| | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| MACSEC | 4 | RW | **MACSEC Egress/Ingress Interrupt**<br>When active, MDINT is activated upon interrupt from MACSEC Egress/Ingress.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| TS_FIFO | 3 | RW | **Time Stamp FIFO Interrupt**<br>When active, MDINT is activated upon interrupt from either TX or RX Time Stamp FIFO.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| MCI | 2 | RW | **MCI Interrupt Request**<br>When active, MDINT is activated upon interrupt request from MCI.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| PM_LPI | 1 | RW | **PM LPI Interrupt Request**<br>When active, MDINT is activated upon LPI Interrupt Request from PM.<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |
| GMACL_TS | 0 | RW | **Status of Interrupt Request GMACL TS**<br>When active, MDINT is activated upon GMACL Timestamp Valid Interrupt<br>$0_B$ **INACTIVE** Interrupt is masked out<br>$1_B$ **ACTIVE** Interrupt is activated |

**MACSec Interrupt Mask Register (Register 30.18)**

This register defines the event source for the MDINT interrupt sent from GPY to an external chip based on the mask settings in VSPEC1_IMASK register.

VSPEC1_ISTAT is a cleared on read by the STA.

IEEE Standard Register=30.18

**VSPEC1_ISTAT** — **Reset Value**
**MACSec Interrupt Mask Register (Register 30.18)** — **$0000_H$**

| 15–5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|
| Res | MACSEC | TS_FIFO | MCI | PM_LPI | GMACL_TS |
| | rosc | rosc | rosc | rosc | rosc |

| Field | Bits | Type | Description |
|---|---|---|---|
| MACSEC | 4 | ROSC | **MACSEC Egress/Ingress Interrupt**<br>When bit is set, MDINT is activated upon interrupt from MACSEC Egress/Ingress.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** MACSEC Egress/Ingress Interrupt is the source of Interrupt |
| TS_FIFO | 3 | ROSC | **Time Stamp FIFO Interrupt**<br>When bit is set, MDINT is activated upon interrupt from either TX or RX Time Stamp FIFO.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** Time Stamp FIFO Interrupt is the source of Interrupt |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| MCI | 2 | ROSC | **MCI Interrupt Request**<br>When bit is set, MDINT is activated upon interrupt request from MCI.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** MCI Interrupt Request is the source of Interrupt |
| PM_LPI | 1 | ROSC | **PM LPI Interrupt Request**<br>When bit is set, MDINT is activated upon LPI Interrupt Request from PM.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** LPI Interrupt Request from PM is the source of Interrupt |
| GMACL_TS | 0 | ROSC | **Status of Interrupt Request GMACL TS**<br>When bit is set, MDINT is activated upon interrupt from GMACL Timestamp Valid Interrupt.<br>$0_B$ **INACTIVE** This event is not the interrupt source<br>$1_B$ **ACTIVE** GMACL Time Stamp is the source of Interrupt |

**ASP Mapping to Physical Lanes(Register 30.20)**

Programmable option to map physical lanes A,B,C,D of the TPI to the ASPs.

*Note: Each ASP must be mapped to each lane.*

IEEE Standard Register=30.20

**VSPEC1_LANE_ASP_MAP** **Reset Value**
**ASP Mapping to Physical Lanes(Register 30.20)** **$00E4_H$**

| 15–8 | 7–6 | 5–4 | 3–2 | 1–0 |
|---|---|---|---|---|
| Res | LANE_D | LANE_C | LANE_B | LANE_A |
| | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| LANE_D | 7:6 | RW | **Map Physical Lane-D to the ASP**<br>$00_B$ **ASPA** Map Physical Lane-D to the ASP-A<br>$01_B$ **ASPB** Map Physical Lane-D to the ASP-B<br>$10_B$ **ASPC** Map Physical Lane-D to the ASP-C<br>$11_B$ **ASPD** Map Physical Lane-D to the ASP-D |
| LANE_C | 5:4 | RW | **Map Physical Lane-C to the ASP**<br>$00_B$ **ASPA** Map Physical Lane-C to the ASP-A<br>$01_B$ **ASPB** Map Physical Lane-C to the ASP-B<br>$10_B$ **ASPC** Map Physical Lane-C to the ASP-C<br>$11_B$ **ASPD** Map Physical Lane-C to the ASP-D |
| LANE_B | 3:2 | RW | **Map Physical Lane-B to the ASP**<br>$00_B$ **ASPA** Map Physical Lane-B to the ASP-A<br>$01_B$ **ASPB** Map Physical Lane-B to the ASP-B<br>$10_B$ **ASPC** Map Physical Lane-B to the ASP-C<br>$11_B$ **ASPD** Map Physical Lane-B to the ASP-D |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| LANE_A | 1:0 | RW | **Map Physical Lane-A to the ASP**<br>$00_B$ **ASPA** Map Physical Lane-A to the ASP-A<br>$01_B$ **ASPB** Map Physical Lane-A to the ASP-B<br>$10_B$ **ASPC** Map Physical Lane-A to the ASP-C<br>$11_B$ **ASPD** Map Physical Lane-A to the ASP-D |

## 6.5 Vendor Specific 2 Device for MMD=0x1F

This register file contains GPY specific register for MMD=31 (decimal)

**Table 25 Registers Overview**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| VPSPEC2_WOL_CTL | Wake-on-LAN Control Register (Register 31.3590) | $0000_H$ |
| VPSPEC2_WOL_AD01 | Wake-On-LAN Address Byte 0 and 1 (Register 31.3592) | $0000_H$ |
| VPSPEC2_WOL_AD23 | Wake-on-LAN Address Byte 2 and 3 (Register 31.3593) | $0000_H$ |
| VPSPEC2_WOL_AD45 | Wake-On-LAN Address Byte 4 and 5 (Register 31.3594) | $0000_H$ |
| VPSPEC2_WOL_PW01 | Wake-On-LAN SecureON Password Byte 0 (Register 31.3595) | $0000_H$ |
| VPSPEC2_WOL_PW23 | Wake-on-LAN SecureON Password Byte 2 and 3 (Register 31.3596) | $0000_H$ |
| VPSPEC2_WOL_PW45 | Wake-on-LAN SecureON Password Byte 4 and 5 (Register 31.3597) | $0000_H$ |

### 6.5.1 Vendor Specific 2 Device for MMD=0x1F

This chapter describes all registers of VSPEC2 in detail.

**Wake-on-LAN Control Register (Register 31.3590)**

Wake-on-LAN Control Register. Redirected to PCS_PDI_WOL_CTL

IEEE Standard Register=31.3590

**VPSPEC2_WOL_CTL** — **Reset Value**

**Wake-on-LAN Control Register (Register 31.3590)** — **$0000_H$**

| 15 … 3 | 2 | 1 | 0 |
|---|---|---|---|
| Res | SPWD_EN | RES | EN |
| | rw | ro | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| SPWD_EN | 2 | RW | **Secure-ON Password Enable**<br>If enabled, checks for the Secure-ON password after the 16 MAC address repetitions.<br>$0_B$ **DISABLED** Secure-On password check is disabled<br>$1_B$ **ENABLED** Secure-On password check is enabled |
| RES | 1 | RO | **Reserved**<br>Must always be written to zero! |
| EN | 0 | RW | **Enables the Wake-on-LAN functionality**<br>If Wake-on-LAN is enabled, the PHY scans for the configured magic packet and indicates its reception via the register bit ISTAT.WOL, and optionally also via interrupt.<br>$0_B$ **DISABLED** Wake-on-LAN functionality is disabled<br>$1_B$ **ENABLED** Wake-on-LAN functionality is enabled |

### Wake-On-LAN Address Byte 0 and 1 (Register 31.3592)

Wake-on-LAN Address Byte 0 and 1. Redirected to PCS_PDI_WOL_AD01

IEEE Standard Register=31.3592

**VPSPEC2_WOL_AD01** — **Reset Value**

**Wake-On-LAN Address Byte 0 and 1 (Register 31.3592)** — **$0000_H$**

| 15 … 8 | 7 … 0 |
|---|---|
| **AD1** | **AD0** |
| rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| AD1 | 15:8 | RW | **Address Byte 1**<br>Defines byte 1 of the WoL-designated MAC address to which the PHY is sensitive. |
| AD0 | 7:0 | RW | **Address Byte 0**<br>Defines byte 0 of the WoL-designated MAC address to which the PHY is sensitive. |

### Wake-on-LAN Address Byte 2 and 3 (Register 31.3593)

Wake-On-LAN Address Byte 2 and 3. Redirected to PCS_PDI_WOL_AD23

IEEE Standard Register=31.3593

**VPSPEC2_WOL_AD23** — **Reset Value**

**Wake-on-LAN Address Byte 2 and 3 (Register 31.3593)** — **$0000_H$**

| 15 … 8 | 7 … 0 |
|---|---|
| **AD3** | **AD2** |
| rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| AD3 | 15:8 | RW | **Address Byte 3**<br>Defines byte 3 of the WoL-designated MAC address to which the PHY is sensitive. |
| AD2 | 7:0 | RW | **Address Byte 2**<br>Defines byte 2 of the WoL-designated MAC address to which the PHY is sensitive. |

### Wake-On-LAN Address Byte 4 and 5 (Register 31.3594)

Wake-On-LAN Address Byte 4 and 5. Redirected to PCS_PDI_WOL_AD45

IEEE Standard Register=31.3594

**VPSPEC2_WOL_AD45** — Reset Value
**Wake-On-LAN Address Byte 4 and 5 (Register 31.3594)** — $0000_H$

| 15 … 8 | 7 … 0 |
|---|---|
| AD5 | AD4 |
| rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| AD5 | 15:8 | RW | **Address Byte 5**<br>Defines byte 5 of the WoL-designated MAC address to which the PHY is sensitive. |
| AD4 | 7:0 | RW | **Address Byte 4**<br>Defines byte 4 of the WoL-designated MAC address to which the PHY is sensitive. |

**Wake-On-LAN SecureON Password Byte 0 (Register 31.3595)**

Wake-on-LAN SecureON Password Byte 0. Redirected to PCS_PDI_WOL_PWD01

IEEE Standard Register=31.3595

**VPSPEC2_WOL_PW01** — Reset Value
**Wake-On-LAN SecureON Password Byte 0 (Register 31.3595)** — $0000_H$

| 15 … 8 | 7 … 0 |
|---|---|
| PW1 | PW0 |
| rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| PW1 | 15:8 | RW | **SecureON Password Byte 1**<br>Defines byte 1 of the WoL-designated SecureON password to which the PHY is sensitive. |
| PW0 | 7:0 | RW | **SecureON Password Byte 0**<br>Defines byte 0 of the WoL-designated SecureON password to which the PHY is sensitive. |

**Wake-on-LAN SecureON Password Byte 2 and 3 (Register 31.3596)**

Wake-On-LAN SecureON Password Byte 2 and 3. Redirected to PCS_PDI_WOL_PWD23

IEEE Standard Register=31.3596

**VPSPEC2_WOL_PW23** — Reset Value
**Wake-on-LAN SecureON Password Byte 2 and 3 (Register 31.3596)** — $0000_H$

| 15 … 8 | 7 … 0 |
|---|---|
| PW3 | PW2 |
| rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| PW3 | 15:8 | RW | **SecureON Password Byte 3**<br>Defines byte 3 of the WoL-designated SecureON password to which the PHY is sensitive. |
| PW2 | 7:0 | RW | **SecureON Password Byte 2**<br>Defines byte 2 of the WoL-designated SecureON password to which the PHY is sensitive. |

**Wake-on-LAN SecureON Password Byte 4 and 5 (Register 31.3597)**

Wake-on-LAN SecureON Password Byte 4 and 5. Redirected to PCS_PDI_WOL_PWD45

IEEE Standard Register=31.3597

**VPSPEC2_WOL_PW45** **Reset Value**
**Wake-on-LAN SecureON Password Byte 4 and 5 (Register 31.3597)** **$0000_H$**

| 15 … 8 | 7 … 0 |
|---|---|
| PW5 | PW4 |
| rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| PW5 | 15:8 | RW | **SecureON Password Byte 5**<br>Defines byte 5 of the WoL-designated SecureON password to which the PHY is sensitive. |
| PW4 | 7:0 | RW | **SecureON Password Byte 4**<br>Defines byte 4 of the WoL-designated SecureON password to which the PHY is sensitive. |

# 7 Electrical Characteristics

This chapter defines the electrical characteristics of the Gigabit Ethernet PHY.

*Note: This chapter is a preliminary draft and subject to change until PRQ.*

## 7.1 Absolute Maximum Ratings

Table 26 shows the absolute maximum ratings for the Gigabit Ethernet PHY.

**Table 26 Absolute Maximum Ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Storage Temperature Limits | $T_{STG}$ | -55.0 | – | 125.0 | °C | – |
| Soldering Temperature | $T_{SOL}$ | – | – | 260.0 | °C | Compliance with Pb free re-flow soldering profile as J-STD-020D |
| Moisture Level 3 Temperature Limits | $T_{ML3}$ | – | – | 260.0 | °C | According to IPS J-STD 020 |
| Absolute Junction Temperature | $T_{JABS}$ | 0 | | 125 | °C | Thermal solution must ensure that $T_J$ never exceeds $T_{JABS}$. The chip resets the device when $T_J$ > $T_{JABS}$ to prevent any damage to occur. |
| DC Voltage Limits on VDDP3V3 Pins | $V_{DDP3V3}$ | -0.5 | – | +3.63 | V | $V_{HIGH}$ supply |
| DC Voltage Limits on VDDP Pins when pin 19 pin strap PS_MDIO_VOLTAGE is HIGH | $V_{DDP}$ | -0.5 | – | +3.63 | V | $V_{HIGH}$ supply |
| DC Voltage Limits on VDDP Pins when pin 19 pin strap PS_MDIO_VOLTAGE is LOW | $V_{DDP}$ | -0.5 | – | +1.98 | V | 1.8 V supply dedicated to MDIO pads in lower mode |
| DC Voltage Limits on VPH Pins | $V_{PH}$ | -0.5 | – | +3.63 | V | $V_{HIGH}$ supply |
| DC Voltage Limits on VP Pins | $V_P$ | -0.5 | – | +1.05 | V | $V_{LOW}$ supply |
| DC Voltage Limits on VDDA3V3 Pins | $V_{DDA3V3}$ | -0.5 | – | +3.63 | V | $V_{HIGH}$ supply |
| DC Voltage Limits on VDDA3V3XO, VDDA3V3CDB, VDDA3V3AON Pins | $V_{DDA3V3XO}$ $V_{DDA3V3CDB}$ $V_{DDA3V3AON}$ | -0.5 | – | +3.63 | V | $V_{HIGH}$ supply |
| DC Voltage Limits on VDDA0V9 Pins | $V_{DDA0V9}$ | -0.5 | – | +1.05 | V | $V_{LOW}$ supply |
| DC Voltage Limits on VDD Pins | $V_{DD}$ | -0.5 | – | +1.05 | V | $V_{LOW}$ supply |

**Table 26 Absolute Maximum Ratings** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| DC Voltage Limits on VDD3V3DCDC Pins | $V_{DD3V3DCDC}$ | -0.5 | – | +3.63 | V | $V_{HIGH}$ supply |
| DC Voltage Limits on any other pins[1] with respect to the ground | $V_{DC}$ | -0.5 | – | $V_{DDP3V3}$+ 0.5 | V | Unless specified otherwise |
| ESD HBM Robustness | $V_{ESD,HBM}$ | – | – | 1000.0 | V | According to ANSI/ESDA/JEDEC JS-001-2014 |
| ESD CDM Robustness | $V_{ESD,CDM}$ | – | – | 250.0 | V | According to ANSI/ESDA/JEDEC JS-002-2014 |

1) This means any pin which is not a supply pin out of one of the domains: $V_{DDP}$, $V_{PH}$, $V_P$, $V_{DDA3V3}$, $V_{DDA3V3XO}$, $V_{DDA3V3CDB}$,$V_{DDA3V3AON}$, $V_{DDA0V9}$, $V_{DD}$, $V_{DD3V3DCDC}$.

***Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.***

## 7.2 Operating Range

Table 27 defines the maximum values of voltages and temperature that must be applied to guarantee proper operation of the Gigabit Ethernet PHY. The values are relative to a ground voltage $V_{SS}$ of 0.0 V.

**Table 27 Operating Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Ambient Temperature | $T_A$ | 0 | – | 70 | °C | The device can operate in an ambient temperature of up to 85°C, when it is ensured that the maximum junction temperature ($T_j$) of 110°C is not exceeded. |
| Junction Temperature | $T_j$ | – | – | 110 | °C | Thermal solution must ensure that $T_j$ remains within operating range and never exceed maximum absolute ratings. |
| Pad Supply Voltage for MDIO signals when pin 19 pin strap PS_MDIO_VOLTAGE is LOW | $V_{DDP}$ | 1.71 | 1.8 | 1.89 | V | 1.8 V supply dedicated to MDIO pads in lower mode |
| Pad Supply Voltage for MDIO signals when pin 19 pin strap PS_MDIO_VOLTAGE is HIGH | $V_{DDP}$ | 3.135 | 3.30 | 3.46 | V | $V_{HIGH}$ supply |
| Pad Supply Voltage for non-MDIO signals | $V_{DDP3V3}$ | 3.13 | 3.30 | 3.46 | V | $V_{HIGH}$ supply |
| Analog High Supply Voltage | $V_{DDA3V3}$ | 3.13 | 3.30 | 3.46 | V | $V_{HIGH}$ supply |
| XO High Supply Voltage | $V_{DDA3V3XO}$ | 3.13 | 3.30 | 3.46 | V | $V_{HIGH}$ supply |
| CDB High Supply Voltage | $V_{DDA3V3CDB}$ | 3.13 | 3.30 | 3.46 | V | $V_{HIGH}$ supply |
| AON High Supply Voltage | $V_{DDA3V3AON}$ | 3.13 | 3.30 | 3.46 | V | $V_{HIGH}$ supply |
| SGMII High Supply Voltage | $V_{PH}$ | 3.13 | 3.30 | 3.46 | V | $V_{HIGH}$ supply |
| Analog Low Supply Voltage | $V_{DDA0V9}$ | 0.97 | 1.00 | 1.03 | V | $V_{LOW}$ supply |
| SGMII Low Supply Voltage | $V_P$ | 0.97 | 1.00 | 1.03 | V | $V_{LOW}$ supply |
| Core Digital Supply Voltage | $V_{DD}$ | 0.97 | 1.00 | 1.03 | V | $V_{LOW}$ supply |
| DCDC Supply Voltage | $V_{DD3V3DCDC}$ | 3.13 | 3.30 | 3.46 | V | $V_{HIGH}$ supply |
| Digital Input Voltage | $V_{ID}$ | -0.30 | – | $V_{DDP3V3}$+0.3 | V | – |
| XTAL1 Input Voltage | $V_{XTLA1}$ | -0.30 | 1.8 | 2 | V | – |

***Attention:** Operations above the max. values listed here for extended periods can adversely affect long-term reliability of the device.*

## 7.3 Chip Power Consumption

Power consumption at 25°C ambient temperature is indicated in **Table 28** and **Table 29** for the different modes 2500/1000/100/10BASE-T in Link-up and EEE modes. The Link-up conditions are full-speed, bidirectional, full-duplex.

Power numbers are indicated for the 2 supply configuration:

- using an external supply of the $V_{LOW}$ domains at 1.0 V (circuitry specified in **Figure 29**)
- using the internal DCDC SVR (circuitry specified in **Figure 28**)

**Table 28 Typical Power Consumption (GPY212C0VC)**

| **Conditions:**<br>**25°C, CAT 5E Cable**<br>**$V_{LOW}$ at 1.0 V** | **3.3 V $V_{HIGH}$ Domain Current, with external Supply of $V_{LOW}$** | **1.0 V $V_{LOW}$ Domain Current, with external Supply of $V_{LOW}$** | **Chip Power with external Supply of $V_{LOW}$** | **Chip Power with Supply of $V_{LOW}$ generated by internal DC/DC SVR** |
|---|---|---|---|---|
| **Unit** | **mA** | **mA** | **W** | **W** |
| 2500BASE-T Link-Up, 100 m cable | 104 | 705 | 1.05 | 1.3 |
| 2500BASE-T Link-Up, 30 m cable | 100 | 670 | 1.0 | 1.1 |
| 2500BASE-T EEE | 85 | 370 | 0.65 | 0.72 |
| 1000BASE-T Link-Up, 100 m cable | 74 | 275 | 0.52 | 0.58 |
| 1000BASE-T EEE | 30 | 140 | 0.24 | 0.24 |
| 100BASE-TX Link-Up, 100 m cable | 42 | 121 | 0.26 | 0.24 |
| 100BASE-TX EEE | 30 | 112 | 0.21 | 0.17 |
| 10BASE-Te Link-Up, 100 m cable | 33 | 101 | 0.21 | 0.18 |
| Cable Unplugged - ANEG | 33 | 103 | 0.22 | 0.23 |
| Cable Unplugged - ULP | NA[1)] | NA[1)] | NA[1)] | 0.005 |
| Reset | 8.6 | 19 | 0.045 | 0.015 |

1) The ULP state is reachable only when an internal DCDC SVR supply mode is used. In such cases, 1.6 mA is consumed by the 3.3 V $V_{high}$ domain. When the External DCDC SVR supply mode is used, the lowest power state is ANEG.

**Table 29 Typical Power Consumption (GPY212B1VC)**

| **Conditions:**<br>**25°C, CAT 5E Cable**<br>**$V_{LOW}$ at 1.0 V** | **3.3 V $V_{HIGH}$ Domain Current, with external Supply of $V_{LOW}$** | **1.0 V $V_{LOW}$ Domain Current, with external Supply of $V_{LOW}$** | **Chip Power with external Supply of $V_{LOW}$** | **Chip Power with Supply of $V_{LOW}$ generated by internal DC/DC SVR** |
|---|---|---|---|---|
| **Unit** | **mA** | **mA** | **W** | **W** |
| 2500BASE-T Link-Up, 100 m cable | 165 | 850 | 1.34 | 1.57 |
| 2500BASE-T Link-Up, 30 m cable | 152 | 741 | 1.19 | 1.41 |
| 2500BASE-T EEE | 140 | 560 | 0.99 | 1.1 |
| 1000BASE-T Link-Up, 100 m cable | 98 | 322 | 0.63 | 0.62 |
| 1000BASE-T EEE | 43 | 187 | 0.32 | 0.31 |

**Table 29 Typical Power Consumption (GPY212B1VC)**

| Conditions: 25°C, CAT 5E Cable $V_{LOW}$ at 1.0 V | 3.3 V $V_{HIGH}$ Domain Current, with external Supply of $V_{LOW}$ | 1.0 V $V_{LOW}$ Domain Current, with external Supply of $V_{LOW}$ | Chip Power with external Supply of $V_{LOW}$ | Chip Power with Supply of $V_{LOW}$ generated by internal DC/DC SVR |
|---|---|---|---|---|
| 100BASE-TX Link-Up, 100 m cable | 57 | 132 | 0.31 | 0.28 |
| 100BASE-TX EEE | 38 | 122 | 0.24 | 0.21 |
| 10BASE-Te Link-Up, 100 m cable | 45 | 114 | 0.25 | 0.23 |
| Cable Unplugged - ANEG | 39 | 134 | 0.26 | 0.23 |
| Cable Unplugged - ULP | NA[1)] | NA[1)] | NA[1)] | 0.005 |
| Reset | 8.6 | 19 | 0.045 | 0.015 |

1) The ULP state is reachable only when an internal DCDC SVR supply mode is used. In such cases, 1.6 mA is consumed by the 3.3 V $V_{high}$ domain. When the External DCDC SVR supply mode is used, the lowest power state is ANEG.

**Table 30 Maximum Power Consumption (GPY212C0VC)**

| Conditions: $T_j$ 110°C | External Supply of $V_{LOW}$ | $V_{LOW}$ Generated by Internal DC/DC SVR |
|---|---|---|
| **Unit** | **W** | **W** |
| Maximum Chip Power at maximum operating range | 1.40 | 1.80 |

**Table 31 Maximum Power Consumption (GPY212B1VC)**

| Conditions: $T_j$ 110°C | External Supply of $V_{LOW}$ | $V_{LOW}$ Generated by Internal DC/DC SVR |
|---|---|---|
| **Unit** | **W** | **W** |
| Maximum Chip Power at maximum operating range | 1.50 | 1.92 |

*Note: Analysis indicates that real application are unlikely to cause $T_j$ to exceed 110°C, given a properly designed thermal solution: Heat Sink and change of speed controlled by the STA when the temperature $T_j$ (reported in MDIO register VSPEC1_TMP_STA) exceeds the operating range.*

## 7.4 DC Characteristics

The following sections describe the DC characteristics of the Gigabit Ethernet PHY external interfaces.

### 7.4.1 Digital Interfaces

This chapter defines the DC characteristics of the GPIO interfaces as follows:

- MDIO
- Interrupts
- Clock Outputs
- General Purpose IO
- LED
- JTAG
- SPI

The DC characteristics for $V_{DDP}$=3.3 V are summarized in **Table 32**.

**Table 32 DC Characteristics of the GPIO Interfaces (VDDP = 3.3 V)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input High Voltage | $V_{IH}$ | 2 | – | $V_{DDP}$+0.3 | V | – |
| Input Low Voltage | $V_{IL}$ | –0.3 | – | 0.8 | V | – |
| Output High Voltage | $V_{OH}$ | $V_{DDP}$-0.4 | – | – | V | $I_{OH}$= 2, 4, 8, 12 mA |
| Output Low Voltage | $V_{OL}$ | – | – | 0.4 | V | $I_{OL}$= 2, 4, 8, 12 mA |

The DC characteristics for $V_{DDP}$=1.8 V are summarized in **Table 33**.

**Table 33 DC Characteristics of the GPIO Interfaces (VDDP = 1.8 V)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input High Voltage | $V_{IH}$ | 0.65*$V_{DDP}$ | – | $V_{DDP}$+0.3 | V | – |
| Input Low Voltage | $V_{IL}$ | –0.3 | – | 0.35*$V_{DDP}$ | V | – |
| Output High Voltage | $V_{OH}$ | $V_{DDP}$-0.4 | – | – | V | $I_{OH}$= 2, 4, 8, 12 mA |
| Output Low Voltage | $V_{OL}$ | – | – | 0.4 | V | $I_{OL}$= 2, 4, 8, 12 mA |

### 7.4.2 Twisted Pair Interface

The TPI conforms to the specifications of 10BASE-T (Clause 14), 100BASE-TX (Clause 25), 1000BASE-T (Clause 40) and 2.5GBASE-T (Clause 126) given in IEEE 802.3-2005, IEEE 802.3bz, as well as ANSI X3.263-1995.

### 7.4.3 Built-in Temperature Sensor

The following table gives the parameters of the integrated temperature sensor, measuring junction temperature $T_j$.

**Table 34 Temperature Sensor Characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Temperature Range | $T_{range}$ | -40 | | 125 | °C | Thermal Mitigation measures must ensure that $T_j$ remains within operating range. If $T_j$ exceeds Maximum Ratings, the GPY performs a self-reset to prevent damage, and the next ANEG is re-started advertising a lower speed. |
| Resolution | | – | 10 | – | bits | – |
| Accuracy | | -5 | – | +5 | °C | – |

## 7.5 AC Characteristics

The following sections describe the AC characteristics of the external interfaces.

### 7.5.1 Power Up and Power Down Sequence with External Supply of $V_{LOW}$ Domain

In this configuration, both $V_{HIGH}$, $V_{DDP}$[1)] and $V_{LOW}$ are supplied externally.

The High Voltage domain $V_{HIGH}$ must always be at a higher voltage level, than the Low Voltage Domain $V_{LOW}$. When PS_MDIO_VOLTAGE is LOW then $V_{DDP}$ will be at 1.8 V. In such scenario $V_{HIGH}$ must always be at a higher voltage than $V_{DDP}$ and $V_{DDP}$ must always be at a higher voltage than the Low Voltage Domain $V_{LOW}$.

$V_{HIGH}$, $V_{DDP}$[1)] and $V_{LOW}$ ramp-up times ($t_{vh\_rampup}$, $t_{vddp\_rampup}$[1)] and $t_{vl\_rampup}$) must be above the minimum requirement.

All the supply domains $V_{HIGH}$, $V_{DDP}$[1)] and $V_{LOW}$ must be stabilized before releasing the reset HRSTN.

During the power-down Sequence, $V_{HIGH}$ ramp down time must not be shorter than the minimum requirement.

The device reset HRSTN must be held for a $t_{reset}$ time after the stabilization of the power supplies and pin strap values. When reset is released, the integrated PLL locks and the device boots up.

The GPY212 supports an asynchronous hardware reset HRSTN. The timing requirements of the power supply pins are listed in **Table 35**. The timings refer to the signal sequence waveforms depicted in **Figure 17** when PS_MDIO_VOLTAGE is HIGH and **Figure 18** PS_MDIO_VOLTAGE is LOW.

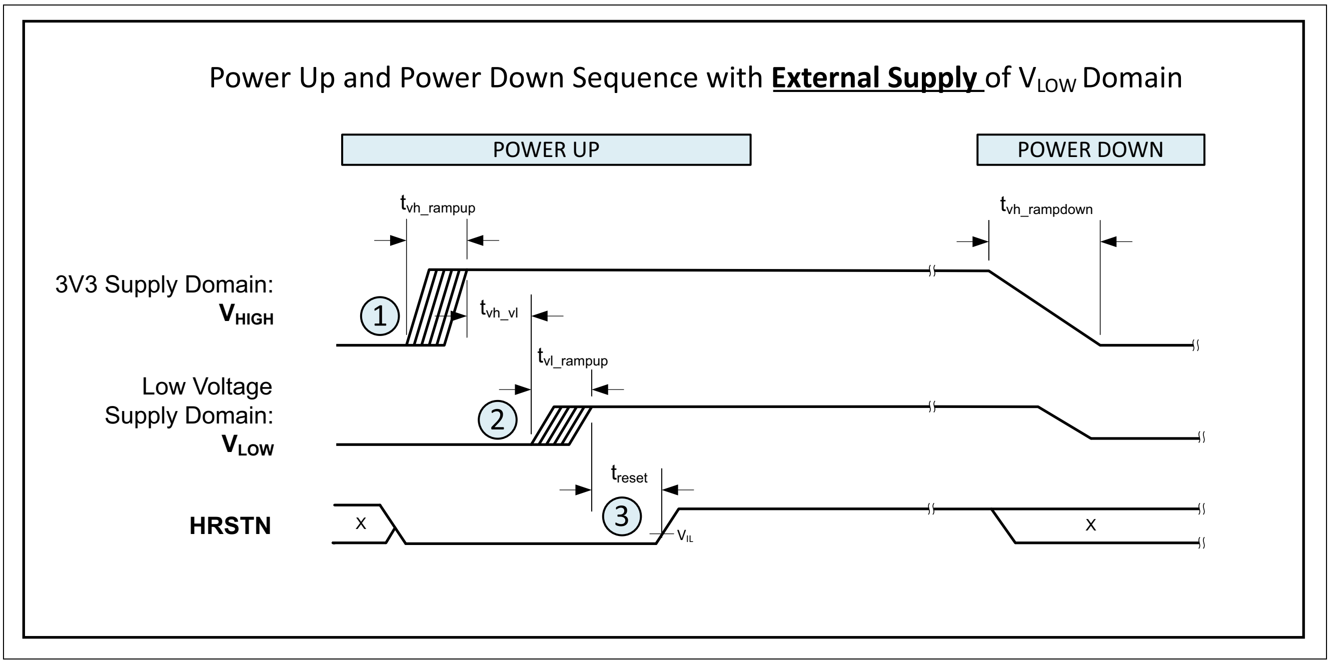



**Figure 17 Timing Diagram for the Reset Sequence (External supply of $V_{LOW}$ domain)**

1) When PS_MDIO_VOLTAGE is LOW then $V_{DDP}$ will be at 1.8 V and requirements that differentiate $V_{DDP}$ from $V_{HIGH}$ is applicable. When PS_MDIO_VOLTAGE is HIGH then $V_{DDP}$ will be treated as $V_{HIGH}$.

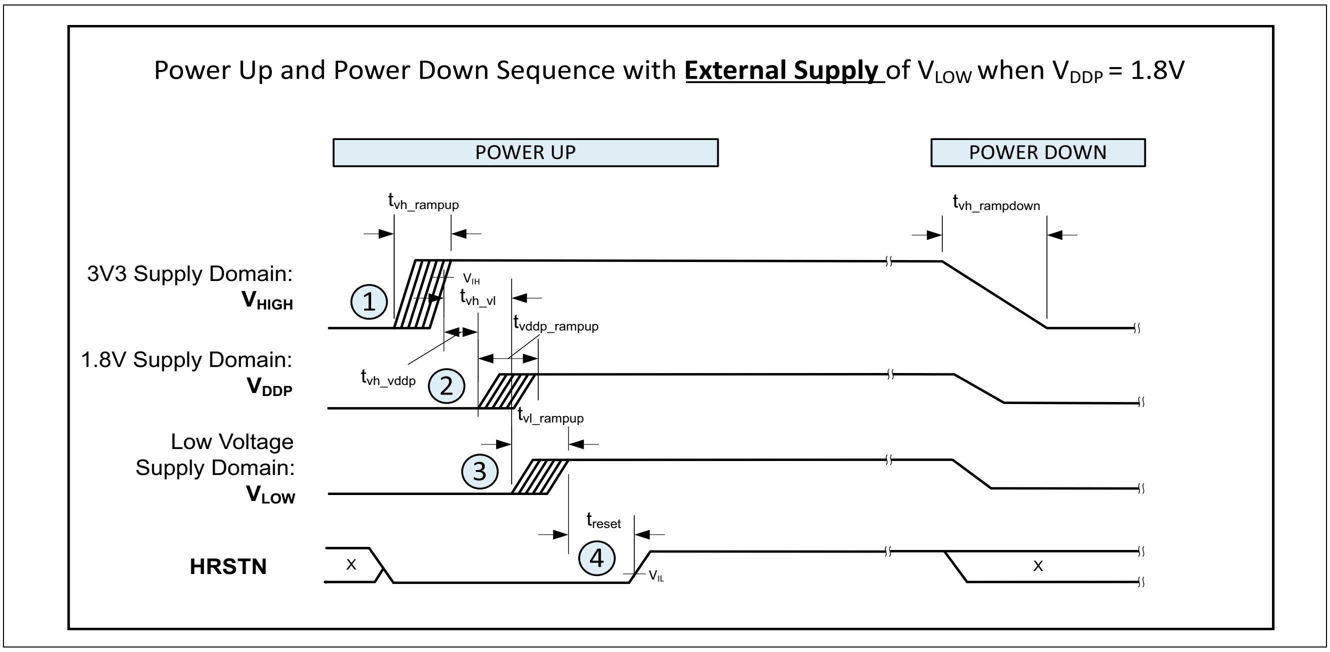



**Figure 18** Timing Diagram for the Reset Sequence (External supply of $V_{LOW}$ domain) when $V_{DDP}$=1.8 V

**Table 35** Power Supply Timings (External supply of $V_{LOW}$ domain)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{HIGH}$ domain ramp up | $t_{vh\_rampup}$ | 50 | – | – | µs | To avoid current surge. |
| $V_{DDP}$ 1) domain ramp up | $t_{vddp\_rampup}$ | 50 | – | – | µs | To avoid current surge. |
| $V_{LOW}$ domain ramp up | $t_{vl\_rampup}$ | 50 | – | – | µs | To avoid current surge. |
| Delay between $V_{HIGH}$ and $V_{LOW}$ domains voltage ramp up | $t_{vh\_vl}$ | 100 | - | - | µs | The $V_{LOW}$ voltage must never be higher than $V_{HIGH}$ voltage |
| Delay between $V_{HIGH}$ and $V_{DDP}$ 1) domains voltage ramp up | $t_{vh\_vddp}$ | 50 | - | - | µs | The $V_{DDP}$ voltage must never be higher than $V_{HIGH}$ voltage. |
| $V_{HIGH}$ domain ramp down | $t_{vh\_rampdown}$ | 1.0 | – | – | ms | The $V_{LOW}$ voltage must never be higher than $V_{HIGH}$ voltage . |
| Reset time after $V_{HIGH}$ and $V_{LOW}$ domains are stabilized | $t_{reset}$ | 100 | – | – | ns | HRSTN must be released after the power supplies have stabilized. |

Rise and ramp down times are from 10% to 90% marks for $V_{HIGH}$, $V_{LOW}$ and HRSTN.

### 7.5.2 Power Up and Power Down Sequence in Internal DCDC SVR Configuration

In internal DCDC SVR configuration, the High Voltage domain $V_{HIGH}$, $V_{DDP}$[1)] and the HRSTN need to be controlled externally. The $V_{LOW}$ domain is supplied by the DCDC_REGO outputs of the internal SVR.

$V_{HIGH}$, $V_{DDP}$[1)] domain ramp-up time $t_{vh\_rampup}$, $t_{vddp\_rampup}$[1)] must not be too short.

$V_{HIGH}$ domain must be stabilized for $t_{reset}$ time before releasing the reset HRSTN.

When reset is released, the integrated SVR generates the DCDC_REGO which supplies the $V_{LOW}$ domain. Subsequently, integrated PLL locks and the device boots up.

During the power-down sequence, $V_{HIGH}$ ramp down time $t_{vh\_rampdown}$ must be higher than the minimum requirement.

The timing requirements of the power supply pins are listed in **Table 36**. The timings refer to the signal sequence waveforms depicted in **Figure 19** when PS_MDIO_VOLTAGE is HIGH and **Figure 20** PS_MDIO_VOLTAGE is LOW.

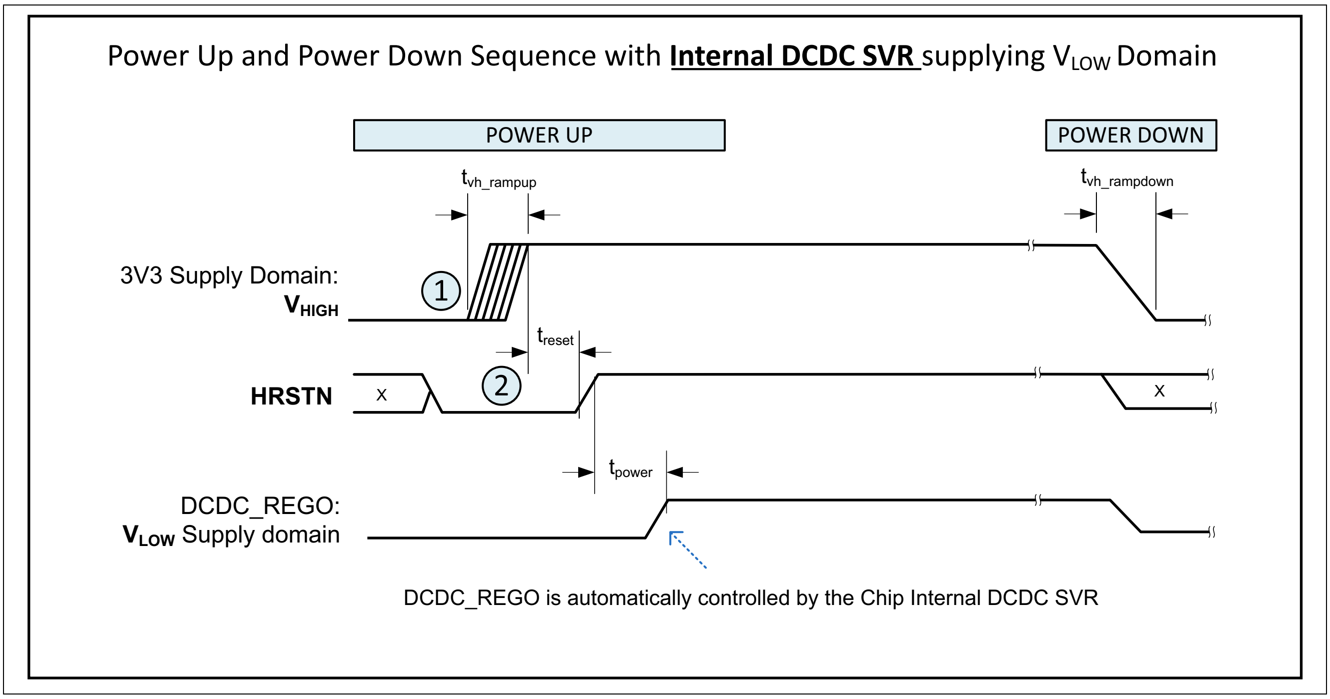



**Figure 19 Timing Diagram for the Reset Sequence (Internal DCDC SVR Configuration)**

1) When PS_MDIO_VOLTAGE is LOW then $V_{DDP}$ will be at 1.8 V and requirements that differentiate $V_{DDP}$ from $V_{HIGH}$ is applicable. When PS_MDIO_VOLTAGE is HIGH then $V_{DDP}$ will be treated as $V_{HIGH}$.

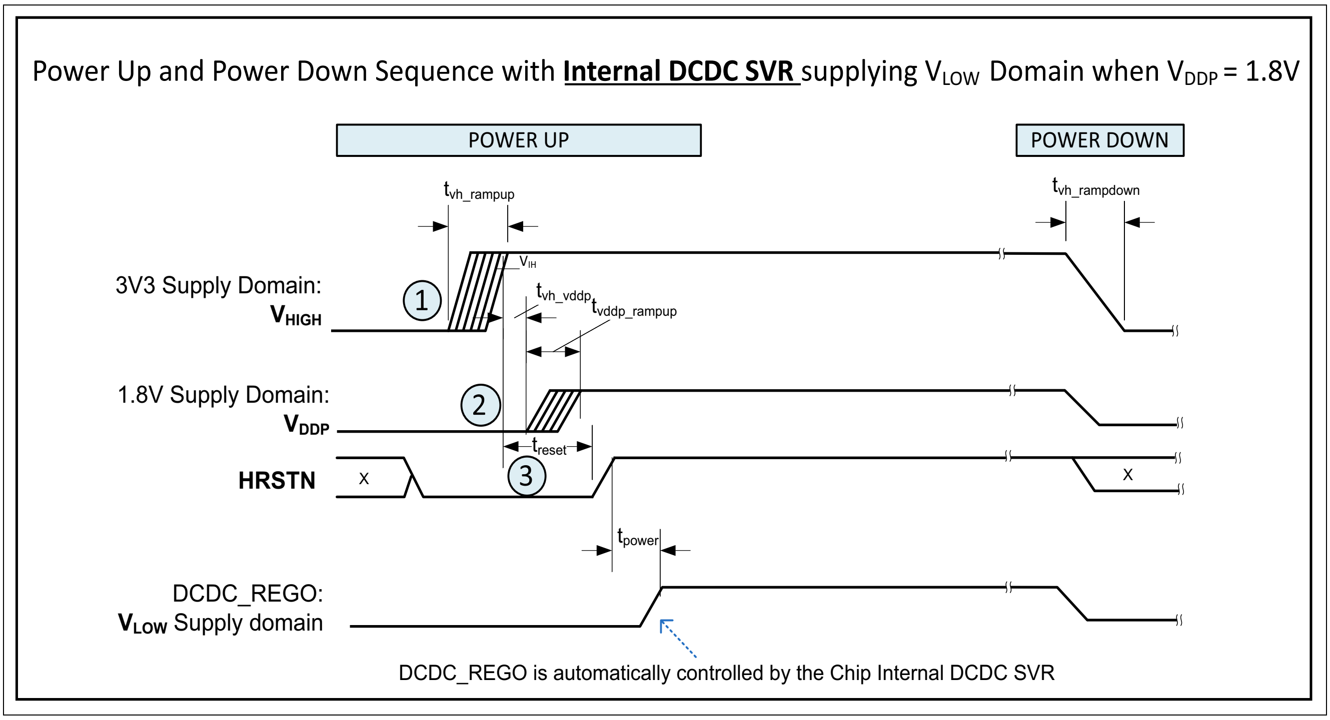



**Figure 20 Timing Diagram for the Reset Sequence (Internal DCDC SVR Configuration) when $V_{DDP}$=1.8 V**

**Table 36 Power Supply Timings (Internal DCDC SVR Configuration)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{HIGH}$ domain ramp up | $t_{vh\_rampup}$ | 50.0 | – | – | µs | To avoid current surge. |
| $V_{HIGH}$ domain ramp down | $t_{vh\_rampdown}$ | 1.0 | – | – | ms | - |
| $V_{DDP}$[1)] domain ramp up | $t_{vddp\_rampup}$ | 50 | – | – | µs | To avoid current surge. |
| Delay between $V_{HIGH}$ and $V_{DDP}$[1)] domains voltage ramp up | $t_{vh\_vddp}$ | 50 | - | - | µs | The $V_{DDP}$ voltage must never be higher than $V_{HIGH}$ voltage. |
| Reset Time | $t_{reset}$ | 500 | – | – | µs | HRSTN must be released after stabilization of $V_{HIGH}$ domain. |
| DCDC_REGO ramp up (indication) | $t_{power}$ | – | 2 | 5.0 | ms | Indicative of the maximum time for the internal DC/DC converter to stabilize DCDC_REGO low voltage after HRSTN is released. This is internally controlled by the chip, thus it is not an external system requirement. |

Rise and ramp down times are from 10% to 90% marks for $V_{HIGH}$, $V_{LOW}$ and HRSTN.

### 7.5.3 Power Supply Rail Requirements

Table 37 lists the required characteristics of the power supplies.

**Table 37 AC Characteristics of the Power Supply**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Power Supply Ripple on VDDA0V9 | $R_{VDDA0V9}$ | – | – | 60.0 | mV | Peak to Peak value |
| Power Supply Ripple on VP | $R_{VP}$ | – | – | 60.0 | mV | Peak to Peak value |
| Power Supply Ripple on VDD | $R_{VDD}$ | – | – | 60.0 | mV | Peak to Peak value |
| Power Supply Ripple on VDDP | $R_{VDDP}$ | – | – | 100.0 | mV | Peak to Peak value |
| Power Supply Ripple on VDDA3V3 | $R_{VDDA3V3}$ | – | – | 100.0 | mV | Peak to Peak value |
| Power Supply Ripple on VDDA3V3XO | $R_{VDDA3V3XO}$ | – | – | 100.0 | mV | Peak to Peak value |
| Power Supply Ripple on VDDA3V3CDB | $R_{VDDA3V3CDB}$ | – | – | 100.0 | mV | Peak to Peak value |
| Power Supply Ripple on VDDA3V3AON | $R_{VDDA3V3AON}$ | – | – | 100.0 | mV | Peak to Peak value |
| Power Supply Ripple on VPH | $R_{VPH}$ | – | – | 100.0 | mV | Peak to Peak value |
| Power Supply Ripple on VDD3V3DCDC | $R_{VDD3V3DCDC}$ | – | – | 100.0 | mV | Peak to Peak value |

### 7.5.4 MDIO Interface

Figure 21 shows a timing diagram of the slave MDIO interface for a clock cycle in the read, write and turnaround modus. The timing measurements are annotated. The defined absolute values are summarized in Table 38.

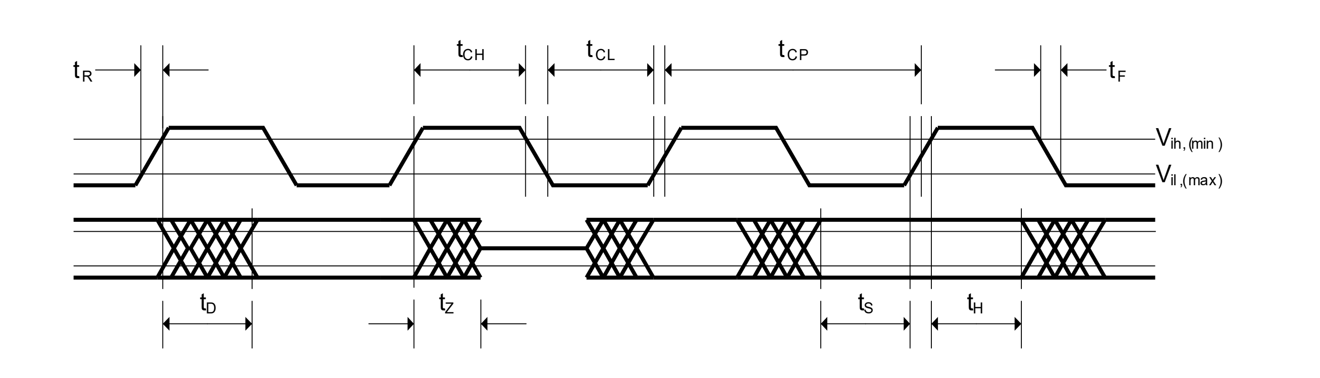



**Figure 21 Timing Diagram for the MDIO Interface**

**Table 38 Timing Characteristics of the MDIO Interface**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| MDC High Time | $t_{CH}$ | 10.0 | – | – | ns | Given timings all refer to the MDC signal probed at the pin of the Gigabit Ethernet PHY. |
| MDC Low Time | $t_{CL}$ | 10.0 | – | – | ns | |
| MDC Clock Period | $t_{CP}$ | 40.0 | 400.0 | – | ns | |
| MDC Clock Frequency[1)] | $t_{CP}$ | – | 2.5 | 25.0 | MHz | |
| MDC Rise Time | $t_R$ | – | – | 5.0 | ns | |
| MDC Fall Time | $t_F$ | – | – | 5.0 | ns | |
| MDIO Input Setup Time | $t_S$ | 10.0 | – | – | ns | Gigabit Ethernet PHY Receive |
| MDIO Input Hold Time | $t_H$ | 10.0 | – | – | ns | Gigabit Ethernet PHY receive |
| MDIO Output Delay Time | $t_D$ | 0.0 | – | 10 | ns | Gigabit Ethernet PHY transmit |
| **Standard @2.5 MHz** | | | | | | |
| MDIO Output Delay | $t_D$ | 0.0 | – | 300.0 | ns | PHY transmit |
| MDIO Output Setup Time | $t_S$ | 10.0 | – | – | ns | MAC transmit |
| MDIO Output Hold Time | $t_H$ | 10.0 | – | – | ns | MAC transmit |

1) MDC clock supports range of frequencies up to 25 MHz. Default/typical frequency is 2.5 MHz.

### 7.5.5 SGMII Interface

This section describes the AC characteristics of the SGMII Interface on the GPY212.

The SGMII Interface timing characteristics are described below:

- Transmit timing characteristics (**Chapter 7.5.5.1**)
- Receive timing characteristics (**Chapter 7.5.5.2**)

#### 7.5.5.1 Transmit Timing Characteristics

**Figure 22** shows the timing diagram of the transmit SGMII interface on the GPY212. It is referred to by **Table 39**, which specifies the timing requirements.

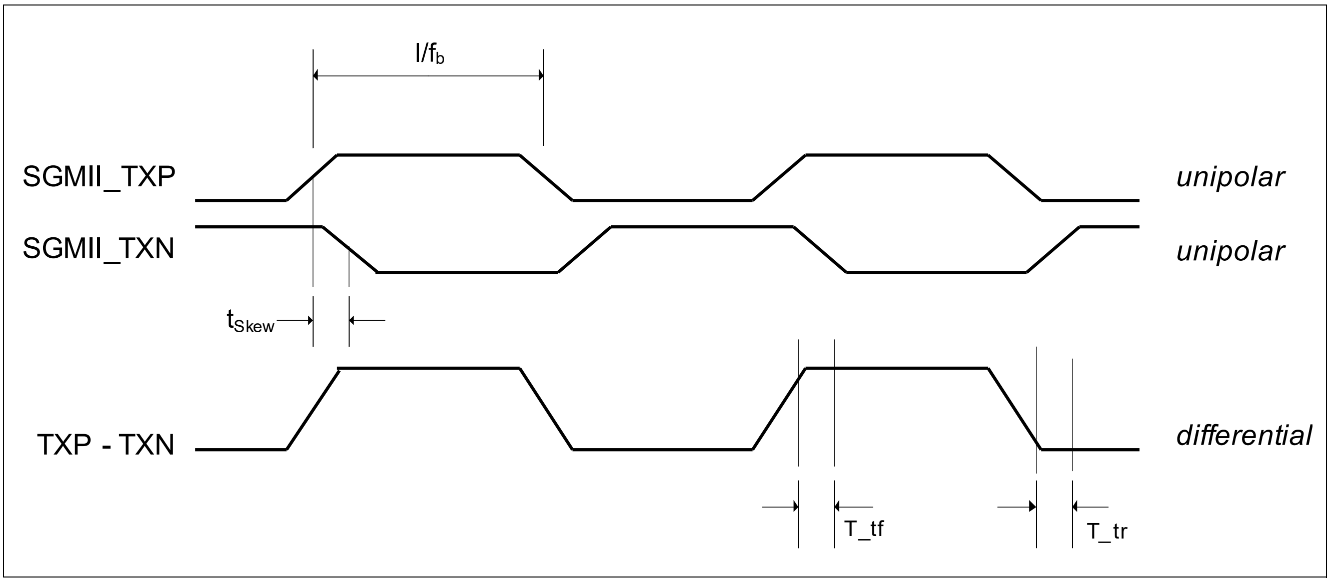



**Figure 22 Transmit Timing Diagram of the SGMII (shows alternating data sequence)**

**Table 39 Transmit Timing Characteristics of the SGMII**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Transmit baud rate | $f_b$ | -100 ppm | $f_b$ | +100 ppm | Mbaud | $f_b$ = 1.25/3.125 Gbaud |
| Differential transmit rise time | T_tr | 30 ps | – | 0.25 UI | – | 20%→80%[1)] |
| Differential transmit fall time | T_tf | 30 ps | – | 0.25 UI | – | 80%→20% |
| Output timing jitter | T_TJ | – | – | 0.30 | $UI_{pp}$[2)] | |
| Time skew between pairs | $t_{Skew}$ | – | – | 15 | ps | – |
| Output differential voltage | $V_{OD}$ | 400 | – | 1600 | mV | Peak-peak amplitude |
| Output impedance (differential) | $R_O$ | 80 | 100 | 120 | Ω | – |

1) UI = 1/$f_b$, Unit Interval.

2) Refer to [1] for details. The p-p (peak to peak) measurement states the maximum to minimum amount of time deviation.

#### 7.5.5.2 Receive Timing Characteristics

**Figure 23** shows the timing diagram of the receive SGMII interface of the GPY212. Refer to **Table 40** for the timing requirements.

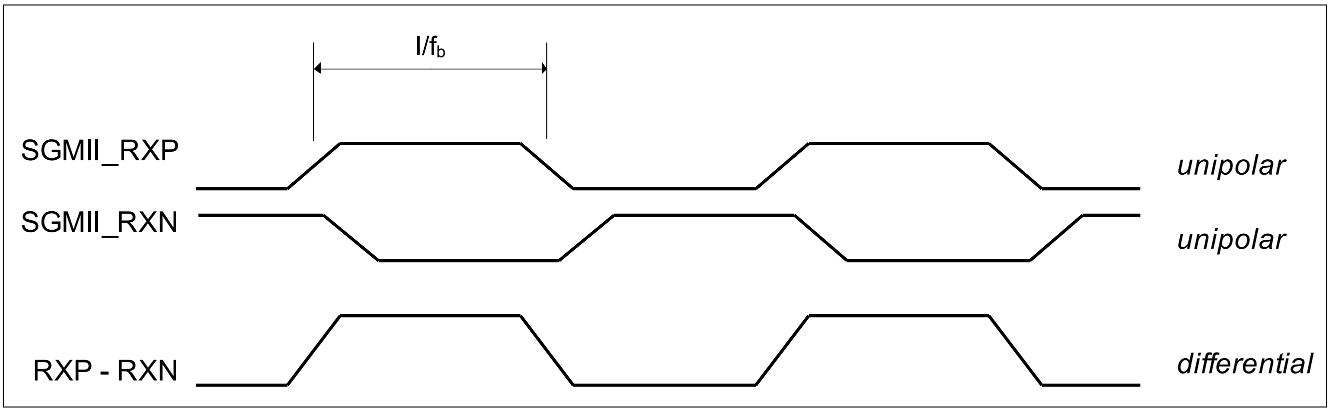



**Figure 23 Receive Timing Diagram of the SGMII (alternating data input sequence)**

**Table 40 Receive Timing Characteristics of the SGMII**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Receive baud rate | $f_b$ | -100 ppm | $f_b$ | +100 ppm | Mbaud | $f_b$ = 1.25/3.125 Gbaud |
| Receive data jitter tolerance | R_TJ | – | – | 0.6 | $UI_{pp}$ 1) | – |
| Input differential voltage | $V_{ID}$ | 200 | – | 1600 | mV | peak-peak amplitude |
| Input impedance (differential) | $R_I$ | 80 | 100 | 120 | Ω | – |

1) Refer to [1] for details.

### 7.5.6 Serial Peripheral Interface (SPI)

The SPI master interface timing is shown in **Figure 24**.

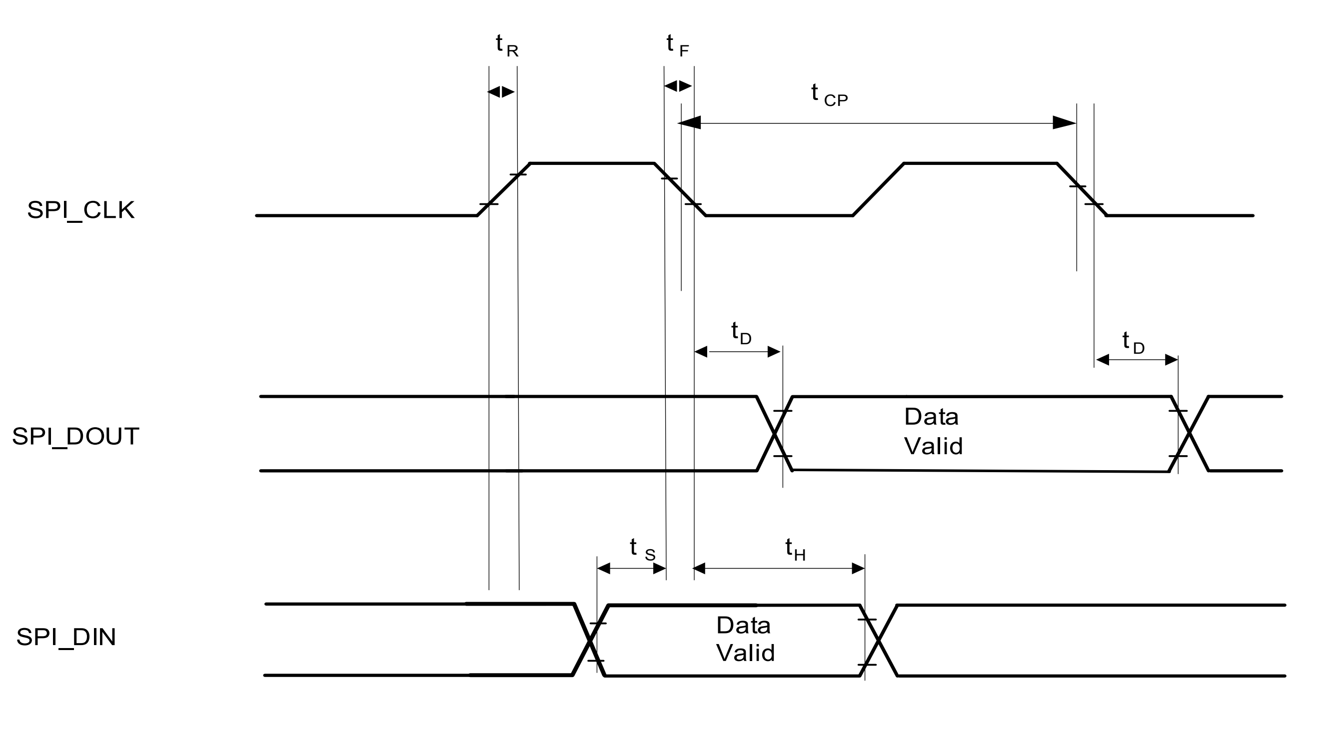



**Figure 24 SPI Master Interface Timing**

**Table 41 SPI Interface Timing Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **Master Mode** | | | | | | |
| Tx Data Output Delay | $t_D$ | 0 | – | 4 | ns | – |
| Rx Data Input Setup Time | $t_S$ | 7 | – | – | ns | – |
| Rx Data Hold Time | $t_H$ | 0 | – | – | ns | – |
| SPI Clock Period (Master Mode) | $t_{CP}$ | 20 | – | 50 | ns | - |
| SPI Clock Rise Time | $t_R$ | – | – | 5.0 | ns | 10% - 90% |
| SPI Clock Fall Time | $t_F$ | – | – | 5.0 | ns | 10% - 90% |
| SPI Clock Duty Cycle | D | 45 | – | 55 | % | – |

### 7.5.7 JTAG Interface

The JTAG interface is used for boundary scan.

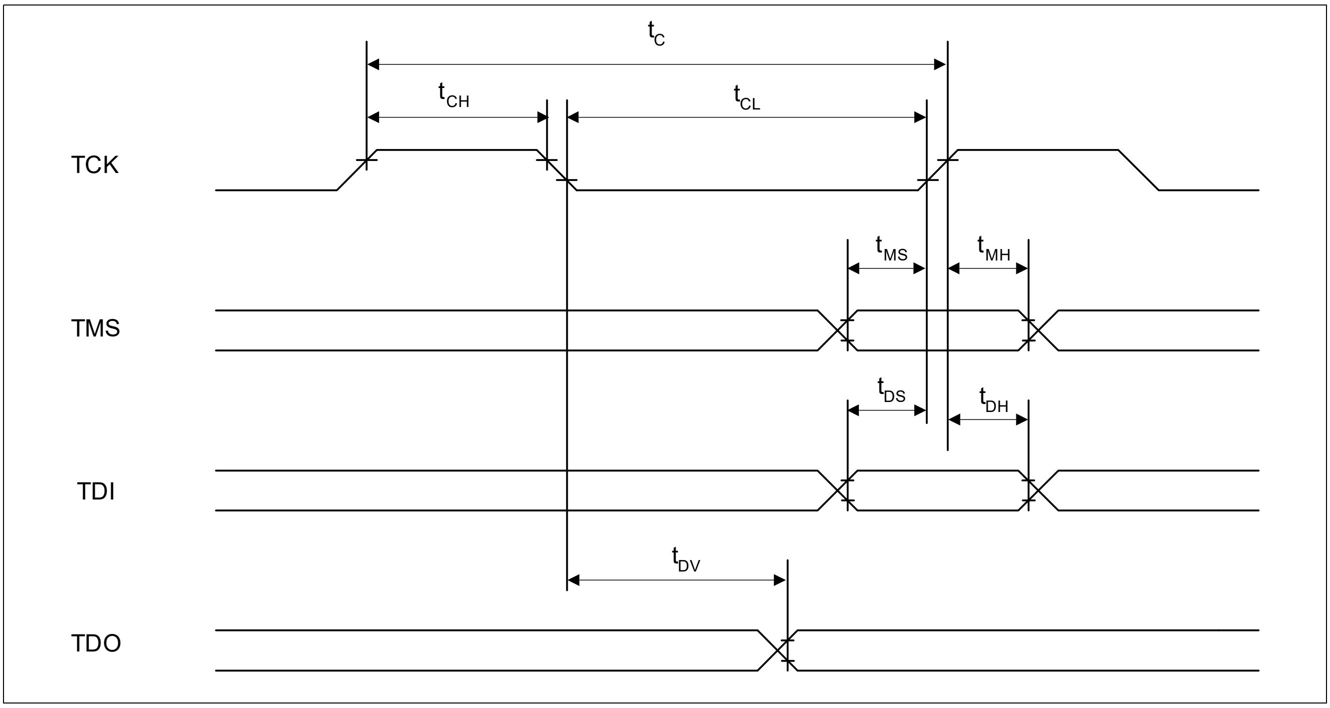



**Figure 25 JTAG Interface Timing**

The timing values are described in **Table 42** and **Table 43**.

**Table 42 JTAG Interface Clock**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TCK Clock Period | $t_C$ | 100 | – | – | ns | – |
| TCK High Time | $t_{CH}$ | 40 | – | – | ns | – |
| TCK Low Time | $t_{CL}$ | 40 | – | – | ns | – |

**Table 43 JTAG Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TMS setup time | $t_{MS}$ | 40 | – | – | ns | – |
| TMS hold time | $t_{MH}$ | 40 | – | – | ns | – |
| TDI setup time | $t_{DS}$ | 40 | – | – | ns | – |
| TDI hold time | $t_{DH}$ | 40 | – | – | ns | – |
| Hold: $\overline{TRST}$ after TCK | $t_{HD}$ | 10 | – | – | ns | – |
| TDO valid delay | $t_{DV}$ | – | – | 60 | ns | – |

### 7.5.8 Crystal Specification

The 25 MHz crystal must follow the specification given in **Table 44**.

**Table 44 Specification of the Crystal**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Frequency with 25 MHz input | $f_{clk25}$ | – | 25.0 | – | MHz | – |
| Total Frequency Stability | – | -50 | – | +50 | ppm | Refers to sum of all effects: e.g. general tolerance, aging, temperature dependency |
| Series Resonant Resistance | – | – | – | 60 | Ω | – |
| Drive Level | – | – | – | 0.1 | mW | – |
| Load Capacitance | $C_L$ | – | 18 | – | pF | – |
| Shunt Capacitance | $C_0$ | – | – | 5 | pF | – |

## 7.6 External Circuitry

This chapter specifies the component characteristics of the external circuitry connected to the GPY212.

### 7.6.1 Twisted-Pair Common-Mode Rejection and Termination Circuitry

This section describes the external circuitry that is required to properly terminate the common mode of the Twisted Pair Interface (TPI). These external components are also required to perform proper rejection of alien disturbers injected into the common mode of the TPI. **Figure 26** shows a typical external circuit, and in particular the common-mode components. **Table 45** defines the component values and their supported tolerances.

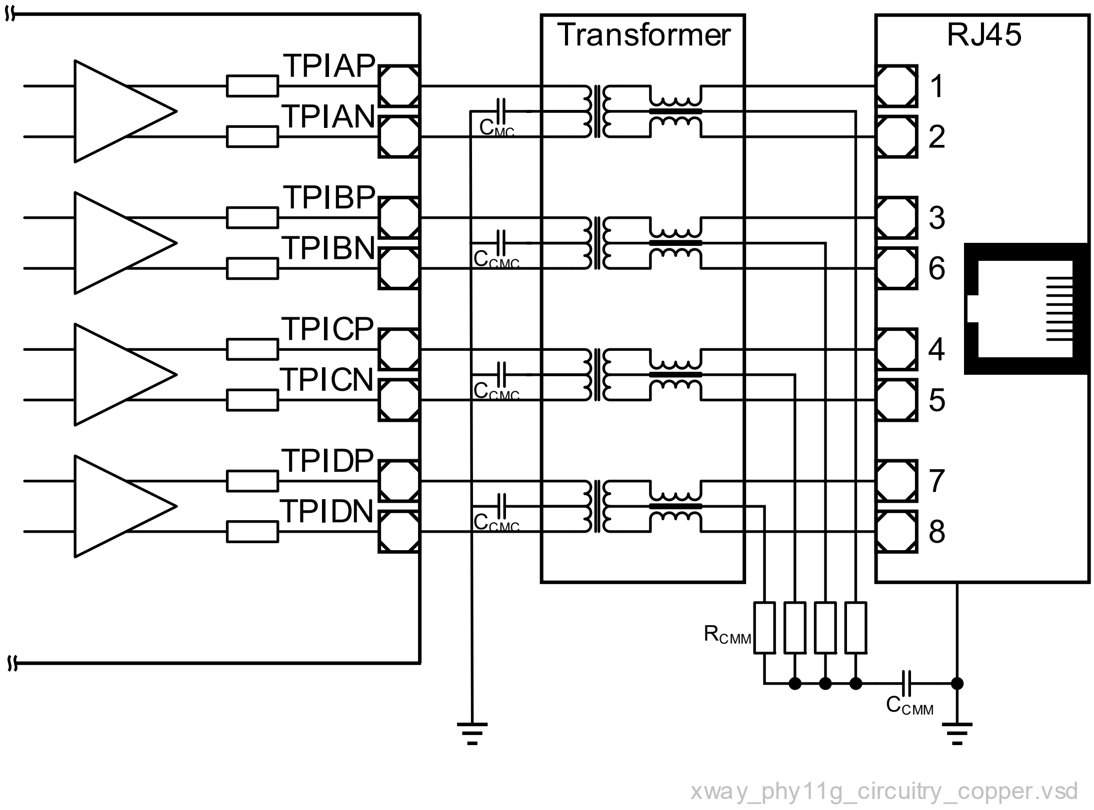



**Figure 26 Twisted Pair Common-Mode Rejection and Termination Circuitry**

**Table 45 Electrical Characteristics for Common-Mode Rejection and Termination Circuitry**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Common-mode de-coupling capacitance (media end) | $C_{CMM}$ | 800 | 1000 | 1200 | pF | ±20%, 2 kV |
| Common-mode de-coupling capacitance (chip end) | $C_{CMC}$ | 80 | 100 | 120 | nF | ±20%, 2 kV |
| Common-mode termination resistance (media end) | $R_{CMM}$ | 67.5 | 75 | 82.5 | Ω | ±10% |

### 7.6.2 Transformer (Magnetics)

This section specifies the required electrical characteristics of the transformer[1] devices that are supported. The specifications listed here guarantee proper operation according to IEEE 802.3 [2].

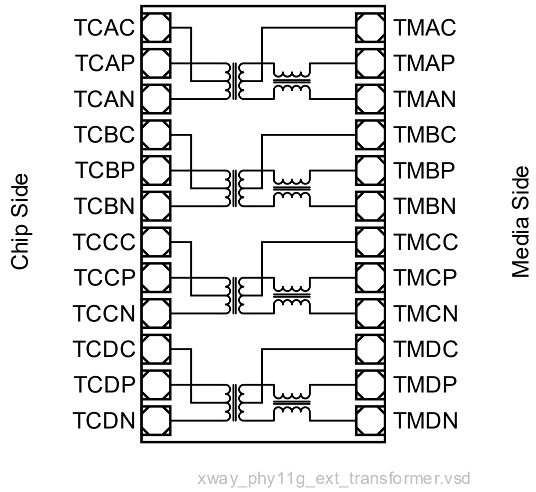



**Figure 27 Schematic of an Ethernet Transformer Device**

A typical Gigabit Ethernet capable transformer device is depicted in Figure 27. Table 46 lists the characteristics of the supported transformer devices. Note that these characteristics represent the minimum for achieving standard performance. Since the transformer significantly impacts the link performance, it is possible to increase the loop reach by selecting transformers with improved parameters.

**Table 46 Electrical Characteristics for Supported Transformers (Magnetics)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Turns Ratio | 1:tr | 0.95 | 1.00 | 1.05 | | ±5% |
| Differential-to-common-mode rejection | DCMR | 40 | – | – | dB | 30 MHz |
| | | 35 | – | – | dB | 60 MHz |
| | | 30 | – | – | dB | 100 MHz |
| Crosstalk attenuation | CTA | 45 | – | – | dB | 30 MHz |
| | | 40 | – | – | dB | 60 MHz |
| | | 35 | – | – | dB | 100 MHz |
| Insertion loss | IL | – | – | 1 | dB | 1 MHz ≤ f ≤ 250 MHz |
| Return loss | RL | 16 | – | – | dB | 1 MHz ≤ f ≤ 40 MHz |
| Return loss | RL | 16-10*log10(f/40) | – | – | dB | 40 MHz ≤ f ≤ 125 MHz |

1) Also often referred to as “magnetics”.

### 7.6.3 RJ45 Plug

**Table 47** describes the electrical characteristics of the RJ45 plug to be used in conjunction with the GPY212.

**Table 47 Electrical Characteristics for Supported RJ45 Plugs**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Crosstalk attenuation | CTA | 45 | – | – | dB | 30 MHz |
| | | 40 | – | – | dB | 60 MHz |
| | | 35 | – | – | dB | 100 MHz |
| Insertion loss | IL | – | – | 1 | dB | 1 MHz ≤ f ≤ 250 MHz |
| Return loss | RL | 16 | – | – | dB | 1 MHz ≤ f ≤ 40 MHz |
| Return loss | RL | 16-10*log10(f/40) | – | – | dB | 40 MHz ≤ f ≤ 250 MHz |

### 7.6.4 Calibration Resistors

An external resistor $R_{CAL}$ of 22 kΩ 1% must be connected between the RCAL pin and ground to calibrate the GPY212 Ethernet analog modules.

Additionally, an external resistor $R_{RESREF}$ of 200 Ω 1% must be connected between the RESREF pin and ground to calibrate the GPY212 SGMII analog modules.

The resistor values are indicated in **Table 48**.

**Table 48 Calibration Resistors Values**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| GPY212 calibration resistor | $R_{CAL}$ | 21780 | 22000 | 22220 | Ω | ±1% |
| SGMII PHY calibration resistor | $R_{RESREF}$ | 198 | 200 | 202 | Ω | ±1% |

## 7.7 Power Supply

Due to its integrated DC/DC SVR converter, the GPY212 can be powered using a single power supply, as described in the next section. However, the device can also be powered without the integrated DC/DC converter. **Figure 28** and **Figure 29** show the high-level principle of circuitry. For more details, refer to Reference Board Hardware Design Guide **[7]**.

### 7.7.1 Power Supply Using Integrated DC/DC SVR Converter

The GPY212 can be powered using a single 3.3 V supply when the integrated DC/DC converter is used. As long as the applied nominal voltage remains within the operating range specified in **Chapter 7.2**, the device operates automatically and without the need for additional settings to be applied. Only minor external circuitry is required to enable this feature. **Figure 28** shows an example schematic. The electrical characteristics of the power supply are defined in **Chapter 7.2**.

The required values for the external components are listed in **Table 49**.

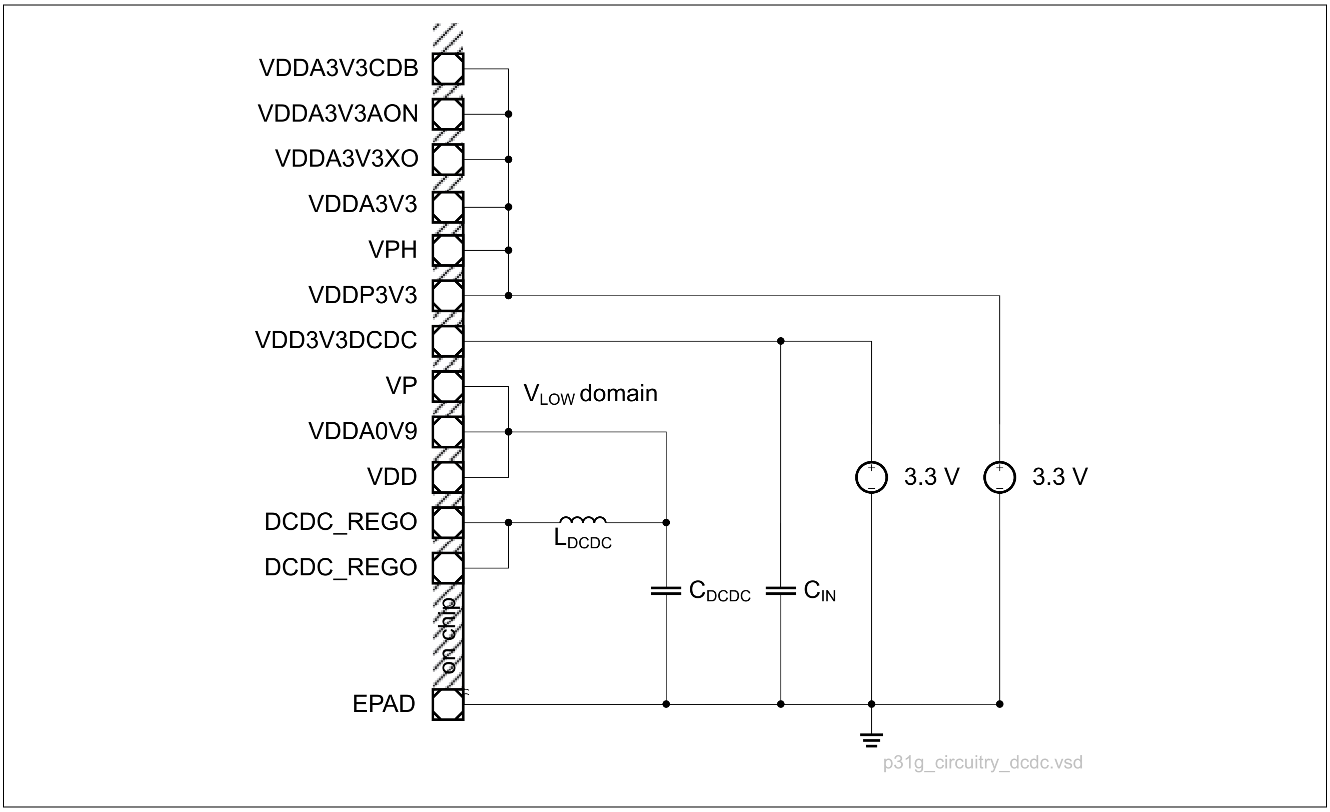



**Figure 28 External Circuitry Using the Integrated DC/DC Converter**

**Table 49 External Component Values for DC/DC Converter**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| DC/DC buck inductance | $L_{DCDC}$ | – | 1.0 | – | µH | $DCR_{max}$= 0.07 ohm |
| DC/DC smoothing capacitance | $C_{DCDC}$ | – | 2 x 22 | – | µF | Refer to [7] for exact reference circuitry |
| | | | 1 x 330 | | pF | |
| DC/DC input capacitance | $C_{IN}$ | – | 10.0 | – | µF | Refer to [7] for exact reference circuitry |
| | | | 22 | | | |
| | | | 0.1 | | | |

### 7.7.2 Power Supply without using Integrated DC/DC Converter

When the integrated DC/DC converter is not used, for example when both power supply voltages are already available in the system, the GPY212 can be powered by a dual power supply, as shown in **Figure 29**. The electrical characteristics of the power supply are defined in **Chapter 7.2**.

In external supply mode, the DC/DC converter output pins are left unconnected. The integrated DC/DC converter can then be switched off after power up. Note that **Figure 29** is only a generic schematic, and does not show power supply blocking for reasons of simplicity.

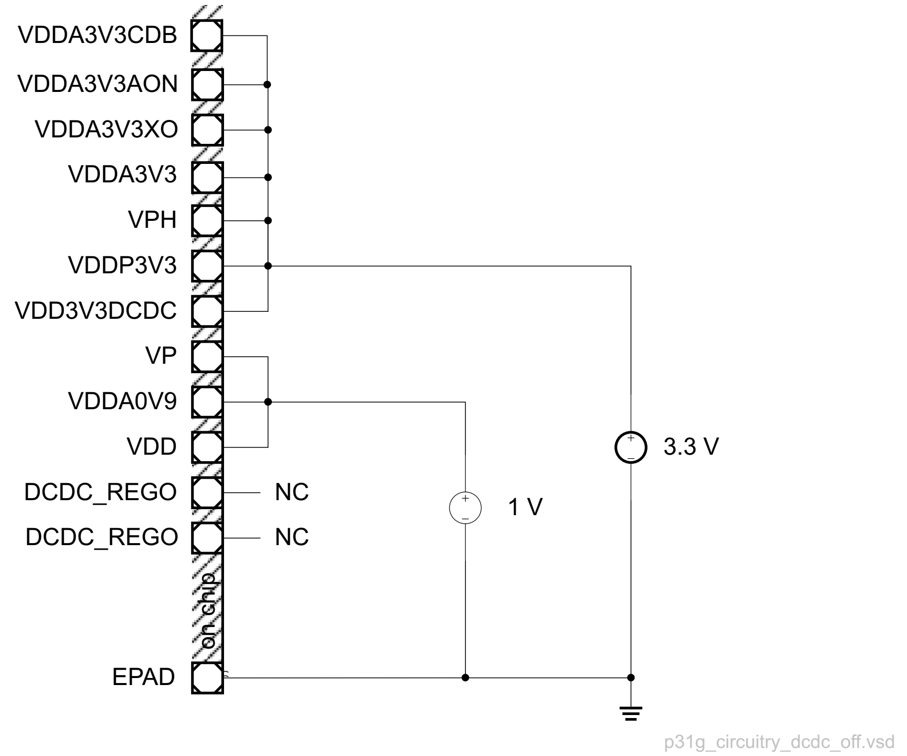



**Figure 29 External Circuitry without using the Integrated DC/DC Converter**

# 8 Package Outline

The product is assembled in a PG-VQFN-56 package, which complies with regulations requiring lead free material. The following parameters are generated in accordance with JEDEC JESD51 standards **[8]**. Three models are provided:

- in natural convection environment, still air (**Table 50**)
- with a thermal solution setting chip top temperature at 70°C (**Table 51**)
- according to compact 2-R model (**Table 52**)

**Table 50 JEDEC Thermal Resistance Package Parameter - Still air conditions**

| Item | Name/Value |
|---|---|
| Environmental conditions | The chip is mounted on a 4-layer PCB (2S2P) according to JESD51-7 **[8]**, PCB size 76.2x114 mm<br>Natural convection: still air, according to JESD51-2 **[8]**<br>Ambient temperature: 85°C |
| Thermal Resistance - Junction to Ambient | $R_{th,\ JA}$ = 23 K/W |
| Thermal Delta - Junction to Case Top | $Psi_{JCTop}$ = 0.53 K/W |

**Table 51 JEDEC Thermal Resistance Package Parameter - With Thermal Solution Environment**

| Item | Name/Value | Environment |
|---|---|---|
| Thermal Resistance Junction to Case Top | $R_{th,\ JCtop}$ = 18.2 K/W | Cold plate on package top surface.<br>Temp = 70°C.<br>PCB with 16 thermal vias |
| Thermal Resistance - Junction to Case Bottom | $R_{th,\ JB}$ = 12.8 K/W | As per JESD51-8 **[8]**<br>Ring style cold plate on PCB around 3 mm from package edge.<br>Temp = 70°C.<br>PCB with 16 thermal vias. |

**Table 52 JEDEC Thermal Resistance Package Parameter - Compact 2-R Model Network**

| Item | Name/Value |
|---|---|
| Thermal Resistance Junction to Case Top | $R_{th,\ JCtop}$ = 24.6 K/W |
| Thermal Resistance - Junction to Case Bottom | $R_{th,\ JCbottom}$ = 5.24 K/W |

The mechanical drawings for this package are shown in **Figure 30**. Dimensions are in millimeters.

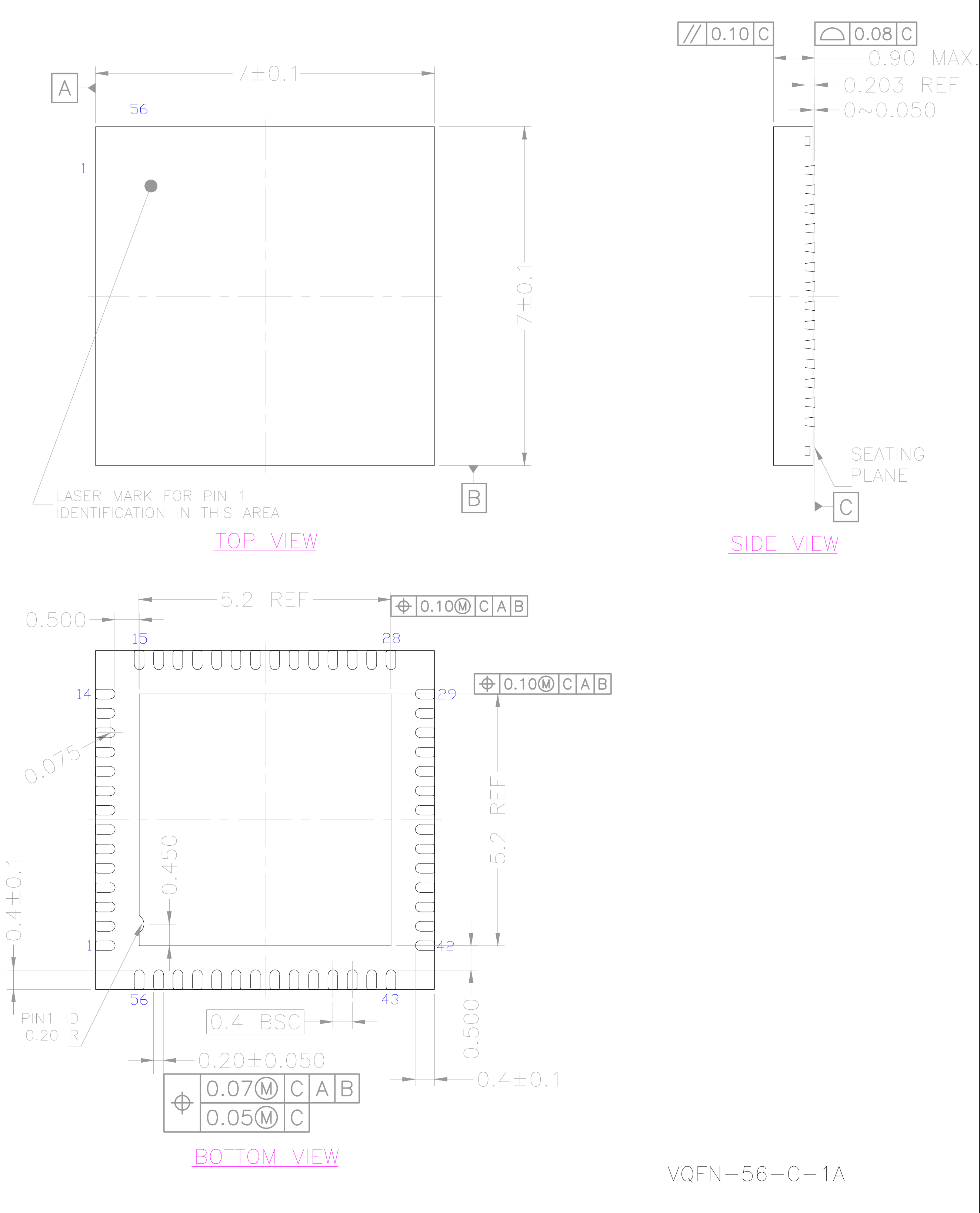



**Figure 30 PG-VQFN-56 7 mm x 7 mm Package Outline**

## 8.1 Chip Identification and Ordering Information

**Figure 31** shows an example of the marking pattern on the Gigabit Ethernet PHY GPY212 device. The actual chip marking may differ slightly from the illustration.

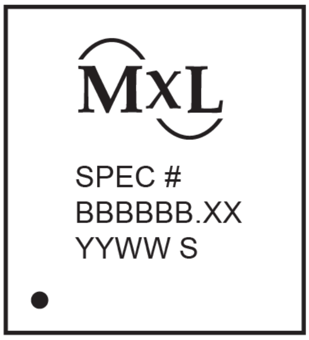



**Figure 31 Example of Chip Marking**

**Table 53** explains the chip marking information, **Table 54** provides chip ordering information for GPY212C0VC, and **Table 55** provides chip ordering information for GPY212B1VC.

**Table 53 Chip Marking Pattern**

| Marking | Description |
|---|---|
| Text Line 1 | MaxLinear Logo |
| Text Line 2 | Spec. Number - See **Table 54** (GPY212C0VC) and **Table 55** (GPY212B1VC) |
| Text Line 3 | Wafer Lot Number |
| Text Line 4 | Date Code (YYWW) and Assembly Site Code (S) |

**Table 54 Product Naming (GPY212C0VC)**

| Product Name | Ordering Code | S-Spec#[1] | MMID | OTP Firmware Version | Device Number[2] | Device Revision Number[3] | PHY Identifier[4] |
|---|---|---|---|---|---|---|---|
| GPY212 | GPY212C0VC | SLNW9 | 99AFC7 | 0x886F | 0x22 | 0x0 | 0xDE20 |

1) Marking of Engineering Sample is QW7Z with MMID xxxxx. OTP, Device Number, Device Revision Number and PHY Identifier identical to S-Spec part.
2) LDN field in CL22 and CL45 registers.
3) LDRN field in CL22 and CL45 registers.
4) PHY Identifier 2 register 16-bit value.

**Table 55 Product Naming (GPY212B1VC)**

| Product Name | Ordering Code | S-Spec# | MMID | OTP Firmware Version | Device Number[1] | Device Revision Number[2] | PHY Identifier[3] |
|---|---|---|---|---|---|---|---|
| GPY212 | GPY212B1VC | SLN8B | 999T0Z | 0x8730 | 0x20 | 0x9 | 0xDE09 |
| GPY212 | GPY212B1VC | SLNHD | 999X4H | 0x8747 | 0x20 | 0xB | 0xDE0B |

1) LDN field in CL22 and CL45 registers.
2) LDRN field in CL22 and CL45 registers.
3) PHY Identifier 2 register 16-bit value.

# Terminology

| | |
|---|---|
| **A** | |
| ADS | Auto-Downspeed |
| ANEG | Auto-Negotiation |
| ANSI | American National Standards Institute |
| **B** | |
| BER | Bit Error Rate |
| BW | Bandwidth |
| **C** | |
| CAT5 | Category 5 Cabling |
| CCR | Configuration Content Record |
| CDR | Clock and Data Recovery |
| CRC | Cyclic Redundancy Check |
| CSR | Configuration Signature Record |
| CRS | Carrier Sense |
| **D** | |
| DEC | Digital Echo Canceler |
| **E** | |
| ECM | Externally Controlled Mode (LED) |
| EEE | Energy-Efficient Ethernet |
| EEPROM | Electrically Erasable Programmable ROM |
| EMI | Electromagnetic Interference |
| ESD | Electrostatic Discharge |
| **F** | |
| FFU | Field Firmware Upgrade |
| FLP | Fast Link Pulse |
| FO | Fiber-Optic |
| **G** | |
| GbE | Gigabit Ethernet |
| GBIC | Gigabit Interface Converter |
| GMII | Gigabit Media-Independent Interface |
| GPIO | General Purpose Input/Output |
| **H** | |
| HBM | Human Body Model |
| HSTL | High-Speed Transceiver Logic |
| HYB | Hybrid |
| **I** | |
| IC | Integrated Circuit |
| ICM | Internally Controlled Mode (LED) |

| | |
|---|---|
| ICV | Integrity Check Value |
| IEEE | Institute of Electrical and Electronics Engineers |
| IPG | Inter-Packet Gap |
| **J** | |
| JTAG | Joined Test Action Group |
| **L** | |
| LAN | Local Area Network |
| LED | Light Emitting Diode |
| LPI | Low Power Idle |
| LSB | Least Significant Bit |
| **M** | |
| MAC | Media Access Controller |
| MDI | Media-Dependent Interface |
| MDIO | Management Data Input/Output |
| MDIX | Media-Dependent Interface Crossover |
| MII | Media-Independent Interface |
| MMD | MDIO Manageable Device |
| MoCA | Multimedia over Coax Alliance |
| MSB | Most Significant Bit |
| **N** | |
| NAS | Network Attached Storage |
| NLP | Normal Link Pulse |
| NP | Next Page |
| **O** | |
| OSI | Open Systems Interconnection |
| OTP | One-Time Programmable Memory |
| OUI | Organizationally Unique Identifier |
| **P** | |
| PCB | Printed Circuit Board |
| PCS | Physical Coding Sublayer |
| PD | Powered Device |
| PHY | Physical Layer (device) |
| PICMG | PCI Industrial Computer Manufacturers Group |
| PLL | Phase-Locked Loop |
| PMA | Physical Media Attachment |
| PON | Passive Optical Network |
| PPS | Pulse Per Second |
| PTS | Precision Time Protocol |
| PSE | Power-Sourcing Equipment |
| **R** | |

| | |
|---|---|
| RX | Receive |
| **S** | |
| SA | Secure Association |
| SC | Secure Channel |
| SerDes | Serializer-Deserializer |
| SFD | Start-of-frame Delimiter |
| SFP | Small Form-Factor Pluggable |
| SGMII | Serial Gigabit Media-Independent Interface |
| SMD | Surface Mounted Device |
| SoC | System on Chip |
| STA | Station Management Entity (MAC SoC) |
| SVR | Switching Voltage Regulator (Internal DCDC) |
| **T** | |
| TAP | Test Access Port |
| TPI | Twisted Pair Interface |
| TsSync | Time Stamp Synchronization |
| TX | Transmit |
| **V** | |
| VQFN | Very Thin Quad Flat Non-leaded |
| **W** | |
| Wi-Fi | Wireless Local Area Network |
| WoL | Wake-on-LAN |
| **X** | |
| xMII | Symbolic shortening which denotes the set of supported MII Interfaces, e.g. RGMII and SGMII |

# References

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[2] IEEE 802.3-2018: “Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications”, IEEE Computer Society

[3] IEEE 802.3bz-2016 “Amendment 7: Media Access Control Parameters, Physical Layers, and Management Parameters for 2.5 Gb/s and 5 Gb/s Operation, Types 2.5GBASE-T and 5GBASE-T”, IEEE Computer Society

[4] Serial-GMII Specification: Revision 1.8, Cisco* Systems, November 2 2005

[5] Sync-E Jitter and Wander specification ITU-T G.8262: “Timing characteristics of a synchronous Ethernet equipment slave clock”

[6] IEEE 1588-2008: “IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems”

[7] Ethernet Network Connection EASY GPY211 LBB Reference Board V1.3.1 HDK HW7.02 Hardware Design Guide Rev. 1.0

[8] JEDEC STANDARD, JESD 51 Methodology for the Thermal Measurement of Component Packages

[9] Ethernet Network Connection GPY API Programmer's Guide Rev. 3.0