XR620A
Instrumentation Amplifier

General Description

The XR620A is a low power, general purpose instrumentation amplifier with a gain range of 1 to 10,000. The XR620A is offered in 8-lead SOIC or DIP packages and requires only one external gain setting resistor making it smaller and easier to implement than discrete, 3-amp designs.

While consuming only 2.2mA of supply current, the XR620A offers a low 6.6nV/Hz input voltage noise and 0.2µVpp noise from 0.1Hz to 10Hz.

The XR620A offers a low input offset voltage of ±125µV that only varies 0.1µV/°C over it's operating temperature range of -40°C to +85°C. The XR620A also features 50ppm maximum nonlinearity. These features make it well suited for use in data acquisition systems.

FEATURES

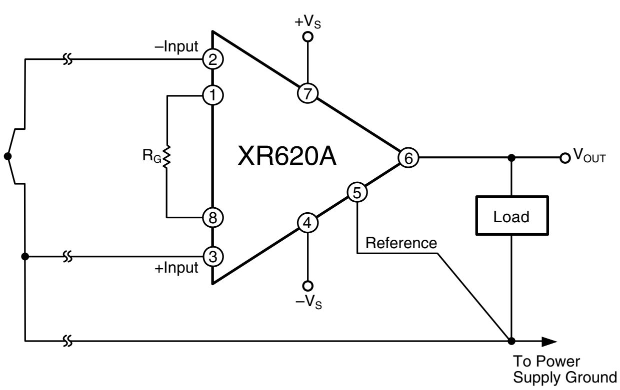
- ±2.3V to ±18V supply voltage range
- Gain range of 1 to 10,000
- Gain set with one external resistor
- ±125µV maximum input offset voltage
- 0.1µV/°C input offset drift
- 700kHz bandwidth at G = 1
- 1.2V/µs slew rate
- 90dB minimum CMRR at G = 10
- 2.2mA maximum supply current
- 6.6nV/√Hz input voltage noise
- 70nV/√Hz output voltage noise
- 0.2µV_{pp} input noise (0.1Hz to 10Hz)
- DIP-8 or Pb-free SOIC-8

APPLICATIONS

- Bridge amplifier
- Weigh scales
- Thermocouple amplifier
- ECG and medical instrumentation
- MRI (Magnetic Resonance Imaging)
- Patient monitors
- Transducer interface
- Data acquisition systems
- Strain gauge amplifier
- Industrial process controls

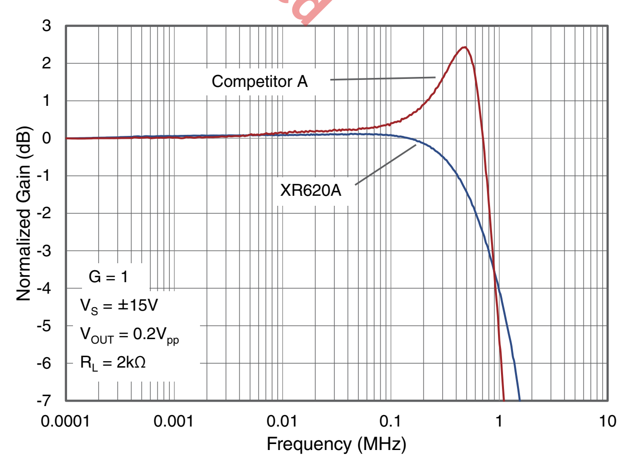
Ordering Information - back page

Typical Application



Thermocouple Amplifier

Competitive Plot



Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Supply Voltage .... ±18V
Input Voltage Range .... $\pm V_S$ V
Differential Input Voltage (G = 1 to 10) 25V
Differential Input Voltage (G > 10) .... $\leq 0.05 (R_G + 800) + 1$ V
Load Resistance (min) 1Ω

Operating Conditions

Supply Voltage Range .... ±2.3V to ±18V (4.6V to 36V)
Gain Range .... 1 to 10,000
Operating Temperature Range .... -40°C to 85°C
Junction Temperature .... 150°C
Storage Temperature Range .... -65°C to 150°C
Lead Temperature (Soldering, 10s) .... 260°C

Package Thermal Resistance

θ_{JA} (DIP-8) .... 100°C/W
θ_{JA} (SOIC-8) .... 150°C/W

Package thermal resistance (θ_{JA}), JEDEC standard, multi-layer test boards, still air.

ESD Protection

SOIC-8 (HBM) 1.5kV

ESD Rating for HBM (Human Body Model).

Electrical Characteristics

T_A = 25°C, V_S = ±15V, R_L = 2kΩ to GND; unless otherwise noted. Gain = 1 + (49.4k/R_G); Total RTI Error = V_{OSI} + (V_{OSO}/G)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Gain						
	Gain Range		1		10,000	
	Gain Error (1)	G = 1, V_{OUT} = ±10V	-0.1		0.1	%
		G = 10, V_{OUT} = ±10V	-0.375		0.375	%
		G = 100, V_{OUT} = ±10V	-0.375		0.375	%
		G = 1,000, V_{OUT} = ±10V	-0.8		0.8	%
	Gain Nonlinearity	G = 1 - 100, V_{OUT} = -10V to 10V, R_L = 10kΩ		10	50	ppm
		G = 1 - 100, V_{OUT} = -10V to 10V, R_L = 2kΩ		10	95	ppm
	Gain vs. Temperature	G = 1		<10		ppm/°C
		G > 1		<-50		ppm/°C
	Reference Gain Error (1)	V_S = ±16.5V	-0.03		0.03	%
Voltage Offset						
V_{OSI}	Input Offset Voltage	V_S = ±4.5V to ±16.5V	-125		125	µV
	Average Temperature Coefficient	V_S = ±4.5V to ±16.5V		0.1		µV/°C
V_{OSO}	Output Offset Voltage	V_S = ±4.5V to ±16.5V, G = 1	-1500	200	1500	µV
	Average Temperature Coefficient	V_S = ±4.5V to ±16.5V		2.5		µV/°C
PSR	Offset Referred to the Input vs. Supply	G = 1, V_S = ±2.3V to ±18V	80	100		dB
		G = 10, V_S = ±2.3V to ±18V	95	120		dB
		G = 100, V_S = ±2.3V to ±18V	110	140		dB
		G = 1000, V_S = ±2.3V to ±18V	110	140		dB
Input Current						
I_B	Input Bias Current	V_S = ±16.5V	-2	0.5	2	nA
	Average Temperature Coefficient	V_S = ±16.5V		3		pA/°C
I_{OS}	Input Offset Current	V_S = ±16.5V	-1		1	nA
Input						
	Input Impedance	Differential		10, 2		GΩ, pF
		Common-Mode		10, 2		GΩ, pF
IVR	Input Voltage Range (2)	V_S = ±4.5V, G = 1	$-V_S$ + 1.9		$+V_S$ - 1.2	V
		V_S = ±16.5V, G = 1	$-V_S$ + 1.9		$+V_S$ - 1.4	V
CMRR	Common-Mode Rejection Ratio	G = 1, V_S = ±16.5V	70	90		dB
		G = 10, V_S = ±16.5V	90	110		dB
		G = 100, V_S = ±16.5V	108	130		dB
		G = 1000, V_S = ±16.5V	108	130		dB
Output						
V_{OUT}	Output Swing	V_S = ±2.3V to ±4.5V	$-V_S$ + 1.1		$+V_S$ - 1.2	V
		V_S = ±18V, G = 1	$-V_S$ + 1.4		$+V_S$ - 1.2	V
I_{SC}	Short Circuit Current			±20		mA
Dynamic Performance						
BW_{-3dB}	Small Signal -3dB Bandwidth	G = 1		700		kHz
		G = 10		400		kHz
		G = 100		100		kHz
		G = 1000		12		kHz
SR	Slew Rate	G = 10, V_S = ±15V	0.6	1.2		V/µs
t_S	Settling Time to 0.01%	5V step, G = 1 to 100		13		µs
		5V step, G = 1000		110		µs

Electrical Characteristics continued

T_A = 25°C, V_S = ±15V, R_L = 2kΩ to GND; unless otherwise noted. Gain = 1 + (49.4k/R_G); Total RTI Error = V_{OSI} + (V_{OSO}/G)

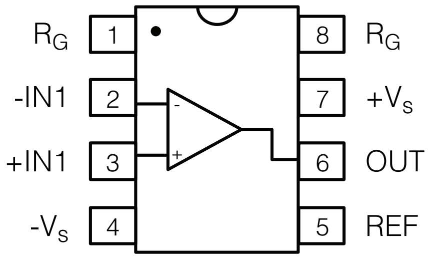
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Noise						
e_{ni}	Input Voltage Noise	1kHz, G = 1000, V_S = ±15V		6.6	13	nV/√Hz
e_{no}	Output Voltage Noise	1kHz, G = 1, V_S = ±15V		70	100	nV/√Hz
e_{npp}	Peak-to-Peak Noise (RTI)	G = 1, 0.1Hz to 10Hz		5		μV_{pp}
		G = 10, 0.1Hz to 10Hz, V_S = ±15V			0.8	μV_{pp}
		G = 100, 0.1Hz to 10Hz, V_S = ±15V		0.2	0.4	μV_{pp}
i_n	Current Noise	f = 1kHz		100		fA/√Hz
i_{npp}	Peak-to-Peak Current Noise	0.1Hz to 10Hz		10		pA_{pp}
Reference Input						
R_{IN}	Input Resistance			20		kΩ
I_{IN}	Input Current	V_S = ±16.5V		50	60	µA
	Voltage Range		$-V_S$ + 1.6		$+V_S$ - 1.6	V
	Gain to Output			1±0.0001		
Power Supply						
V_S	Operating Range		±2.3		±18	V
I_S	Supply Current	V_S = ±16.5V		1.3	2.2	mA

Notes:

1. Nominal reference voltage gain is 1.0
2. Input voltage range = CMV + (G V_{DIFF})/2

XR620A Pin Configurations

SOIC-8, DIP-8



XR620A Pin Assignments

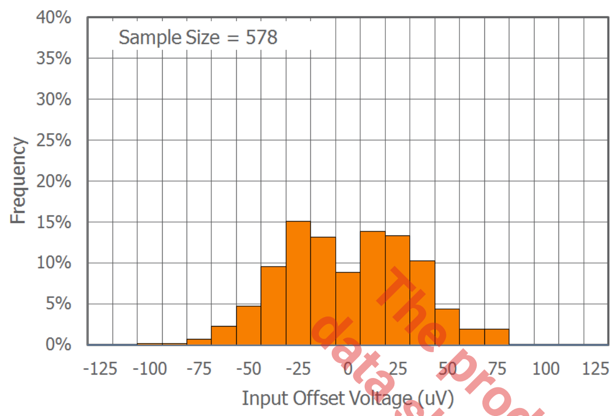
SOIC-8, DIP-8

Pin No.	Pin Name	Description
1, 8	R_G	R_G sets gain
2	-IN	Negative input
3	+IN	Positive input
4	$-V_S$	Negative supply
5	REF	Output is referred to the REF pin potential
6	OUT	Output
7	$+V_S$	Positive supply

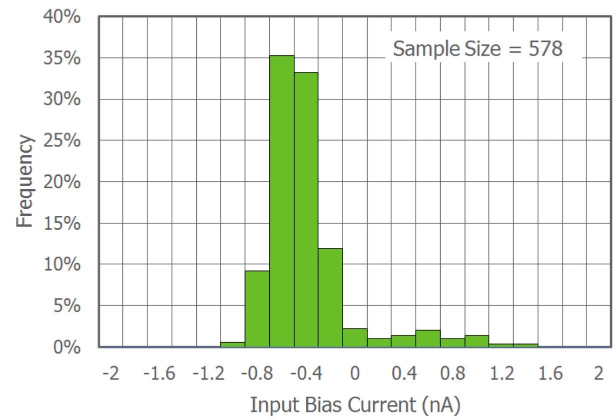
Typical Performance Characteristics

$T_A = 25°C$, $V_S = \pm15V$, $R_L = 2k\Omega$ to GND; unless otherwise noted.

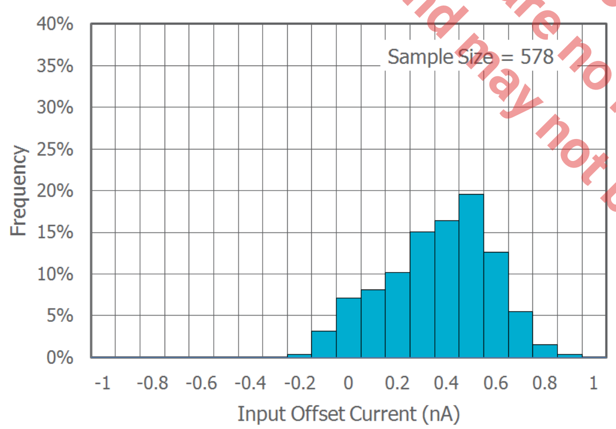
Input Offset Distribution (typical)



Input Bias Current Distribution (typical)



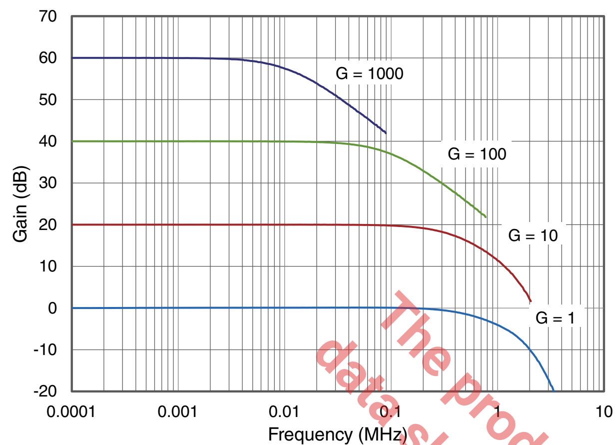
Input Offset Current Distribution (typical)



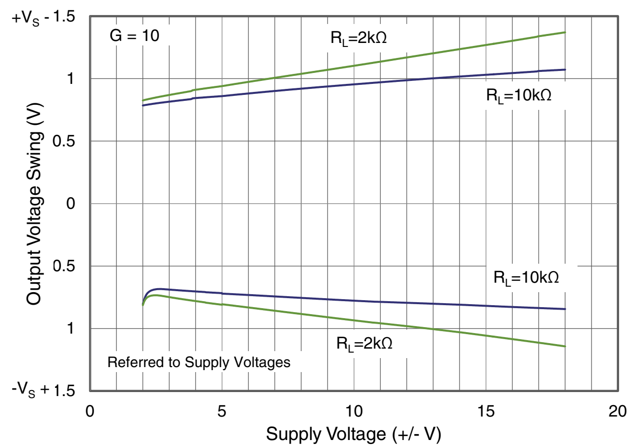
Typical Performance Characteristics

$T_A = 25°C$, $V_S = ±15V$, $R_L = 2kΩ$ to GND; unless otherwise noted.

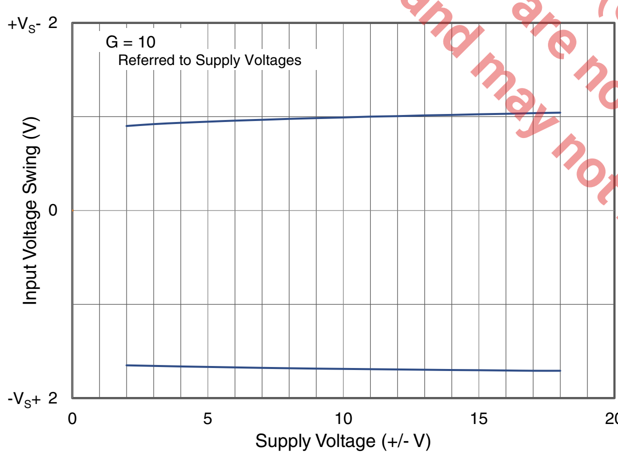
Gain vs. Frequency



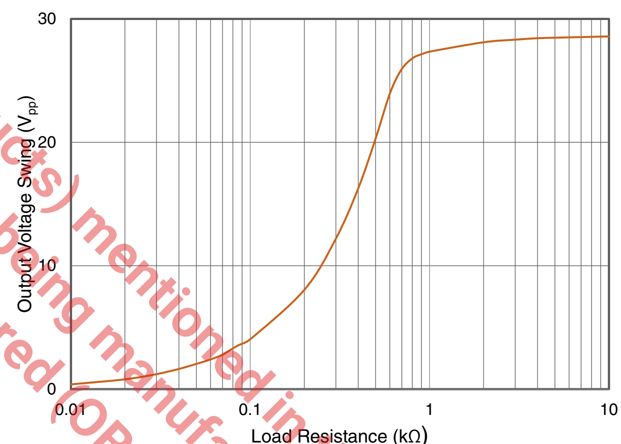
Output Voltage Swing vs. V_S



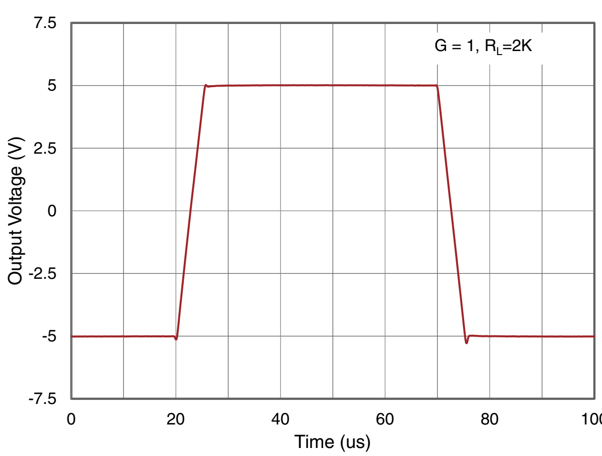
Input Voltage Range vs. V_S



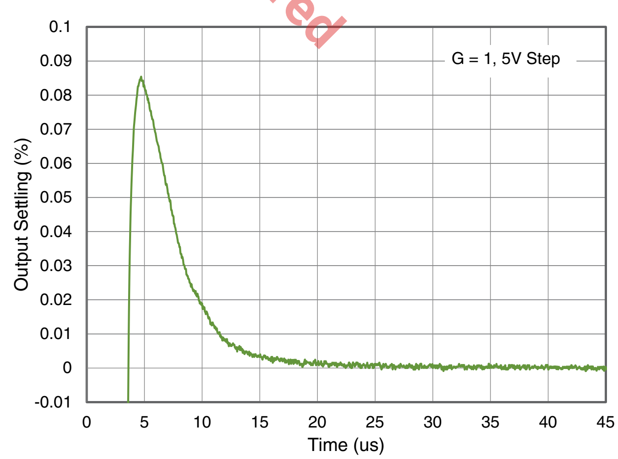
Output Voltage Swing vs. R_L



Large Signal Pulse Response (G = 1)



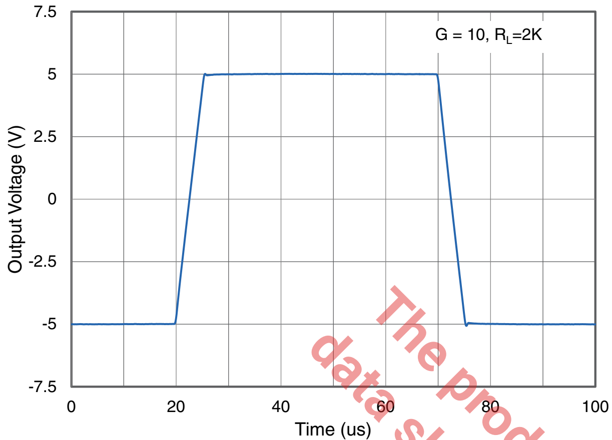
Large Signal Settling Time (G = 1)



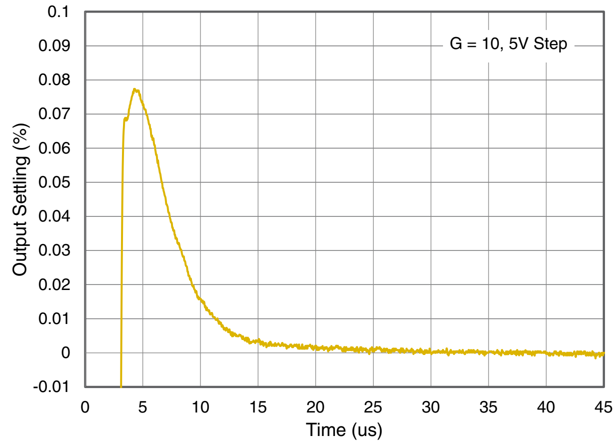
Typical Performance Characteristics

T_A = 25°C, V_S = ±15V, R_L = 2kΩ to GND; unless otherwise noted.

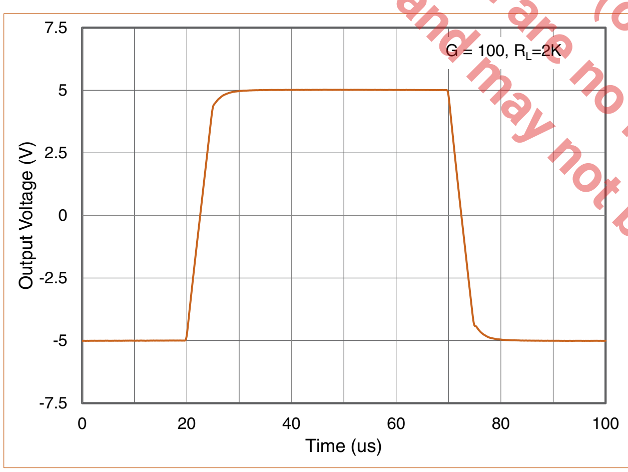
Large Signal Pulse Response (G = 10)



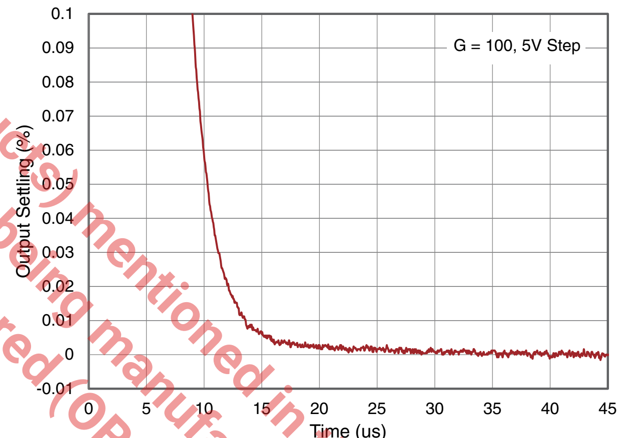
Large Signal Settling Time (G = 10)



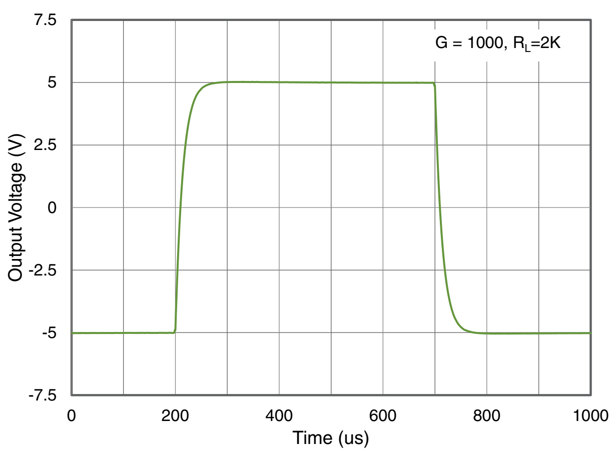
Large Signal Pulse Response (G = 100)



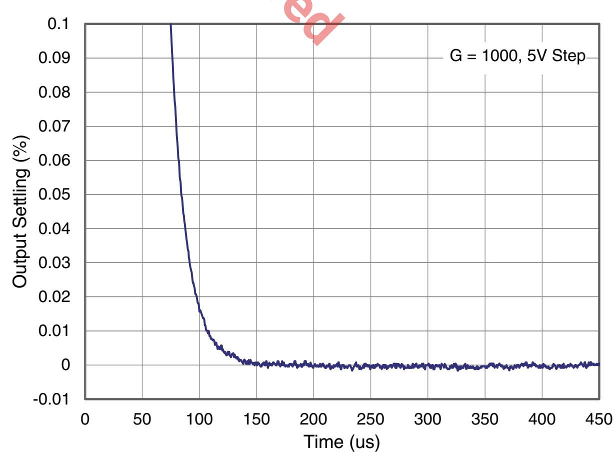
Large Signal Settling Time (G = 100)



Large Signal Pulse Response (G = 1000)



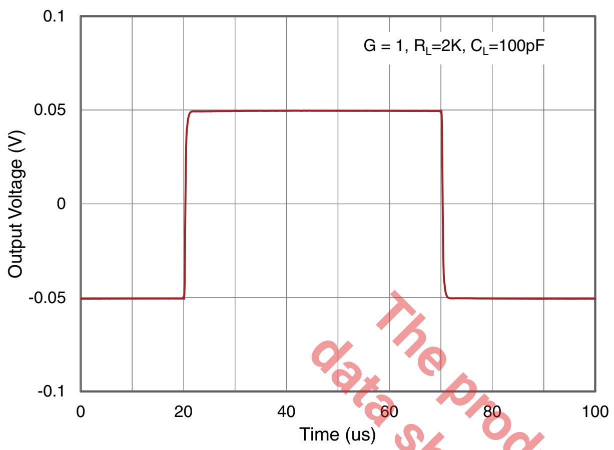
Large Signal Settling Time (G = 1000)



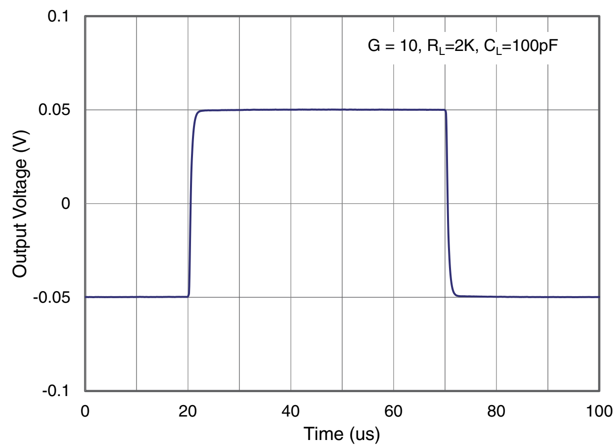
Typical Performance Characteristics

$T_A = 25°C$, $V_S = ±15V$, $R_L = 2kΩ$ to GND; unless otherwise noted.

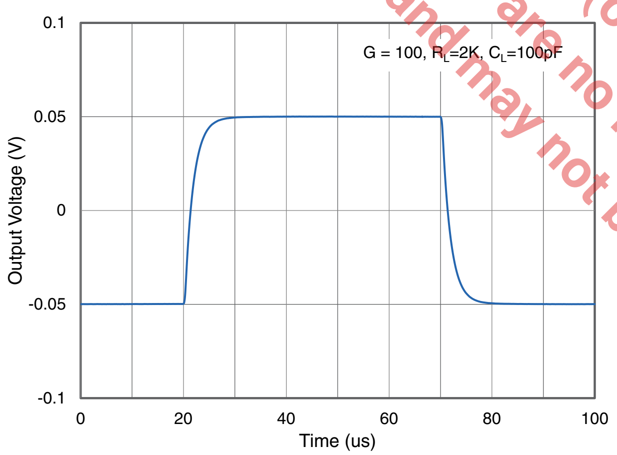
Small Signal Pulse Response (G = 1)



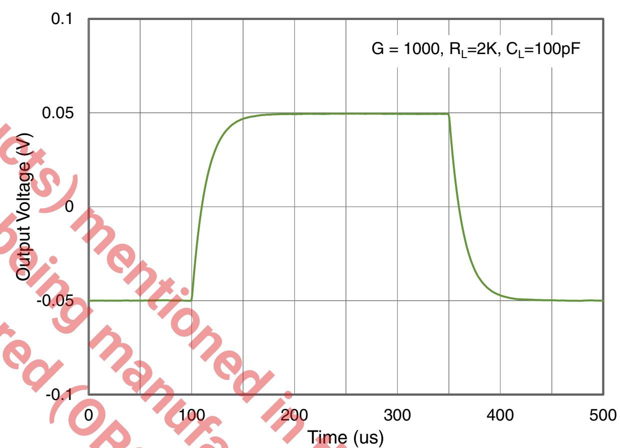
Small Signal Pulse Response (G = 10)



Small Signal Pulse Response (G = 100)



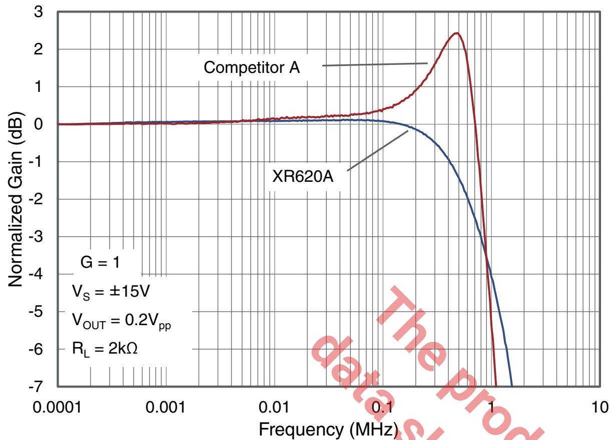
Small Signal Pulse Response (G = 1000)



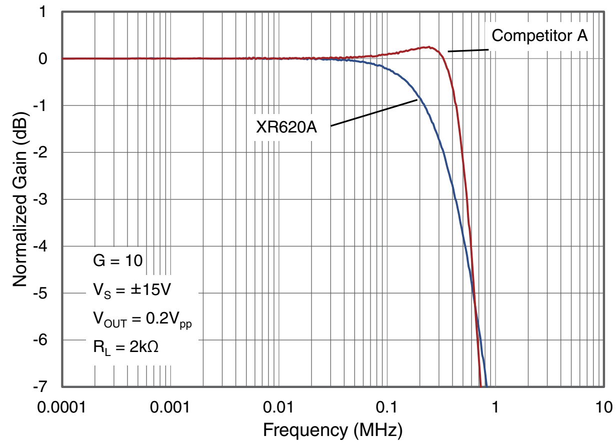
Typical Competitive Comparison Plots

$T_A = 25°C$, $V_S = \pm15V$, $R_L = 2k\Omega$, Exar evaluation board; unless otherwise noted.

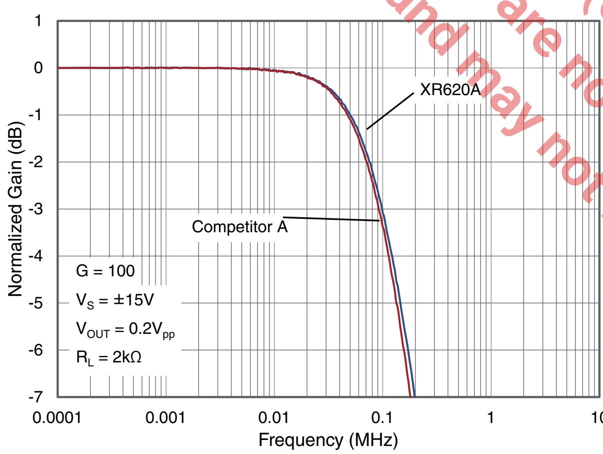
Frequency Response (G = 1)



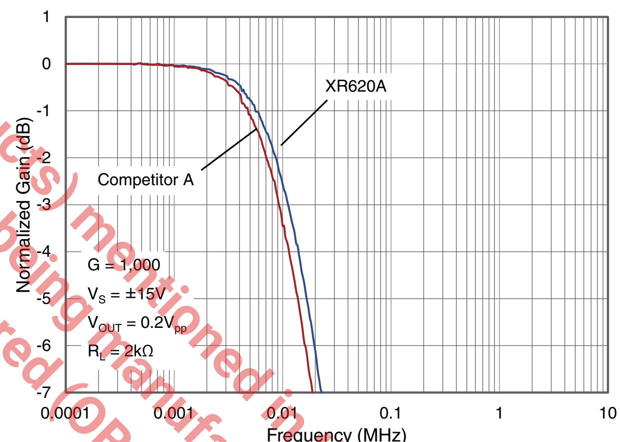
Frequency Response (G = 10)



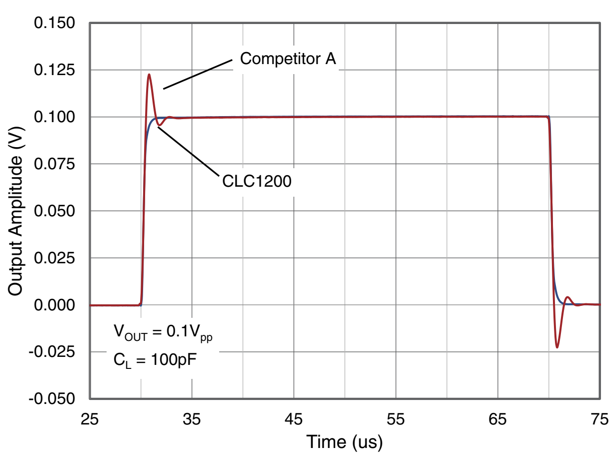
Frequency Response (G = 100)



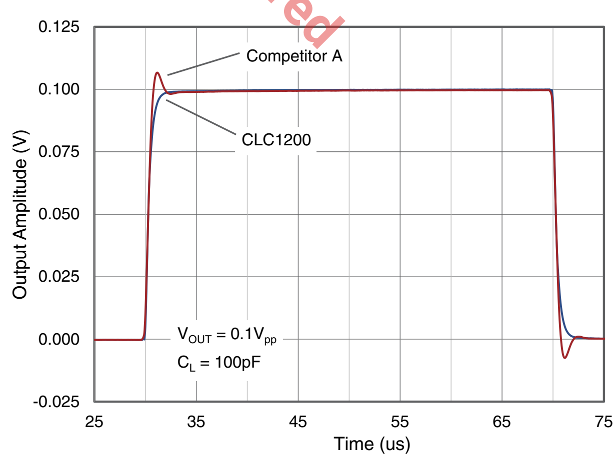
Frequency Response (G = 1000)



Small Signal Pulse Response (G = 1)



Small Signal Pulse Response (G = 10)



Application Information

Basic Information

The XR620A is a monolithic instrumentation amplifier based on the classic three op amp solution, refer to the Functional Block Diagram shown in Figure 1. The XR620A produces a single-ended output referred to the REF pin potential.

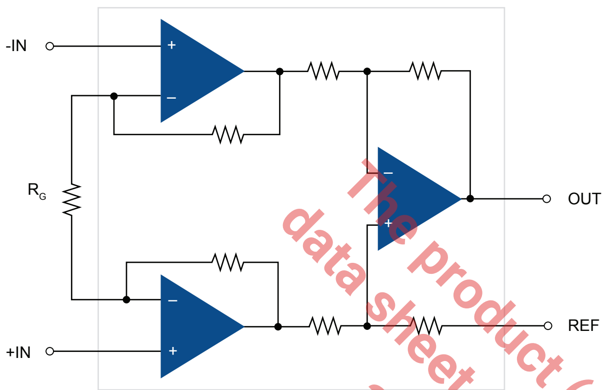


Figure 1: Functional Block Diagram

The internal resistors are trimmed which allows the gain to be accurately adjusted with one external resistor R_G.

$$G = \frac{49.4k}{R_G} + 1; \quad R_G = \frac{49.4k}{G - 1}$$

R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases to that of the input transistors. Producing the following advantages:

- Open-loop gain increases as the gain is increased, reducing gain related errors
- Gain-bandwidth increases as the gain is increased, optimizing frequency response
- Reduced input voltage noise which is determined by the collector current and base resistance of the input devices

Gain Selection

The impedance between pins 1 and 8, R_G, sets the gain of the XR620A. Table 1 shows the required standard table values of R_G for various calculated gains. For G = 1, $R_G = \infty$.

1% R_G (Ω)	Caclulated Gain	0.1% R_G (Ω)	Calculated Gain
49.9k	1.990	49.3k	2.002
12.4k	4.984	12.4k	4.984
5.49k	9.998	5.49k	9.998
2.61k	19.93	2.61k	19.93
1.00k	50.40	1.01k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003.0

Table 1: Recommended R_G Values

Follow these guidelines for improved performance:

- To maintain gain accuracy, use 0.1% to 1% resistors
- To minimize gain error, avoid high parasitic resistance in series with R_G
- To minimize gain drift, use low TC resistors (<10ppm/°C)

Common Mode Rejection

The XR620A offers high CMRR. To achieve optimal CMRR performance:

- Connect the reference terminal (pin 5) to a low impedance source
- Minimize capacitive and resistive differences between the inputs

In many applications, shielded cables are used to minimize noise. Properly drive the shield for best CMRR performance over frequency. Figures 1 and 2 show active data guards that are configured to improve AC common-mode rejections. the capacitances of input cable shields are “bootstrapped” to minimize the capacitance mismatch between the inputs.

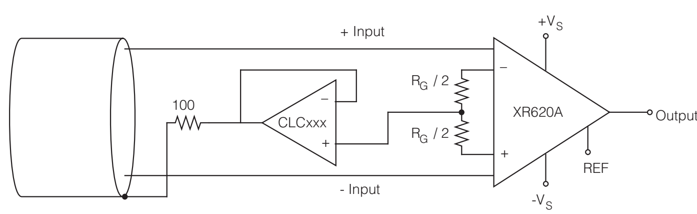


Figure 2: Common-mode Shield Driver

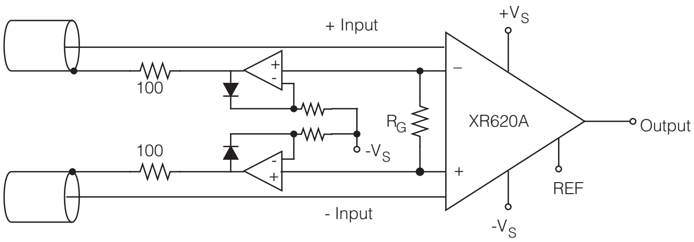


Figure 3: Differential Shield Driver

Pressure Measurement Applications

The XR620A is especially suitable for higher resistance pressure sensors powered at lower voltages where small size and low power become more significant.

Figure 3 shows a 3kΩ pressure transducer bridge powered from 5V. In such a circuit, the bridge consumes only 1.7mA. Adding the XR620A and a buffered voltage divider allows the signal to be conditioned for only 3.8mA of total supply current.

Small size and low cost make the XR620A especially attractive for voltage output pressure transducers. Since it delivers low noise and drift, it will also serve applications such as diagnostic noninvasive blood pressure measurement.

Medical ECG

The XR620A is perfect for ECG monitors because of its low current noise. A typical application is shown in Figure 4. The XR620A's low power, low supply voltage requirements, and space-saving 8-lead SOIC package offerings make it an excellent choice for battery-powered data recorders.

Furthermore, the low bias currents and low current noise, coupled with the low voltage noise of the XR620A, improve the dynamic range for better performance.

The value of capacitor C1 is chosen to maintain stability of the right leg drive loop. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

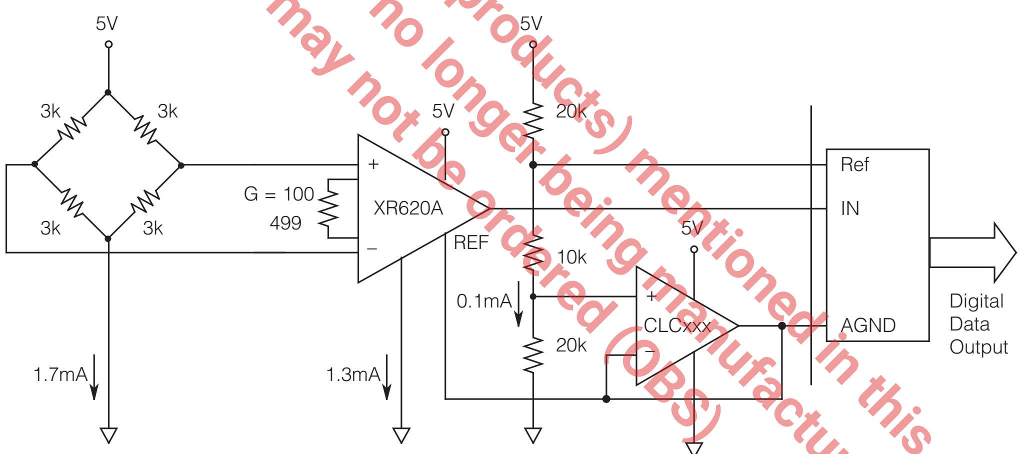


Figure 4: Pressure Monitoring Circuits Operating on a Single 5V Supply

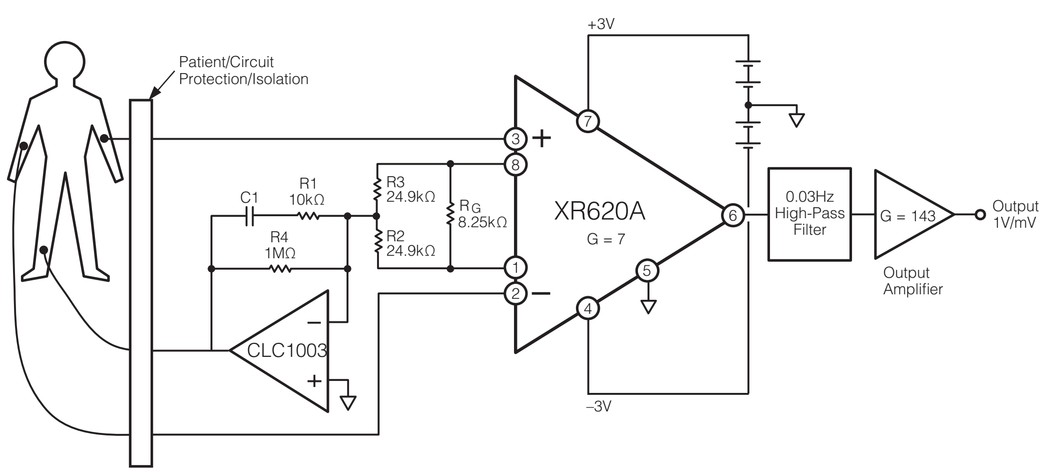


Figure 5: Typical Circuit for ECG Monitor Applications

Grounding

The output voltage of the XR620A is developed with respect to the potential on the reference terminal (pin 8). Simply tie the REF pin to the appropriate “local ground” to resolve many grounding problems.

To isolate low level analog signals from a noisy digital environment, many data acquisition components have separate analog and digital ground pins. Use separate ground lines (analog and digital) to minimize current flow from sensitive areas to system ground. These ground returns must be tied together at some point, usually best at the ADC.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Exar has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.1μF ceramic capacitors for power supply decoupling
- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board #	Products
CEB024	XR620A in SOIC-8

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 6-8. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short $-V_S$ to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

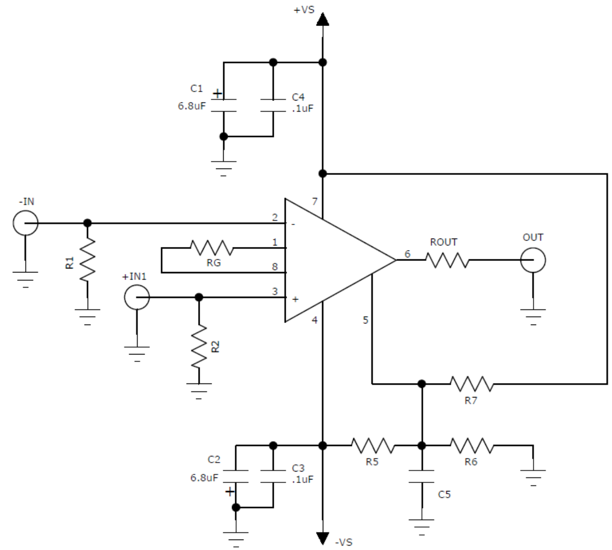


Figure 6. CEB024 Schematic

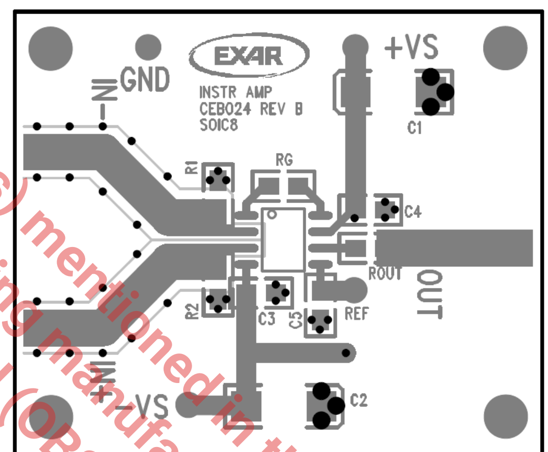


Figure 7. CEB024 Top View

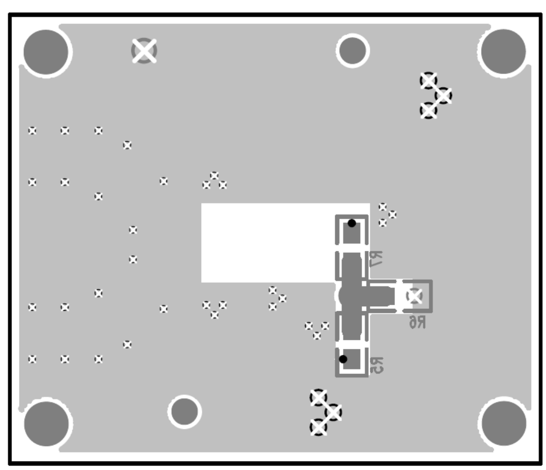
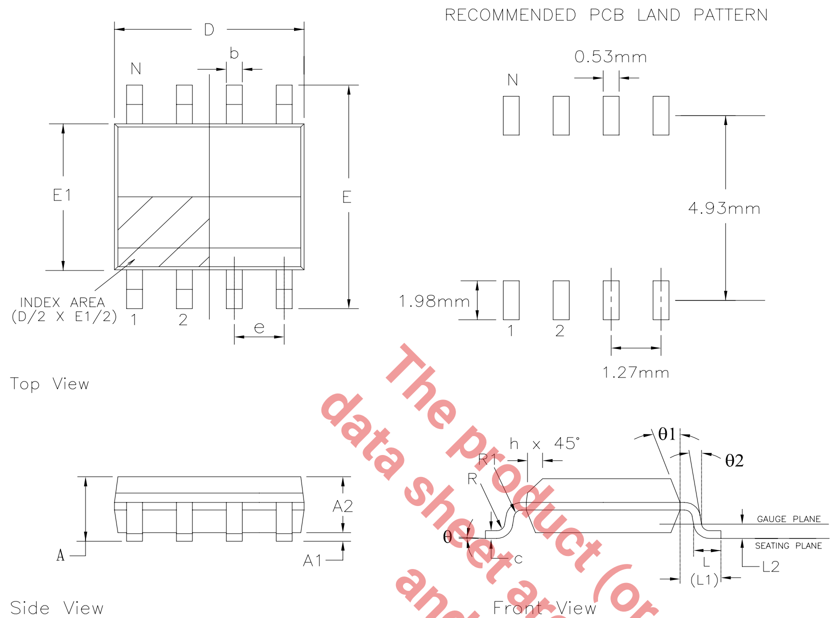


Figure 8. CEB024 Bottom View

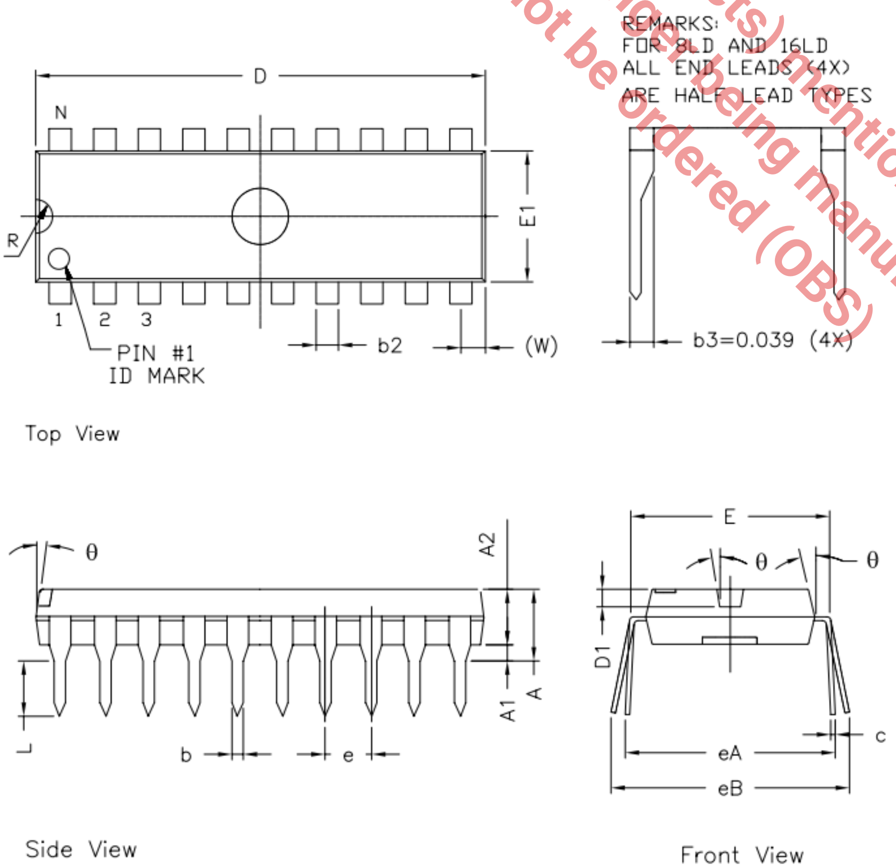
Mechanical Dimensions

SOIC-8 Package



8 Pin SOICN JEDEC MS-012 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8			8		

DIP-8 Package



8 Pin PDIP JEDEC MS-001 Variation BA						
SYMBOLS	DIMENSIONS IN INCH (Control Unit)			DIMENSIONS IN MM (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	0.210	—	—	5.33
A1	0.015	—	—	0.38	—	—
A2	0.115	0.130	0.195	2.92	3.30	4.95
b	0.014	0.018	0.022	0.36	0.46	0.56
b2	0.045	0.060	0.070	1.14	1.52	1.78
c	0.008	0.010	0.014	0.20	0.25	0.36
D1	0.030	—	0.060	0.76	—	1.52
E	0.300	0.310	0.325	7.62	7.87	8.26
E1	0.240	0.250	0.280	6.10	6.35	7.11
e	0.100 BSC			2.54 BSC		
eA	0.300 BSC			7.62 BSC		
eB	—	—	0.430	—	—	10.92
L	0.115	0.130	0.150	2.92	3.30	3.81
W	0.075 REF			1.91 REF		
R	0.030 BSC			0.76 BSC		
θ	4°	7°	10°	4°	7°	10°
D	0.355	0.365	0.400	9.02	9.27	10.16
N	8			8		

Ordering Information

Part Number	Package	Green	Operating Temperature Range	Packaging
XR620AISO8X	SOIC-8	Yes	-40°C to +85°C	Tape & Reel
XR620AISO8MTR	SOIC-8	Yes	-40°C to +85°C	Mini Tape & Reel
XR620AISO8EVB	Evaluation Board	N/A	N/A	N/A
XR620AIDP8	DIP-8	Yes	-40°C to +85°C	Rail

Moisture sensitivity level for all parts is MSL-1. Mini Tape and Reel contains 250 pieces.

Revision History

Revision	Date	Description
1B (ECN 1513-05)	March 2015	Reformat into Exar data sheet template. Updated PODs and thermal resistance numbers. Updated ordering information table to include MTR and EVB part numbers. Updated evaluation board top and bottom views to Rev b. Added schematic used for evaluation boards.

For Further Assistance:

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