



A New Direction in Mixed-Signal

CLC1007, CLC2007, CLC4007

Single, Dual, and Quad Low Cost, High Speed RRO Amplifiers

General Description

The CLC1007 (single), CLC2007 (dual) and CLC4007(quad) are low cost, voltage feedback amplifiers. These amplifiers are designed to operate on +3V to +5V, or ±5V supplies. The input voltage range extends 300mV below the negative rail and 0.9V below the positive rail.

The CLC1007, CLC2007, and CLC4007 offer superior dynamic performance with a 260MHz small signal bandwidth and 220V/μs slew rate. The combination of low power, high output current drive, and rail-to-rail performance make these amplifiers well suited for battery-powered communication/computing systems.

The combination of low cost and high performance make the CLC1007, CLC2007, and CLC4007 suitable for high volume applications in both consumer and industrial applications such as wireless phones, scanners, color copiers, and video transmission.

FEATURES

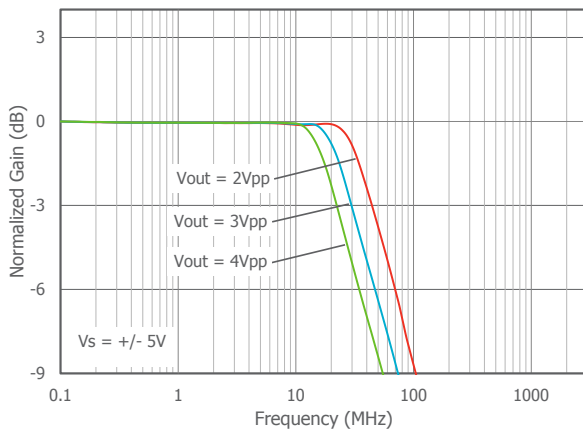
- 260MHz bandwidth
- Fully specified at +3V, +5V and ±5V supplies
- Output voltage range:
 - 0.03V to 4.95V; $V_S = +5$; $R_L = 2k\Omega$
- Input voltage range:
 - -0.3V to +4.1V; $V_S = +5$
- 220V/μs slew rate
- 2.6mA supply current per amplifier
- ±100mA linear output current
- ±125mA short circuit current
- CLC2007 directly replaces LMH6643, AD8042, AD8052, and AD8092
- CLC1007 directly replaces LMH6642, AD8041, AD8051, and AD8091

APPLICATIONS

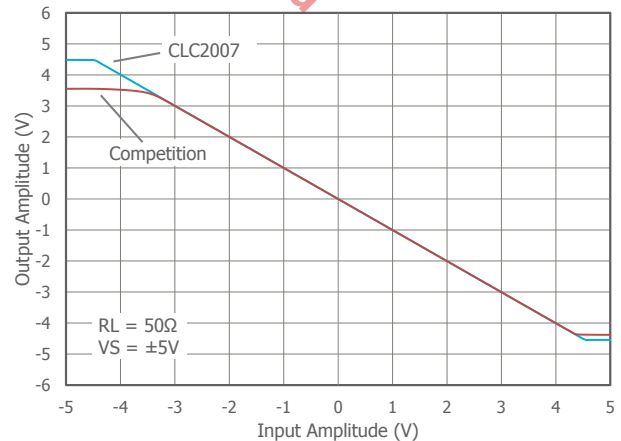
- A/D driver
- Active filters
- CCD imaging systems
- CD/DVD ROM
- Coaxial cable drivers
- High capacitive load driver
- Portable/battery-powered applications
- Twisted pair driver
- Telecom and optical terminals
- Video driver

Ordering Information - [page 26](#)

Large Signal Frequency Response



Output Voltage Swing vs Competition



Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

V_S 0V to +14V
 V_{IN} $-V_S - 0.5V$ to $+V_S + 0.5V$

Operating Conditions

Supply Voltage Range 2.7 to 12.6V
 Operating Temperature Range -40°C to 125°C
 Junction Temperature 150°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10s) 260°C

Package Thermal Resistance

θ_{JA} (TSOT23-5) 215°C/W
 θ_{JA} (SOIC-8) 150°C/W
 θ_{JA} (MSOP-8) 200°C/W
 θ_{JA} (SOIC-14) 90°C/W
 θ_{JA} (TSSOP-14) 100°C/W
 Package thermal resistance (θ_{JA}), JEDEC standard, multi-layer test boards, still air.

ESD Protection

TSOT-5 (HBM) 1kV
 SOIC-8 (HBM) 1kV
 TSOT-5 (CDM) 2kV
 SOIC-8 (CDM) 2kV
 ESD Rating for HBM (Human Body Model) and CDM (Charged Device Model).

The product (or product(s)) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Electrical Characteristics at +3V

$T_A = 25^\circ\text{C}$, $V_S = +3\text{V}$, $R_f = 1.5\text{k}\Omega$, $R_L = 2\text{k}\Omega$ to $V_S/2$; $G = 2$; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------|------------------------------|--|-----|--------------|-----|------------------------------|
| Frequency Domain Response | | | | | | |
| GBWP | -3dB Gain Bandwidth Product | $G = +11$, $V_{OUT} = 0.2V_{pp}$ | | 90 | | MHz |
| UGBW | Unity Gain Bandwidth | $V_{OUT} = 0.2V_{pp}$, $R_F = 0$ | | 245 | | MHz |
| BW _{SS} | -3dB Bandwidth | $V_{OUT} = 0.2V_{pp}$ | | 85 | | MHz |
| $f_{0.1dB}$ | 0.1dB Gain Flatness | $V_{OUT} = 0.2V_{pp}$, $R_L = 150\Omega$ | | 16 | | MHz |
| BW _{LS} | Large Signal Bandwidth | $V_{OUT} = 2V_{pp}$ | | 55 | | MHz |
| DG | Differential Gain | DC-coupled Output | | 0.03 | | % |
| | | AC-coupled Output | | 0.04 | | % |
| DP | Differential Phase | DC-coupled Output | | 0.03 | | ° |
| | | AC-coupled Output | | 0.06 | | ° |
| Time Domain | | | | | | |
| t_R , t_F | Rise and Fall Time | $V_{OUT} = 0.2\text{V}$ step; (10% to 90%) | | 5 | | ns |
| t_S | Settling Time to 0.1% | $V_{OUT} = 1\text{V}$ step | | 25 | | ns |
| OS | Overshoot | $V_{OUT} = 0.2\text{V}$ step | | 8 | | % |
| SR | Slew Rate | $G = -1$, 2V step | | 175 | | V/ μs |
| Distortion/Noise Response | | | | | | |
| THD | Total Harmonic Distortion | 1MHz, $V_{OUT} = 1V_{pp}$ | | 75 | | dBc |
| e_n | Input Voltage Noise | >50kHz | | 16 | | nV/ $\sqrt{\text{Hz}}$ |
| X _{TALK} | Crosstalk | f = 5MHz | | 58 | | dB |
| DC Performance | | | | | | |
| V_{IO} | Input Offset Voltage | | | 0.5 | | mV |
| d_{VIO} | Average Drift | | | 5 | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | | 1.4 | | μA |
| dI_B | Average Drift | | | 2 | | nA/ $^\circ\text{C}$ |
| I_{OS} | Input Offset Current | | | 0.05 | | μA |
| PSRR | Power Supply Rejection Ratio | DC | | 102 | | dB |
| A_{OL} | Open Loop Gain | $R_L = 2\text{k}\Omega$ | | 92 | | dB |
| I_S | Supply Current | per channel | | 2.6 | | mA |
| Input Characteristics | | | | | | |
| C_{IN} | Input Capacitance | | | 0.5 | | pF |
| CMIR | Common Mode Input Range | | | -0.3 to 2.1 | | V |
| CMRR | Common Mode Rejection Ratio | DC, $V_{CM} = 0$ to 1.5V | | 100 | | dB |
| Output Characteristics | | | | | | |
| V_{OUT} | Output Swing | $R_L = 150\Omega$ | | 0.3 to 2.75 | | V |
| | | $R_L = 2\text{k}\Omega$ | | 0.02 to 2.96 | | V |
| I_{OUT} | Output Current | | | ± 100 | | mA |
| I_{SC} | Short Circuit Current | $V_{OUT} = V_S / 2$ | | ± 125 | | V |
| V_S | Power Supply Operating Range | | | 2.7 to 12.6 | | V |

Electrical Characteristics at +5V

$T_A = 25^\circ\text{C}$, $V_S = +5\text{V}$, $R_f = 1.5\text{k}\Omega$, $R_L = 2\text{k}\Omega$ to $V_S/2$; $G = 2$; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------|------------------------------|---|-------|--------------|------|------------------------------|
| Frequency Domain Response | | | | | | |
| GBWP | -3dB Gain Bandwidth Product | $G = +11$, $V_{OUT} = 0.2V_{pp}$ | | 95 | | MHz |
| UGBW | Unity Gain Bandwidth | $V_{OUT} = 0.2V_{pp}$, $R_F = 0$ | | 250 | | MHz |
| BW _{SS} | -3dB Bandwidth | $V_{OUT} = 0.2V_{pp}$ | | 85 | | MHz |
| $f_{0.1dB}$ | 0.1dB Gain Flatness | $V_{OUT} = 0.2V_{pp}$, $R_L = 150\Omega$ | | 35 | | MHz |
| BW _{LS} | Large Signal Bandwidth | $V_{OUT} = 2V_{pp}$ | | 65 | | MHz |
| DG | Differential Gain | DC-coupled Output | | 0.03 | | % |
| | | AC-coupled Output | | 0.04 | | % |
| DP | Differential Phase | DC-coupled Output | | 0.03 | | ° |
| | | AC-coupled Output | | 0.06 | | ° |
| Time Domain | | | | | | |
| t_R , t_F | Rise and Fall Time | $V_{OUT} = 0.2\text{V}$ step | | 5 | | ns |
| t_S | Settling Time to 0.1% | $V_{OUT} = 2\text{V}$ step | | 25 | | ns |
| OS | Overshoot | $V_{OUT} = 0.2\text{V}$ step | | 5 | | % |
| SR | Slew Rate | $G = -1$, 4V step | | 220 | | V/ μs |
| Distortion/Noise Response | | | | | | |
| THD | Total Harmonic Distortion | 1MHz, $V_{OUT} = 2V_{pp}$ | | -75 | | dBc |
| e_n | Input Voltage Noise | >50kHz | | 16 | | nV/ $\sqrt{\text{Hz}}$ |
| X _{TALK} | Crosstalk | $f = 5\text{MHz}$ | | 58 | | dB |
| DC Performance | | | | | | |
| V_{IO} | Input Offset Voltage | | -7 | 0.5 | 7 | mV |
| d_{VIO} | Average Drift | | | 5 | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | -2 | 1.4 | 2 | μA |
| dI_B | Average Drift | | | 2 | | nA/ $^\circ\text{C}$ |
| I_{OS} | Input Offset Current | | -0.75 | 0.05 | 0.75 | μA |
| PSRR | Power Supply Rejection Ratio | DC | 80 | 102 | | dB |
| A_{OL} | Open Loop Gain | $R_L = 2\text{k}\Omega$ | 80 | 92 | | dB |
| I_S | Supply Current | per channel | | 2.6 | 4 | mA |
| Input Characteristics | | | | | | |
| C_{IN} | Input Capacitance | | | 0.5 | | pF |
| CMIR | Common Mode Input Range | | | -0.3 to 4.1 | | V |
| CMRR | Common Mode Rejection Ratio | DC, $V_{CM} = 0$ to 3.5V | 75 | 100 | | dB |
| Output Characteristics | | | | | | |
| V_{OUT} | Output Swing | $R_L = 150\Omega$ | 0.35 | 0.1 to 4.9 | 4.65 | V |
| | | $R_L = 2\text{k}\Omega$ | | 0.03 to 4.95 | | V |
| I_{OUT} | Output Current | | | ± 100 | | mA |
| I_{SC} | Short Circuit Current | $V_{OUT} = V_S / 2$ | | ± 125 | | V |
| V_S | Power Supply Operating Range | | | 2.7 to 12.6 | | V |

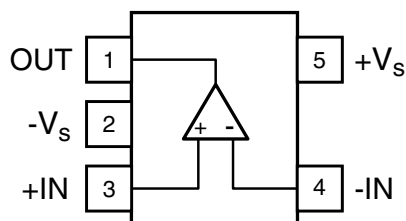
Electrical Characteristics at $\pm 5V$

$T_A = 25^\circ C$, $V_S = \pm 5V$, $R_f = 1.5k\Omega$, $R_L = 2k\Omega$ to GND; $G = 2$; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------|------------------------------|---|-----|---------------|-----|------------------|
| Frequency Domain Response | | | | | | |
| GBWP | -3dB Gain Bandwidth Product | $G = +11$, $V_{OUT} = 0.2V_{pp}$ | | 90 | | MHz |
| UGBW | Unity Gain Bandwidth | $V_{OUT} = 0.2V_{pp}$, $R_F = 0$ | | 260 | | MHz |
| BW _{SS} | -3dB Bandwidth | $V_{OUT} = 0.2V_{pp}$ | | 85 | | MHz |
| $f_{0.1dB}$ | 0.1dB Gain Flatness | $V_{OUT} = 0.2V_{pp}$, $R_L = 150\Omega$ | | 22 | | MHz |
| BW _{LS} | Large Signal Bandwidth | $V_{OUT} = 2V_{pp}$ | | 65 | | MHz |
| DG | Differential Gain | DC-coupled Output | | 0.03 | | % |
| | | AC-coupled Output | | 0.04 | | % |
| DP | Differential Phase | DC-coupled Output | | 0.03 | | ° |
| | | AC-coupled Output | | 0.06 | | ° |
| Time Domain | | | | | | |
| t_R , t_F | Rise and Fall Time | $V_{OUT} = 0.2V$ step | | 5 | | ns |
| t_S | Settling Time to 0.1% | $V_{OUT} = 2V$ step, $R_L = 100\Omega$ | | 25 | | ns |
| OS | Overshoot | $V_{OUT} = 0.2V$ step | | 5 | | % |
| SR | Slew Rate | $G = -1$, $5V$ step | | 225 | | V/ μs |
| Distortion/Noise Response | | | | | | |
| THD | Total Harmonic Distortion | 1MHz, $V_{OUT} = 2V_{pp}$ | | 76 | | dBc |
| e_n | Input Voltage Noise | >50kHz | | 16 | | nV/ \sqrt{Hz} |
| X _{TALK} | Crosstalk | $f = 5MHz$ | | 58 | | dB |
| DC Performance | | | | | | |
| V_{IO} | Input Offset Voltage | | | 0.5 | | mV |
| d_{VIO} | Average Drift | | | 5 | | $\mu V/^\circ C$ |
| I_B | Input Bias Current | | | 1.3 | | μA |
| dI_B | Average Drift | | | 2 | | nA/ $^\circ C$ |
| I_{OS} | Input Offset Current | | | 0.04 | | μA |
| PSRR | Power Supply Rejection Ratio | DC | | 102 | | dB |
| A_{OL} | Open Loop Gain | $R_L = 2k\Omega$ | | 92 | | dB |
| I_S | Supply Current | per channel | | 2.6 | | mA |
| Input Characteristics | | | | | | |
| C_{IN} | Input Capacitance | | | 0.5 | | pF |
| CMIR | Common Mode Input Range | | | -5.3 to 4.1 | | V |
| CMRR | Common Mode Rejection Ratio | DC, $V_{CM} = -5$ to $3.5V$ | | 100 | | dB |
| Output Characteristics | | | | | | |
| V_{OUT} | Output Swing | $R_L = 150\Omega$ | | -4.8 to 4.8 | | V |
| | | $R_L = 2k\Omega$ | | -4.95 to 4.93 | | V |
| I_{OUT} | Output Current | | | ± 100 | | mA |
| I_{SC} | Short Circuit Current | $V_{OUT} = V_S / 2$ | | ± 125 | | V |
| V_S | Power Supply Operating Range | | | 2.7 to 12.6 | | V |

CLC1007 Pin Configurations

TSOT-5

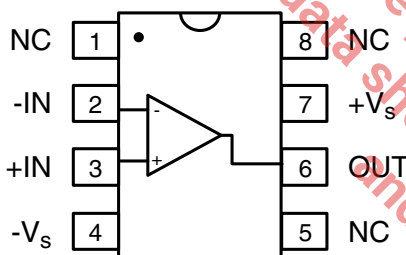


CLC1007 Pin Assignments

TSOT-5

| Pin No. | Pin Name | Description |
|---------|----------|-----------------|
| 1 | OUT | Output |
| 2 | -Vs | Negative supply |
| 3 | +IN | Positive input |
| 4 | -IN | Negative input |
| 5 | +Vs | Positive supply |

SOIC-8

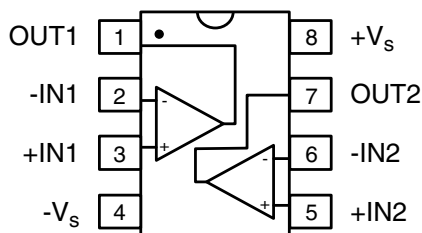


SOIC-8

| Pin No. | Pin Name | Description |
|---------|----------|-----------------|
| 1 | NC | No Connect |
| 2 | -IN | Negative input |
| 3 | +IN | Positive input |
| 4 | -Vs | Negative supply |
| 5 | NC | No Connect |
| 6 | OUT | Output |
| 7 | +Vs | Positive supply |
| 8 | NC | No Connect |

CLC2007 Pin Configuration

SOIC-8 / MSOP-8



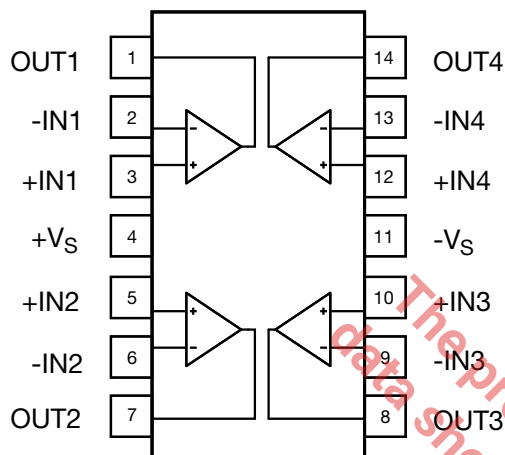
CLC2007 Pin Assignments

SOIC-8 / MSOP-8

| Pin No. | Pin Name | Description |
|---------|----------|---------------------------|
| 1 | OUT1 | Output, channel 1 |
| 2 | -IN1 | Negative input, channel 1 |
| 3 | +IN1 | Positive input, channel 1 |
| 4 | -Vs | Negative supply |
| 5 | +IN2 | Positive input, channel 2 |
| 6 | -IN2 | Negative input, channel 2 |
| 7 | OUT2 | Output, channel 2 |
| 8 | +Vs | Positive supply |

CLC4007 Pin Configuration

SOIC-14 / TSSOP-14



CLC4007 Pin Assignments

SOIC-14 / TSSOP-14

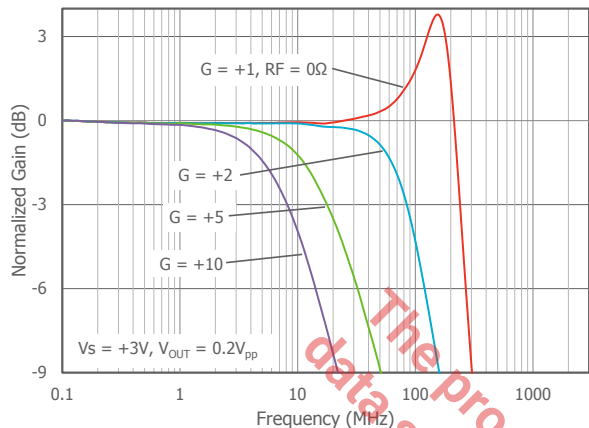
| Pin No. | Pin Name | Description |
|---------|-----------------|---------------------------|
| 1 | OUT1 | Output, channel 1 |
| 2 | -IN1 | Negative input, channel 1 |
| 3 | +IN1 | Positive input, channel 1 |
| 4 | +V _S | Positive supply |
| 5 | +IN2 | Positive input, channel 2 |
| 6 | -IN2 | Negative input, channel 2 |
| 7 | OUT2 | Output, channel 2 |
| 8 | OUT3 | Output, channel 3 |
| 9 | -IN3 | Negative input, channel 3 |
| 10 | +IN3 | Positive input, channel 3 |
| 11 | -V _S | Negative supply |
| 12 | +IN4 | Positive input, channel 4 |
| 13 | -IN4 | Negative input, channel 4 |
| 14 | OUT4 | Output, channel 4 |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

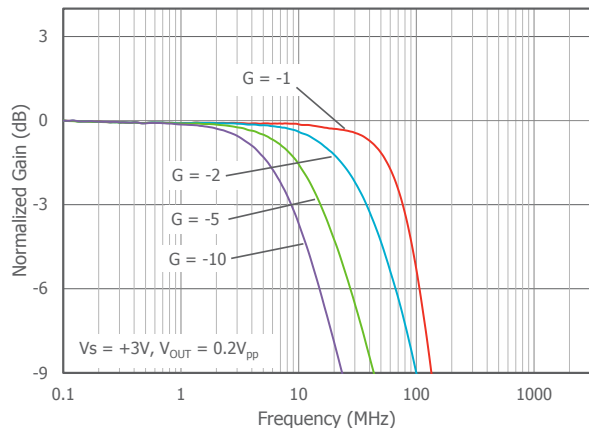
Typical Performance Characteristics at +3V

$T_A = 25^\circ\text{C}$, $V_S = +3\text{V}$, $R_L = 2\text{k}\Omega$ to $V_S/2$, $G = +2$, $R_F = 1.5\text{k}\Omega$; unless otherwise noted.

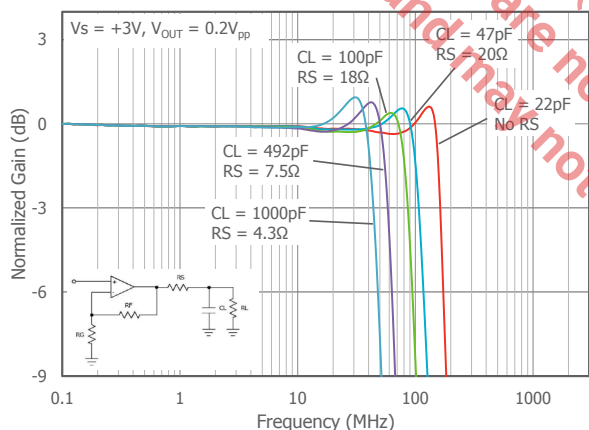
Non-Inverting Frequency Response



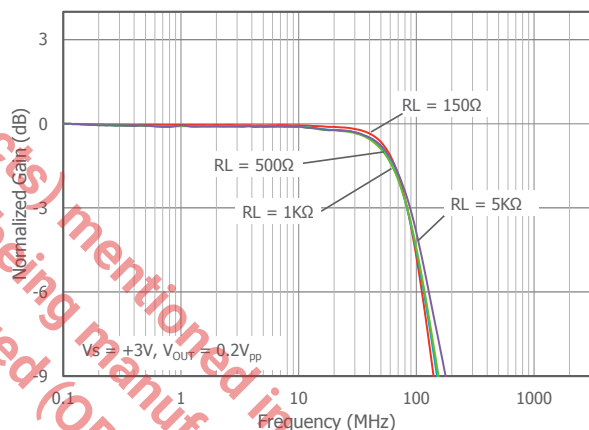
Inverting Frequency Response



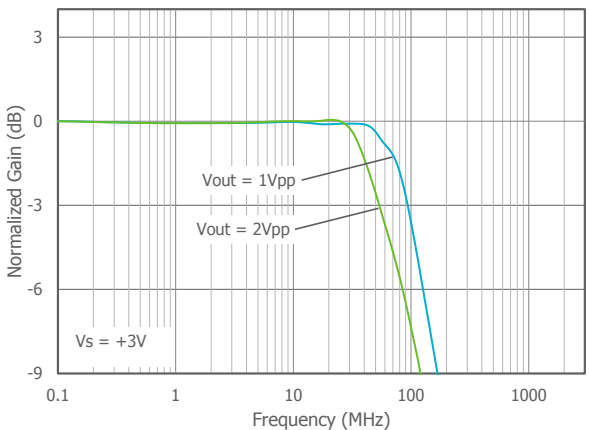
Frequency Response vs C_L



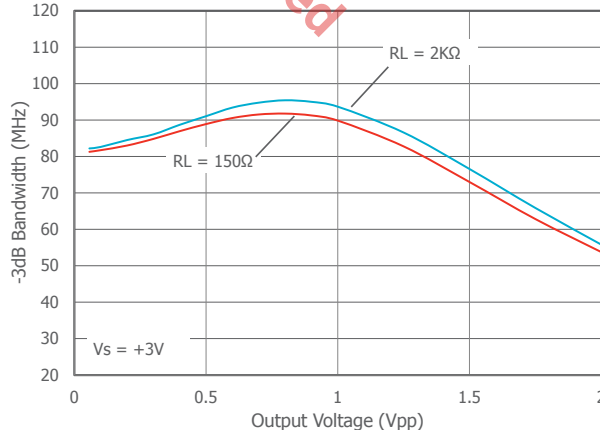
Frequency Response vs R_L



Large Signal Frequency Response



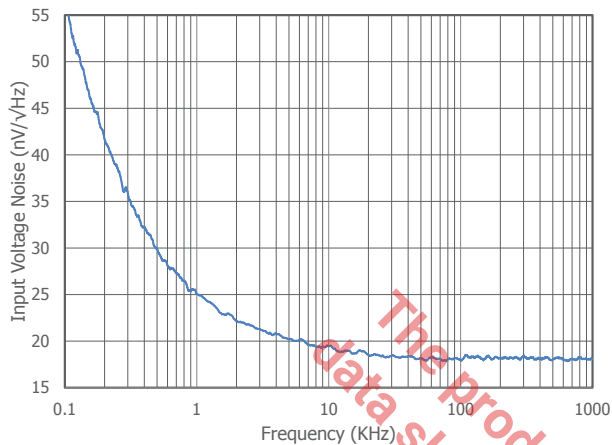
-3dB BW vs Output Voltage



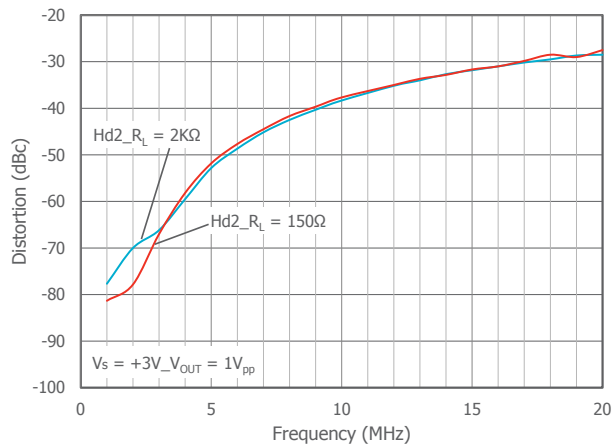
Typical Performance Characteristics at +3V

$T_A = 25^\circ\text{C}$, $V_S = +3\text{V}$, $R_L = 2\text{k}\Omega$ to $V_S/2$, $G = +2$, $R_F = 1.5\text{k}\Omega$; unless otherwise noted.

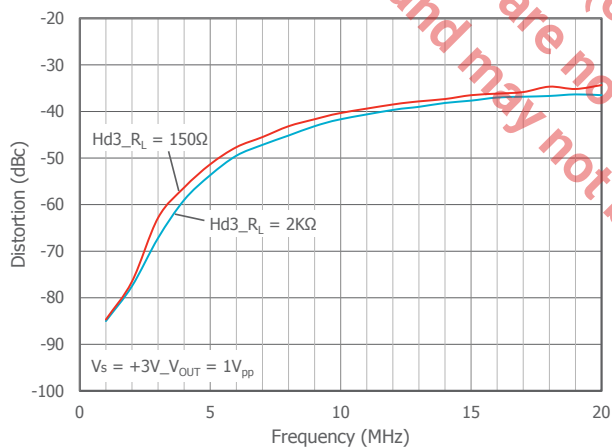
Input Voltage Noise vs Frequency



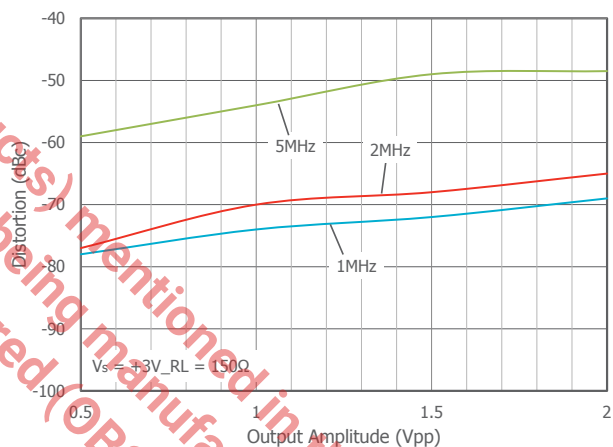
2nd Harmonic Distortion vs R_L over Frequency



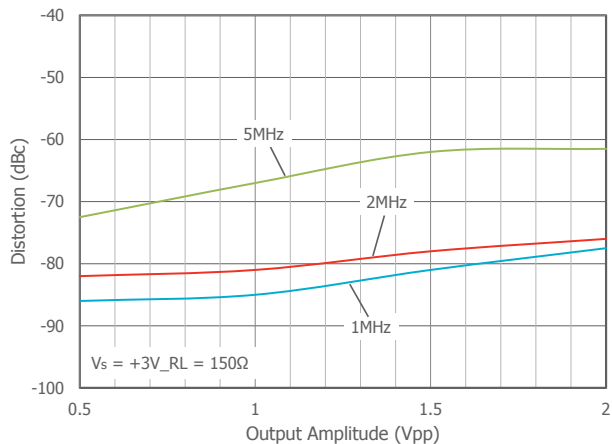
3rd Harmonic Distortion vs R_L over Frequency



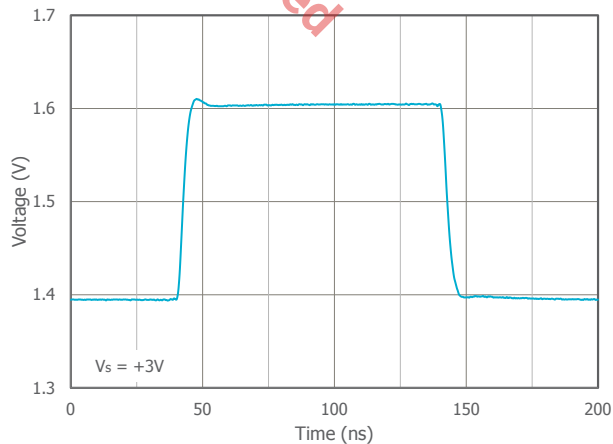
2nd Harmonic Distortion vs V_O over Frequency



3rd Harmonic Distortion vs V_O over Frequency



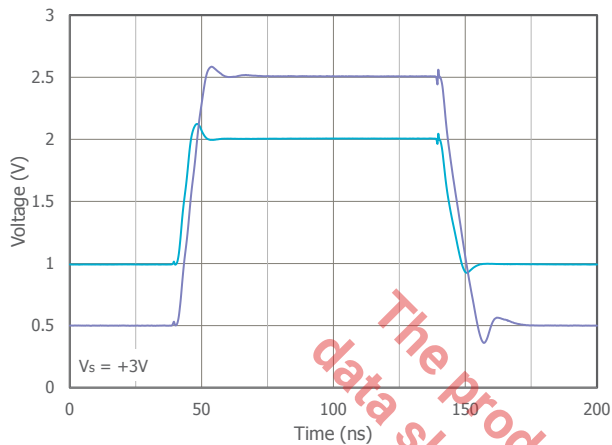
Non-Inverting Small Signal Pulse Response



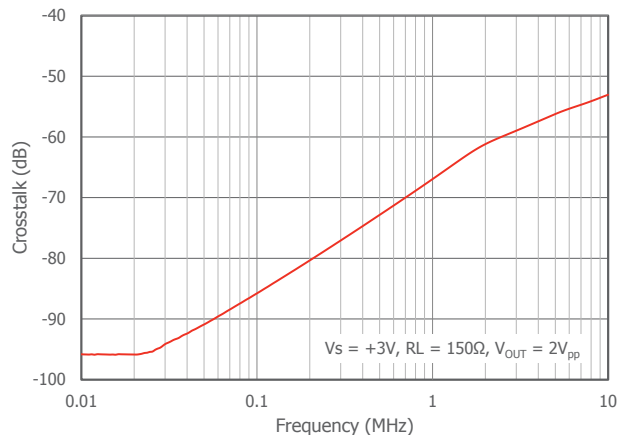
Typical Performance Characteristics at +3V

$T_A = 25^\circ\text{C}$, $V_S = +3\text{V}$, $R_L = 2\text{k}\Omega$ to $V_S/2$, $G = +2$, $R_F = 1.5\text{k}\Omega$; unless otherwise noted.

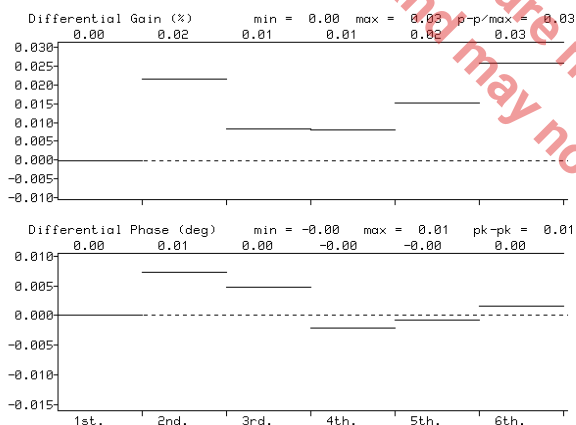
Non-Inverting Large Signal Pulse Response



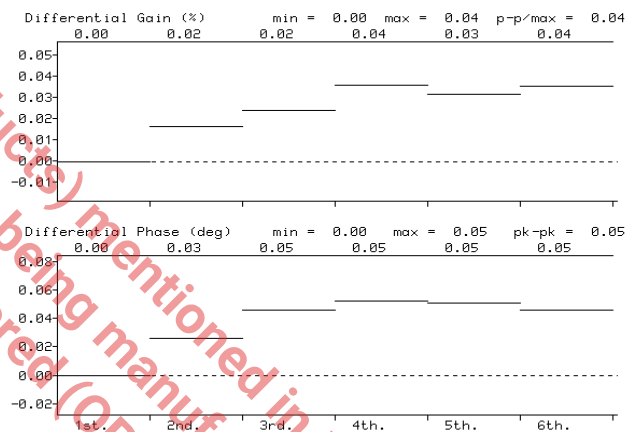
Crosstalk vs Frequency (CLC2007)



Differential Gain & Phase_DC Coupled



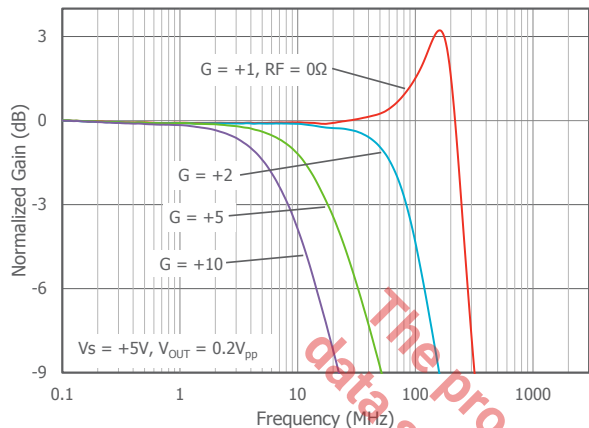
Differential Gain & Phase_AC Coupled



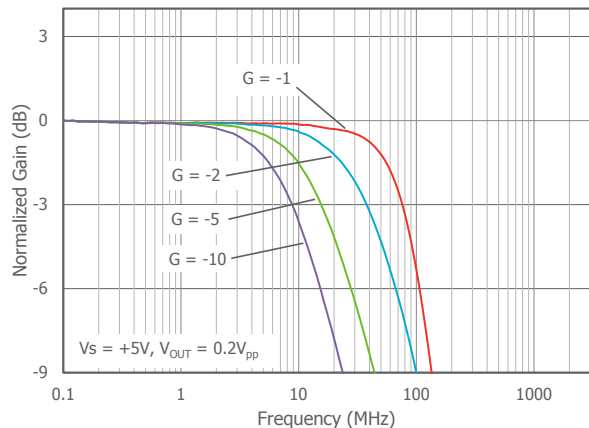
Typical Performance Characteristics at +5V

$T_A = 25^\circ\text{C}$, $V_S = +5\text{V}$, $R_L = 2\text{k}\Omega$ to $V_S/2$, $G = +2$, $R_F = 1.5\text{k}\Omega$; unless otherwise noted.

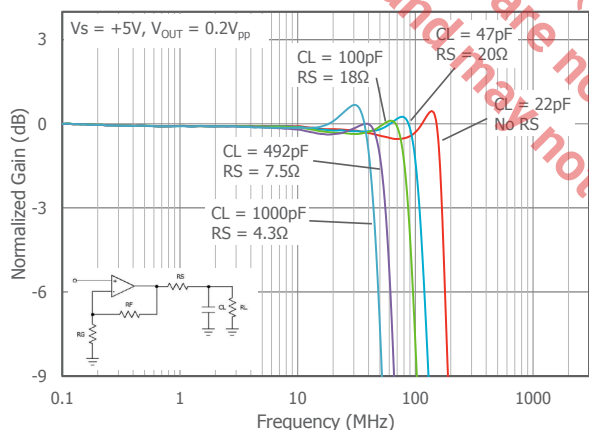
Non-Inverting Frequency Response



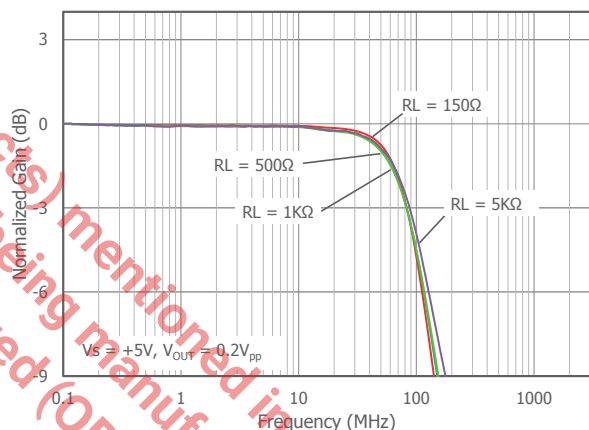
Inverting Frequency Response



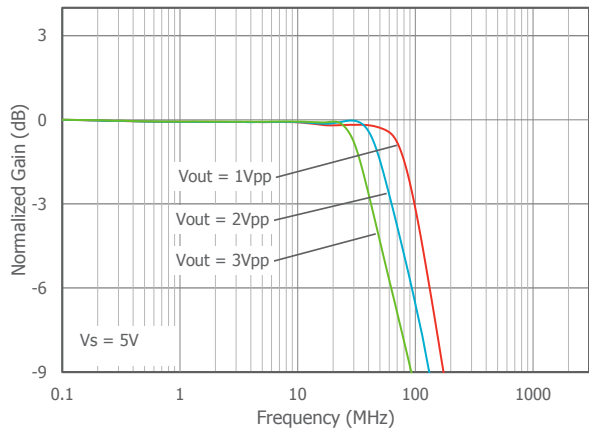
Frequency Response vs C_L



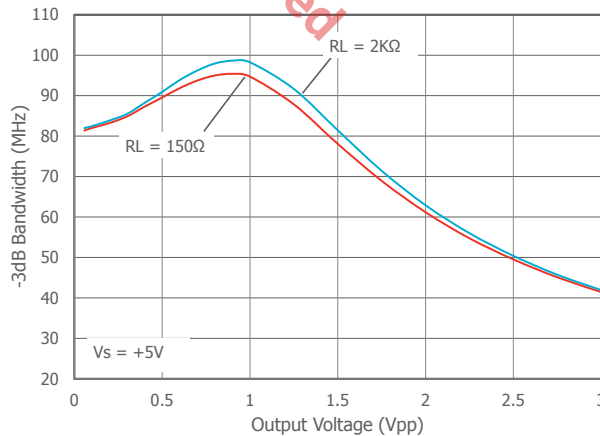
Frequency Response vs R_L



Large Signal Frequency Response



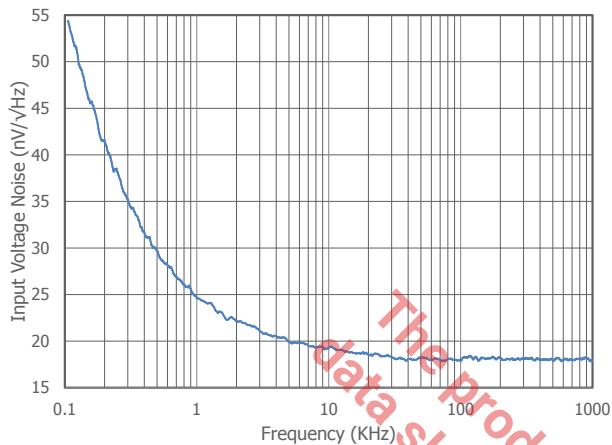
-3dB BW vs Output Voltage



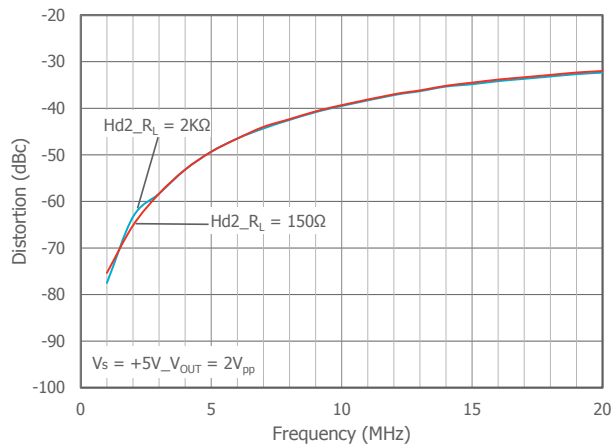
Typical Performance Characteristics at +5V

$T_A = 25^\circ\text{C}$, $V_S = +5\text{V}$, $R_L = 2\text{k}\Omega$ to $V_S/2$, $G = +2$, $R_F = 1.5\text{k}\Omega$; unless otherwise noted.

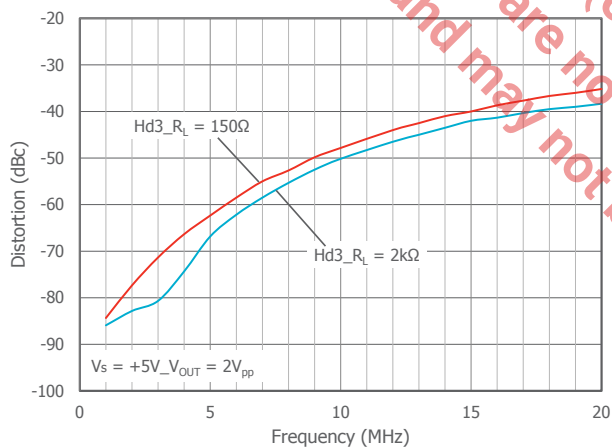
Input Voltage Noise vs Frequency



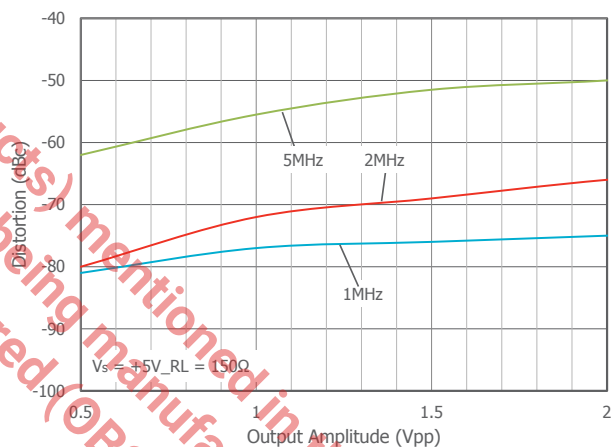
2nd Harmonic Distortion vs R_L over Frequency



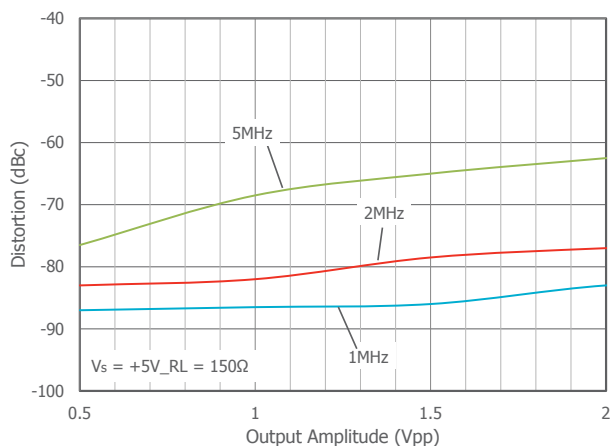
3rd Harmonic Distortion vs R_L over Frequency



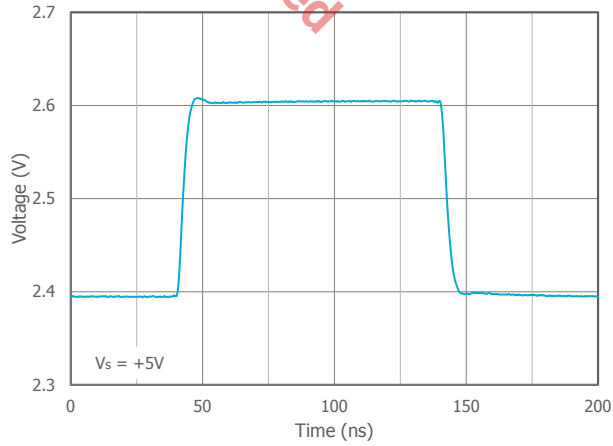
2nd Harmonic Distortion vs V_O over Frequency



3rd Harmonic Distortion vs V_O over Frequency



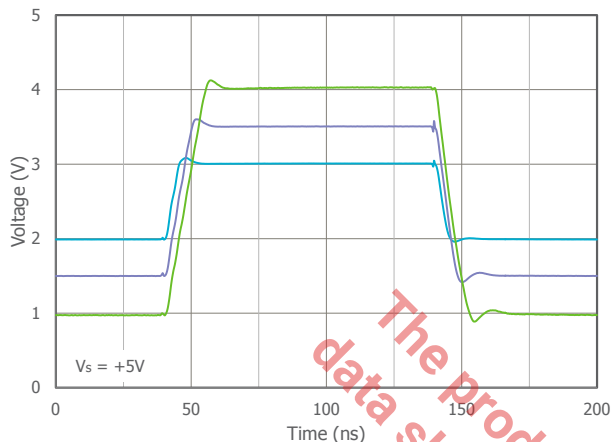
Non-Inverting Small Signal Pulse Response



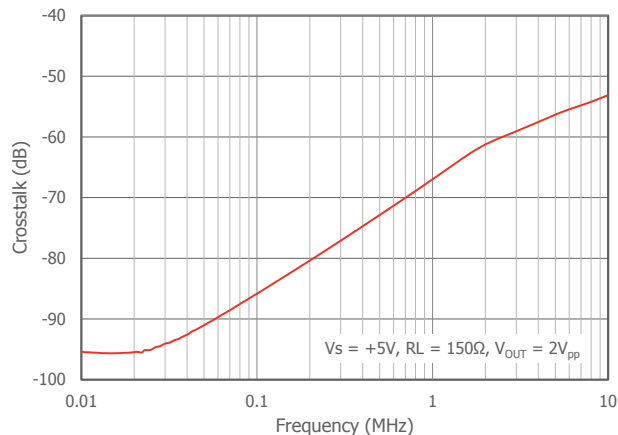
Typical Performance Characteristics at +5V

$T_A = 25^\circ\text{C}$, $V_S = +5\text{V}$, $R_L = 2\text{k}\Omega$ to $V_S/2$, $G = +2$, $R_F = 1.5\text{k}\Omega$; unless otherwise noted.

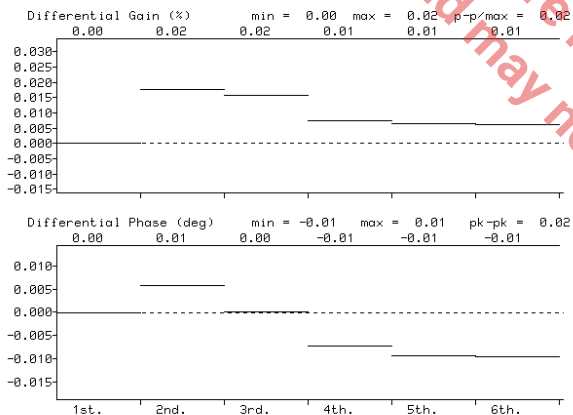
Non-Inverting Large Signal Pulse Response



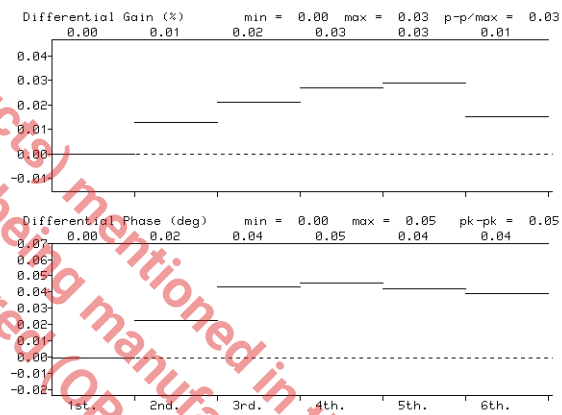
Crosstalk vs Frequency (CLC2007)



Differential Gain & Phase_DC Coupled



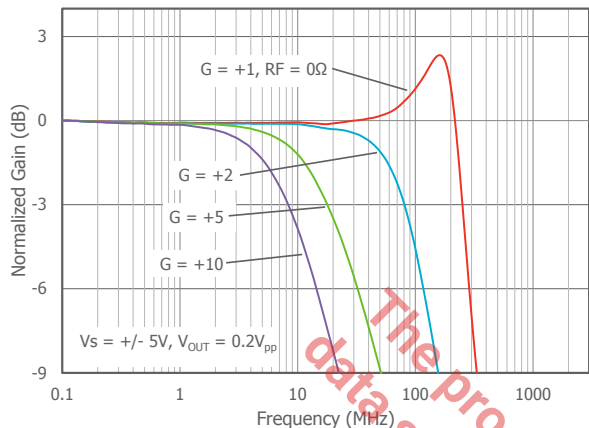
Differential Gain & Phase_AC Coupled



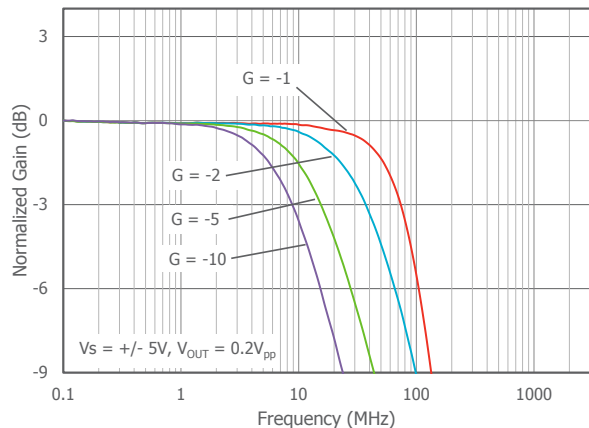
Typical Performance Characteristics at ±5V

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 2\text{k}\Omega$ to GND, $G = +2$, $R_F = 1.5\text{k}\Omega$; unless otherwise noted.

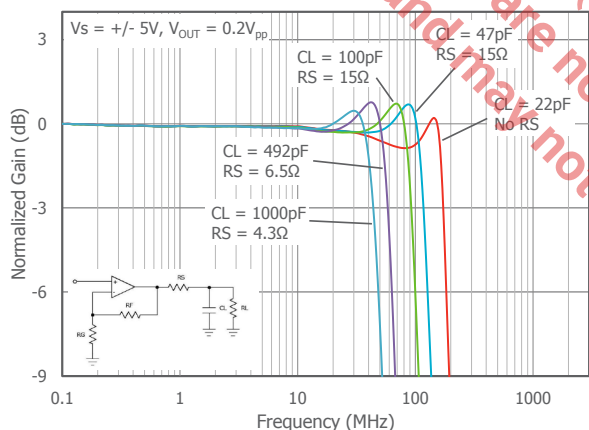
Non-Inverting Frequency Response



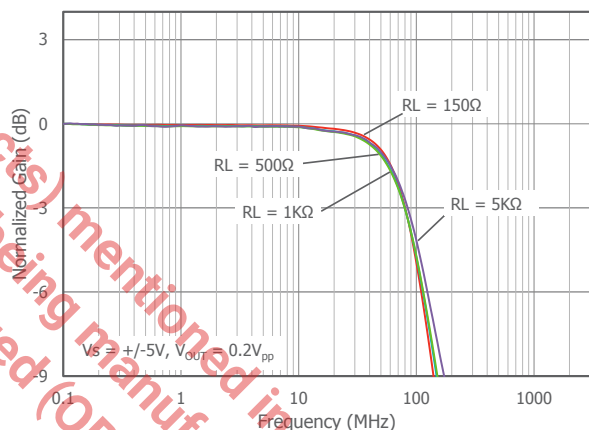
Inverting Frequency Response



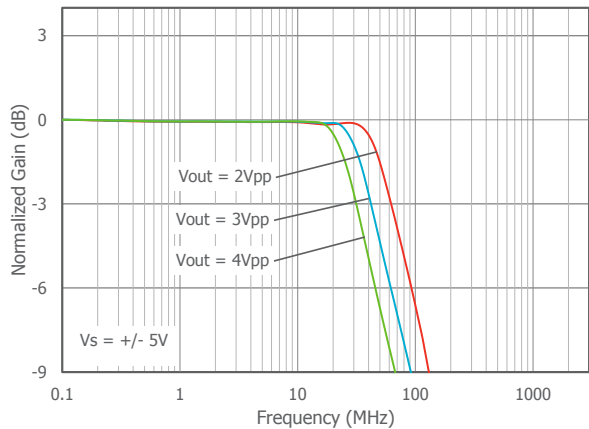
Frequency Response vs C_L



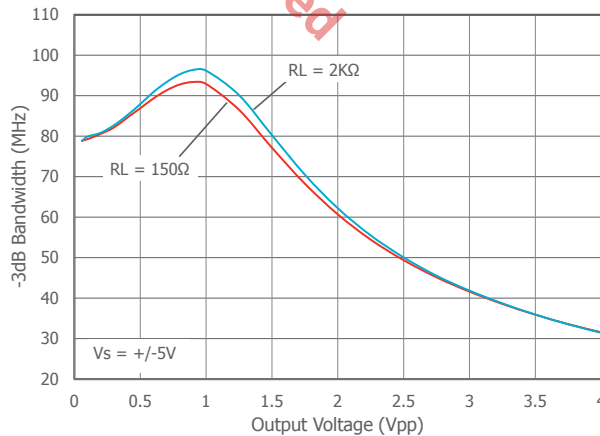
Frequency Response vs R_L



Large Signal Frequency Response



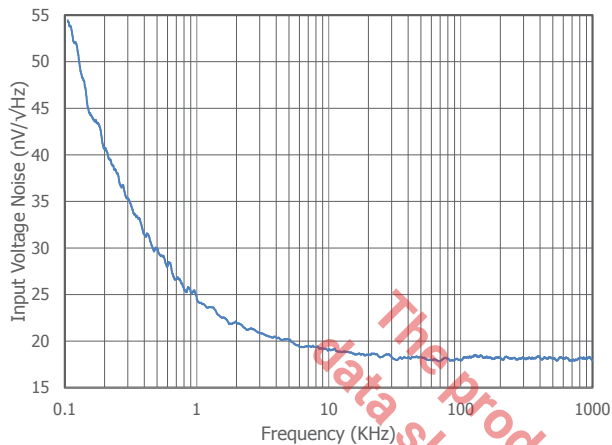
-3dB BW vs Output Voltage



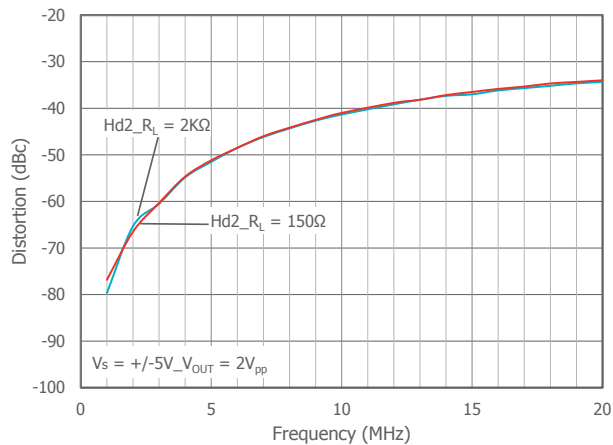
Typical Performance Characteristics at ±5V

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 2\text{k}\Omega$ to GND, $G = +2$, $R_F = 1.5\text{k}\Omega$; unless otherwise noted.

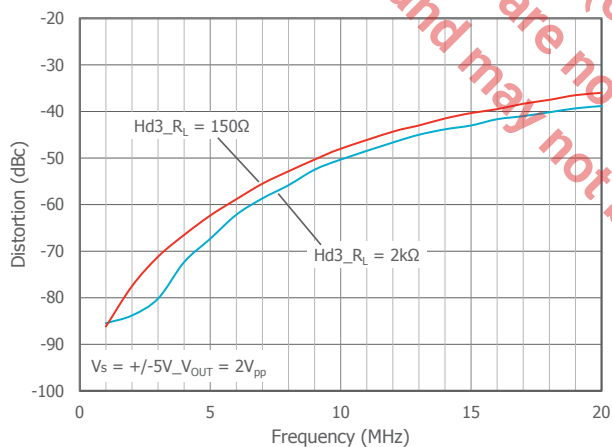
Input Voltage Noise vs Frequency



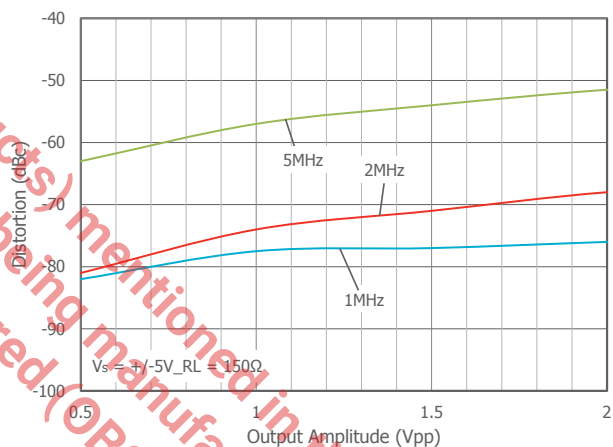
2nd Harmonic Distortion vs R_L over Frequency



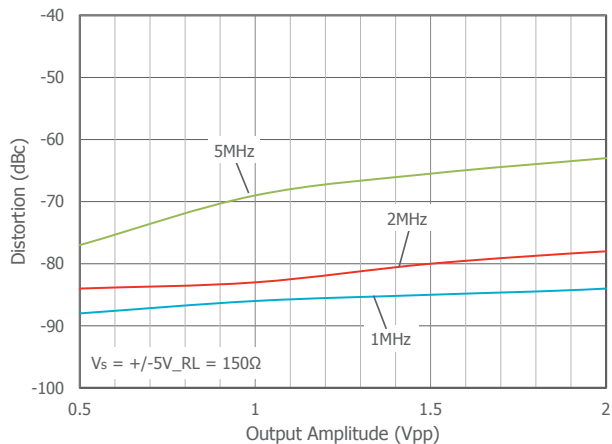
3rd Harmonic Distortion vs R_L over Frequency



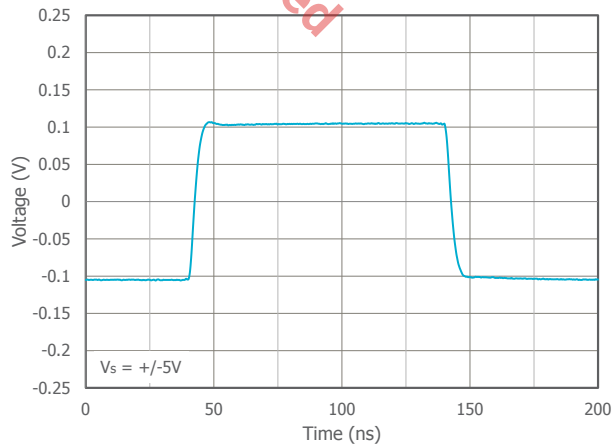
2nd Harmonic Distortion vs V_O over Frequency



3rd Harmonic Distortion vs V_O over Frequency



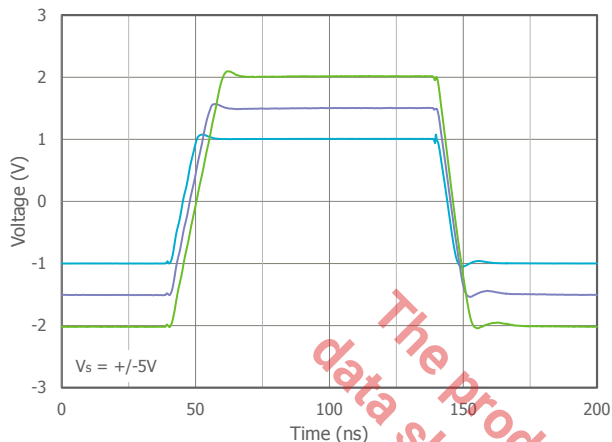
Non-Inverting Small Signal Pulse Response



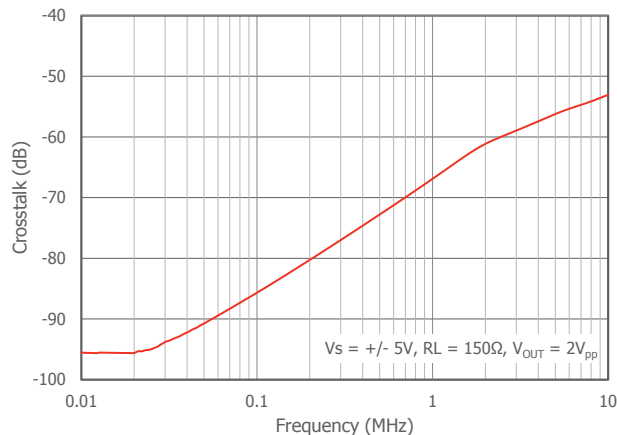
Typical Performance Characteristics at ±5V

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 2\text{k}\Omega$ to GND, $G = +2$, $R_F = 1.5\text{k}\Omega$; unless otherwise noted.

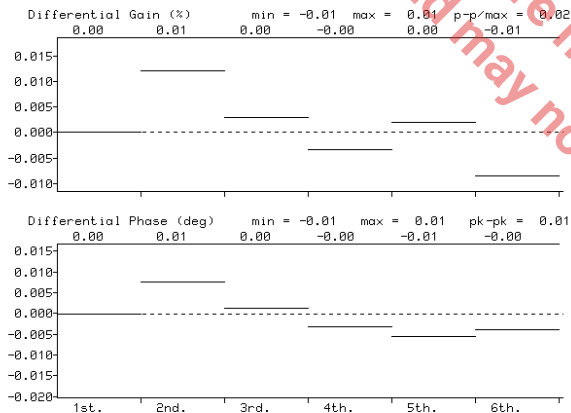
Non-Inverting Large Signal Pulse Response



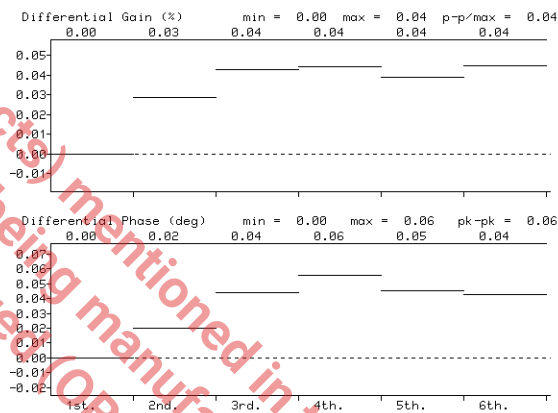
Crosstalk vs Frequency (CLC2007)



Differential Gain & Phase_DC Coupled



Differential Gain & Phase_AC Coupled



Application Information

General Description

The CLC1007, CLC2007, and CLC4007 are single supply, general purpose, voltage-feedback amplifiers fabricated on a complementary bipolar process using a patent pending topography. They feature a rail-to-rail output stage and is unity gain stable. Both gain bandwidth and slew rate are insensitive to temperature.

The common mode input range extends to 300mV below ground and to 0.9V below V_s . Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition.

The design is short circuit protected and offers “soft” saturation protection that improves recovery time.

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applications.

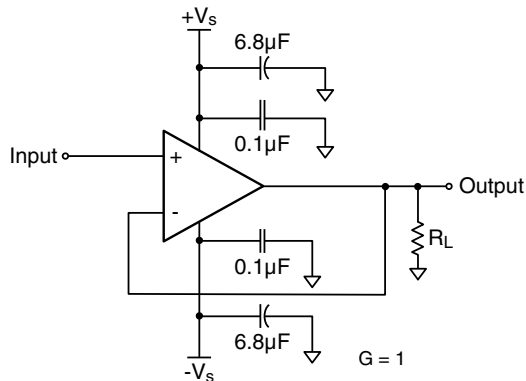


Figure 3: Unity Gain Circuit

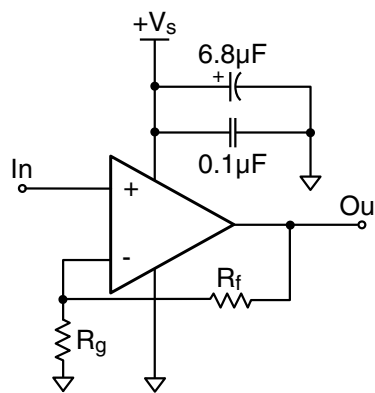


Figure 4: Single Supply Non-Inverting Gain Circuit

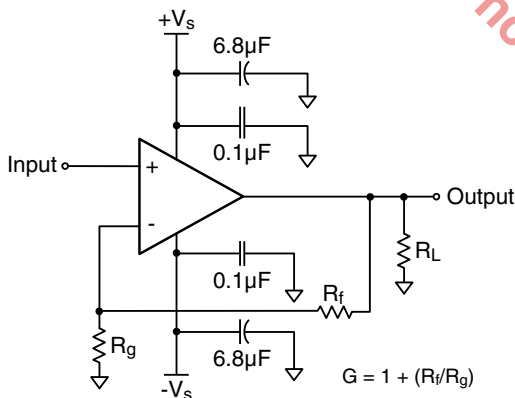


Figure 1: Typical Non-Inverting Gain Circuit

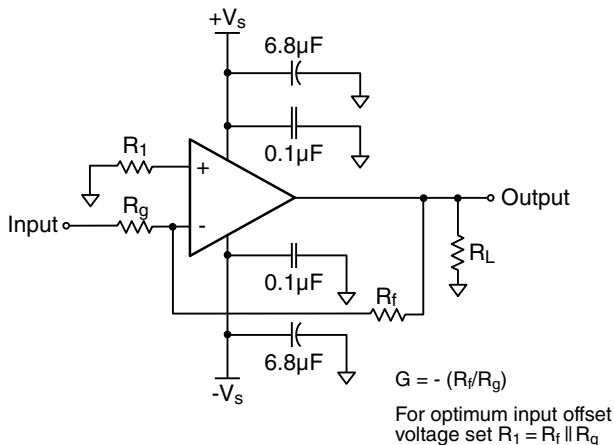


Figure 2: Typical Inverting Gain Circuit

Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The CLC1007, CLC2007, and CLC4007 will typically recover in less than 20ns from an overdrive condition. Figure 5 shows the CLC2007 in an overdriven condition.

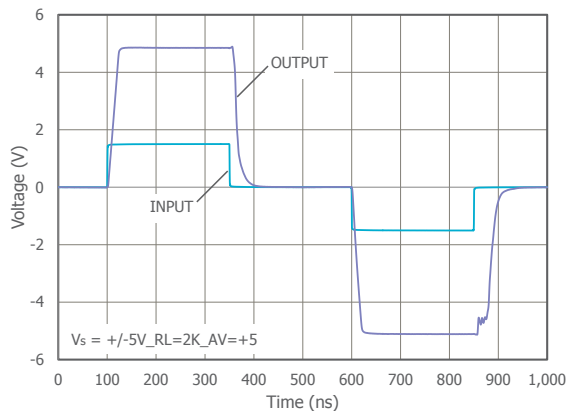


Figure 5: Overdrive Recovery

Power Dissipation

Power dissipation should not be a factor when operating under the stated 2kΩ load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond its intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 170°C. To calculate the junction temperature, the package thermal resistance value θ_{JA} (θ_{JA}) is used along with the total die power dissipation.

$$T_{\text{Junction}} = T_{\text{Ambient}} + (\theta_{JA} \times P_D)$$

Where T_{Ambient} is the temperature of the working environment.

In order to determine P_D , the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{\text{Supply}} - P_{\text{Load}}$$

Supply power is calculated by the standard power equation.

$$P_{\text{Supply}} = V_{\text{Supply}} \times I_{\text{RMSSupply}}$$

$$V_{\text{Supply}} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{\text{Load}} = ((V_{\text{Load}})_{\text{RMS}})^2 / R_{\text{LoadEff}}$$

The effective load resistor (R_{LoadEff}) will need to include the effect of the feedback network. For instance,

R_{LoadEff} in Figure 3 would be calculated as:

$$R_L \parallel (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{\text{Quiescent}} + P_{\text{Dynamic}} - P_{\text{Load}}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply} . Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{\text{Load}})_{\text{RMS}} = V_{\text{peak}} / \sqrt{2}$$

$$(I_{\text{Load}})_{\text{RMS}} = (V_{\text{Load}})_{\text{RMS}} / R_{\text{LoadEff}}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{\text{Dynamic}} = (V_{S+} - V_{\text{Load}})_{\text{RMS}} \times (I_{\text{Load}})_{\text{RMS}}$$

Assuming the load is referenced in the middle of the power rails or $V_{\text{Supply}}/2$.

The CLC1007 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. Figure 6 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

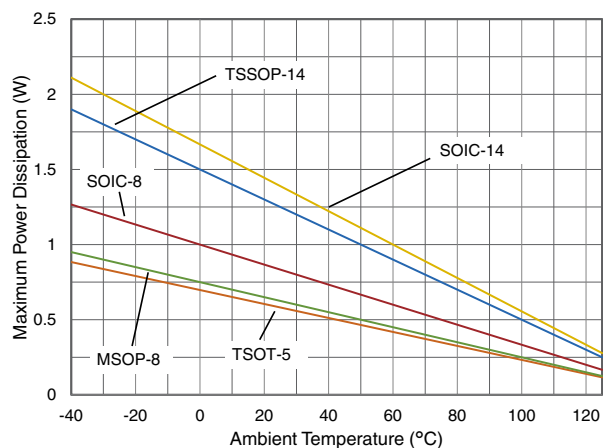


Figure 6. Maximum Power Derating

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S , between the amplifier and the load to help improve stability and settling performance. Refer to Figure 7.

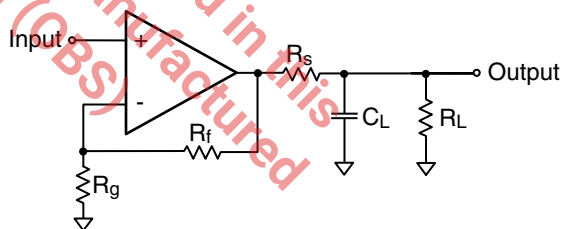


Figure 7. Addition of R_S for Driving Capacitive Loads

Table 1 provides the recommended R_S for various capacitive loads. The recommended R_S values result in approximately <1dB peaking in the frequency response.

| C_L (pF) | R_S (Ω) | -3dB BW (MHz) |
|------------|--------------------|---------------|
| 22pF | 0 | 118 |
| 47pF | 15 | 112 |
| 100pF | 15 | 91 |
| 492pF | 6.5 | 59 |

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Exar has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8 μ F and 0.1 μ F ceramic capacitors for power supply decoupling
- Place the 6.8 μ F capacitor within 0.75 inches of the power pin
- Place the 0.1 μ F capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

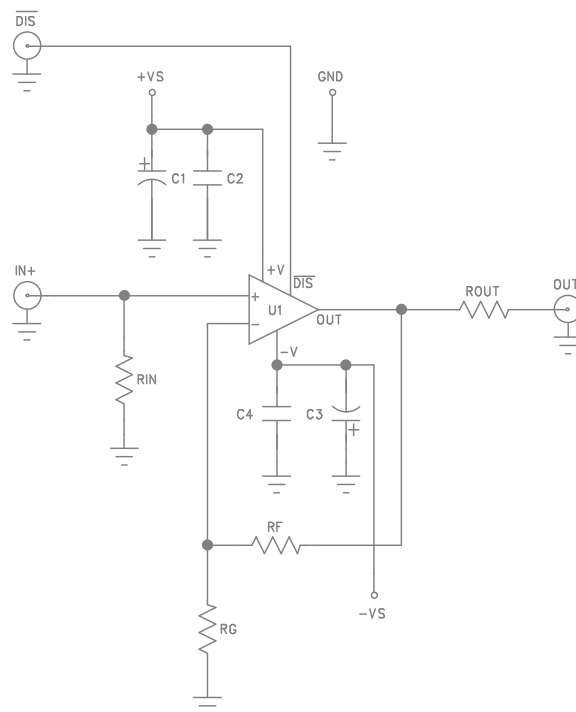


Figure 8. CEB002 & CEB003 Schematic

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

| Evaluation Board # | Products |
|--------------------|------------------|
| CEB002 | CLC1007 in TSOT |
| CEB003 | CLC1007 in SOIC |
| CEB006 | CLC2007 in SOIC |
| CEB010 | CLC2007 in MSOP |
| CEB018 | CLC4007 in SOIC |
| CEB019 | CLC4007 in TSSOP |

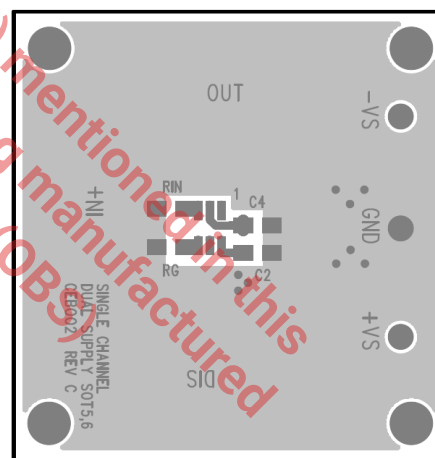


Figure 9. CEB002 Top View

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 8-20. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short $-V_S$ to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

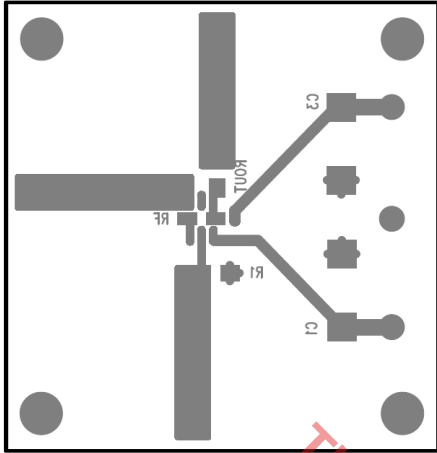


Figure 10. CEB002 Bottom View

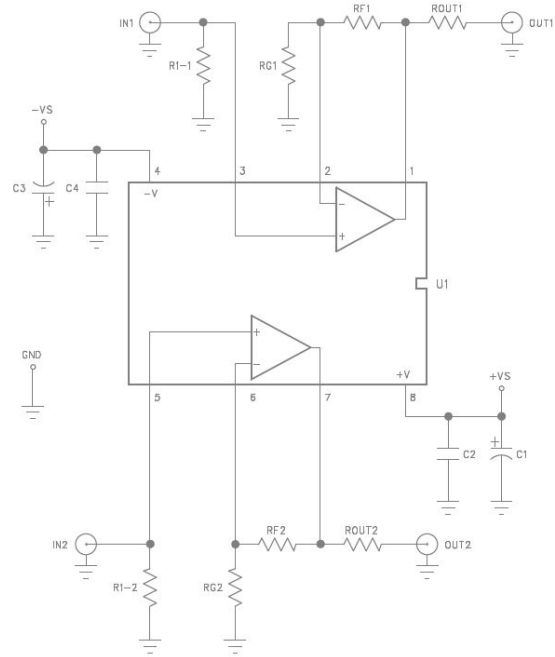


Figure 13. CEB006 & CEB010 Schematic

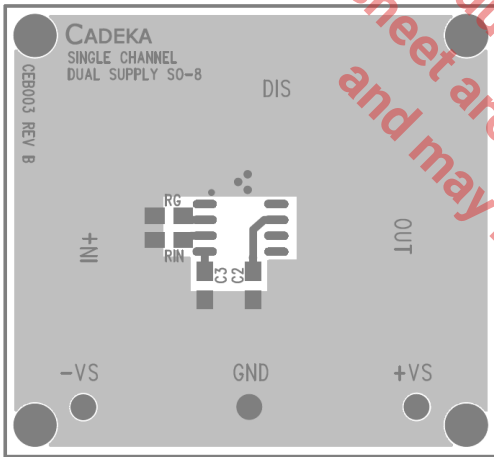


Figure 11. CEB003 Top View

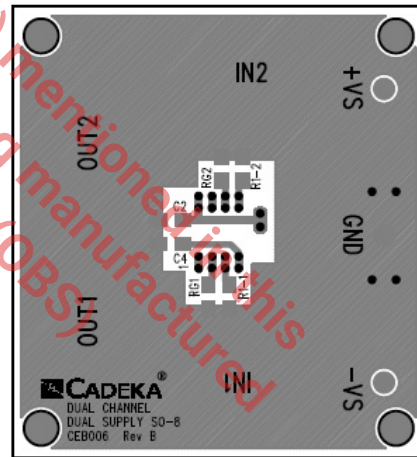


Figure 14. CEB006 Top View

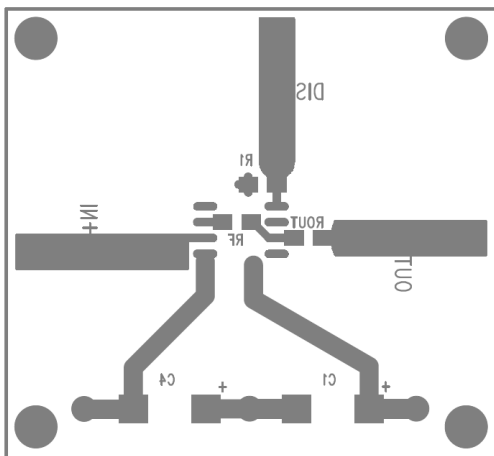


Figure 12. CEB003 Bottom View

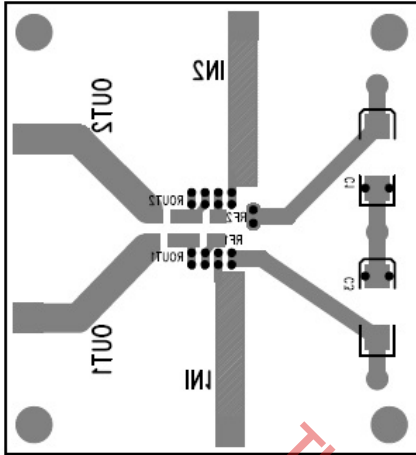


Figure 15. CEB006 Bottom View

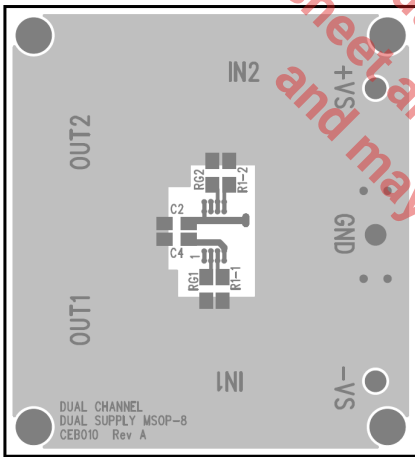


Figure 16. CEB010 Top View

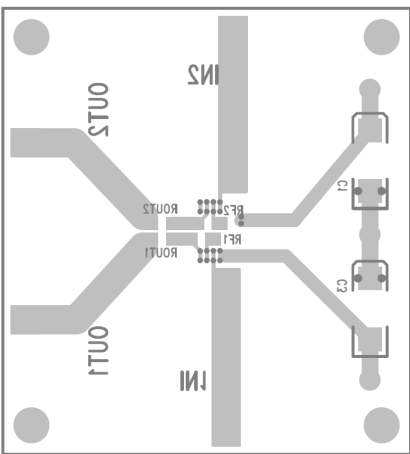


Figure 17. CEB010 Bottom View

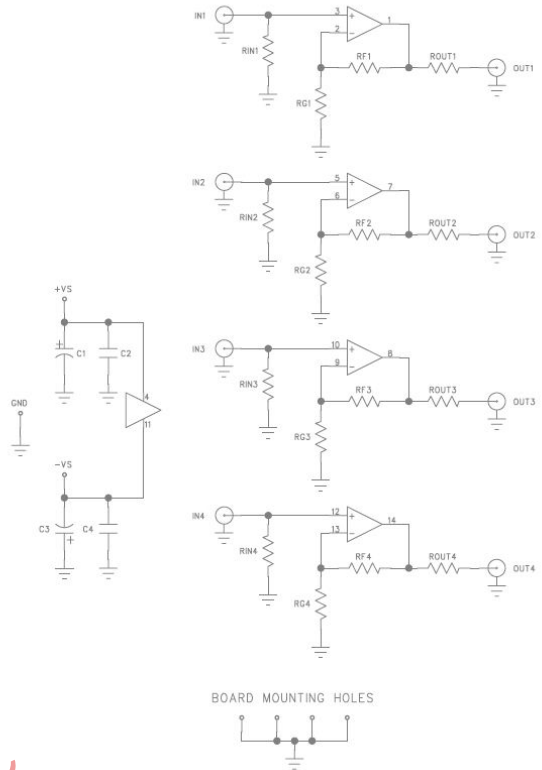


Figure 18. CEB018 Schematic

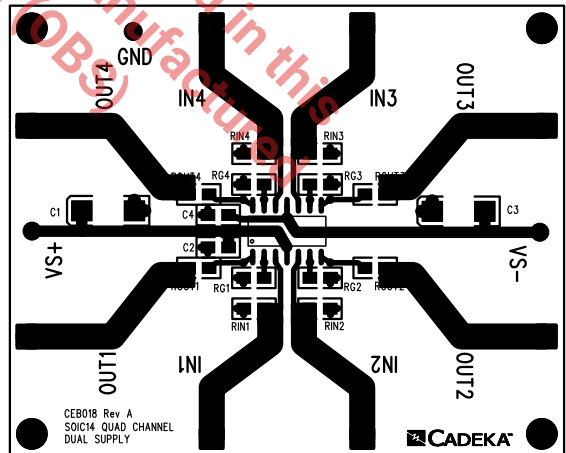


Figure 19. CEB018 Top View

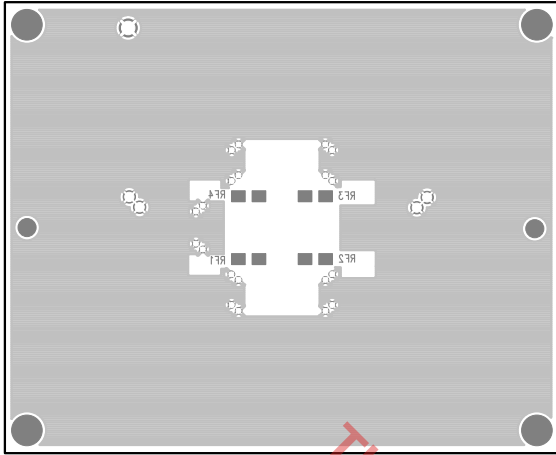
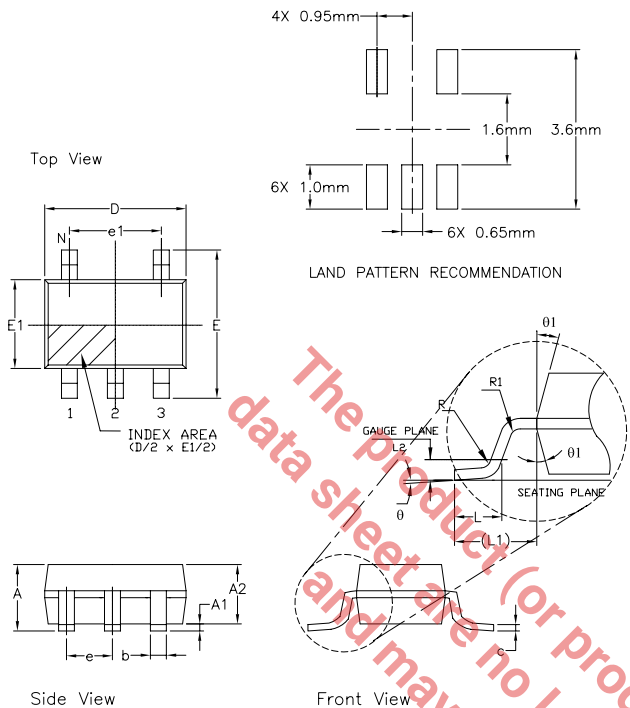


Figure 20. CEB018 Bottom View

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

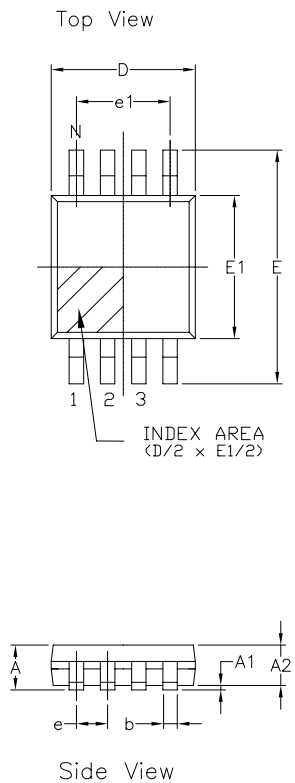
Mechanical Dimensions

TSOT-5 Package

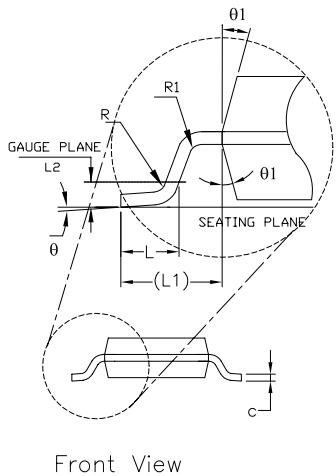


| 5 Pin TSOT (OPTION 2) | | | | | | |
|-----------------------|-----------------------------------|------|------|---------------------------------------|-------|-------|
| SYMBOLS | DIMENSION IN MM (Control Unit) | | | DIMENSION IN INCH (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.75 | — | 0.80 | 0.030 | — | 0.031 |
| A1 | 0.00 | — | 0.05 | 0.000 | — | 0.002 |
| A2 | 0.70 | 0.75 | 0.78 | 0.028 | 0.030 | 0.031 |
| b | 0.35 | — | 0.50 | 0.012 | — | 0.020 |
| c | 0.10 | — | 0.20 | 0.003 | — | 0.008 |
| D | 2.90 BSC | | | 0.114 BSC | | |
| E | 2.80 BSC | | | 0.110 BSC | | |
| E1 | 1.60 BSC | | | 0.063 BSC | | |
| e | 0.95 BSC | | | 0.038 BSC | | |
| e1 | 1.90 BSC | | | 0.075 BSC | | |
| L | 0.37 | 0.45 | 0.60 | 0.012 | 0.018 | 0.024 |
| L1 | 0.60 REF | | | 0.024 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R | 0.10 | — | — | 0.004 | — | — |
| R1 | 0.10 | — | 0.25 | 0.004 | — | 0.010 |
| θ | 0° | 4° | 8° | 0° | 4° | 8° |
| θ 1 | 4° | 10° | 12° | 4° | 10° | 12° |
| N | 5 | | | 5 | | |

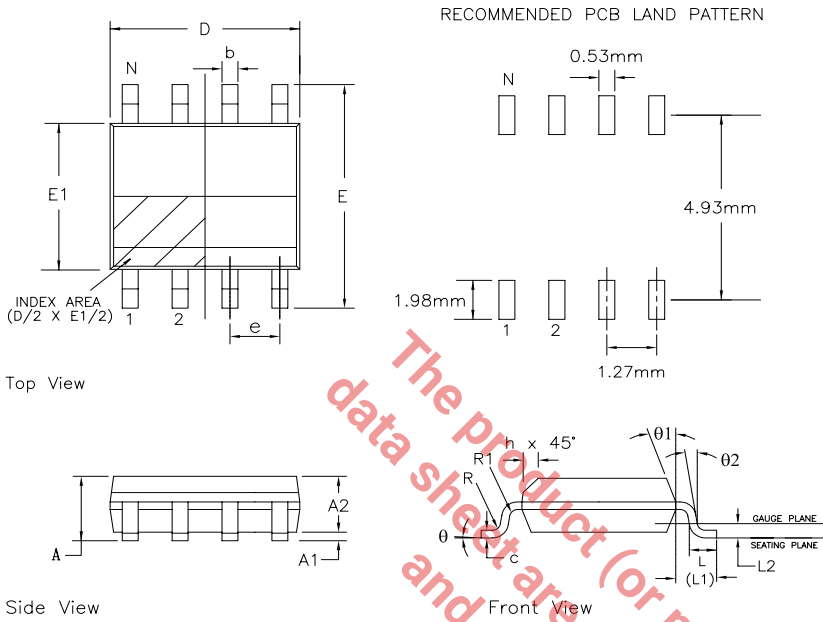
MSOP-8 Package



| 8 Pin MSOP JEDEC MO-187 Variation AA | | | | | | |
|--------------------------------------|------------------------------------|------|------|--|-------|-------|
| SYMBOLS | DIMENSIONS IN MM (Control Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | — | — | 1.10 | — | — | 0.043 |
| A1 | 0.00 | — | 0.05 | 0.000 | — | 0.006 |
| A2 | 0.75 | 0.85 | 0.95 | 0.030 | 0.033 | 0.037 |
| b | 0.22 | — | 0.38 | 0.009 | — | 0.015 |
| c | 0.08 | — | 0.23 | 0.003 | — | 0.009 |
| E | 4.90 BSC | | | 0.193 BSC | | |
| E1 | 3.00 BSC | | | 0.118 BSC | | |
| e | 0.65 BSC | | | 0.026 BSC | | |
| e1 | 1.95 BSC | | | 0.077 BSC | | |
| L | 0.40 | 0.60 | 0.80 | 0.016 | 0.024 | 0.031 |
| L1 | 0.95 REF | | | 0.037 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R | 0.07 | — | — | 0.003 | — | — |
| R1 | 0.07 | — | — | 0.003 | — | — |
| θ | 0° | — | 8° | 0° | — | 8° |
| θ 1 | 5° | — | 15° | 5° | — | 15° |
| D | 3.00 BSC | | | 0.118 BSC | | |
| N | 8 | | | 8 | | |

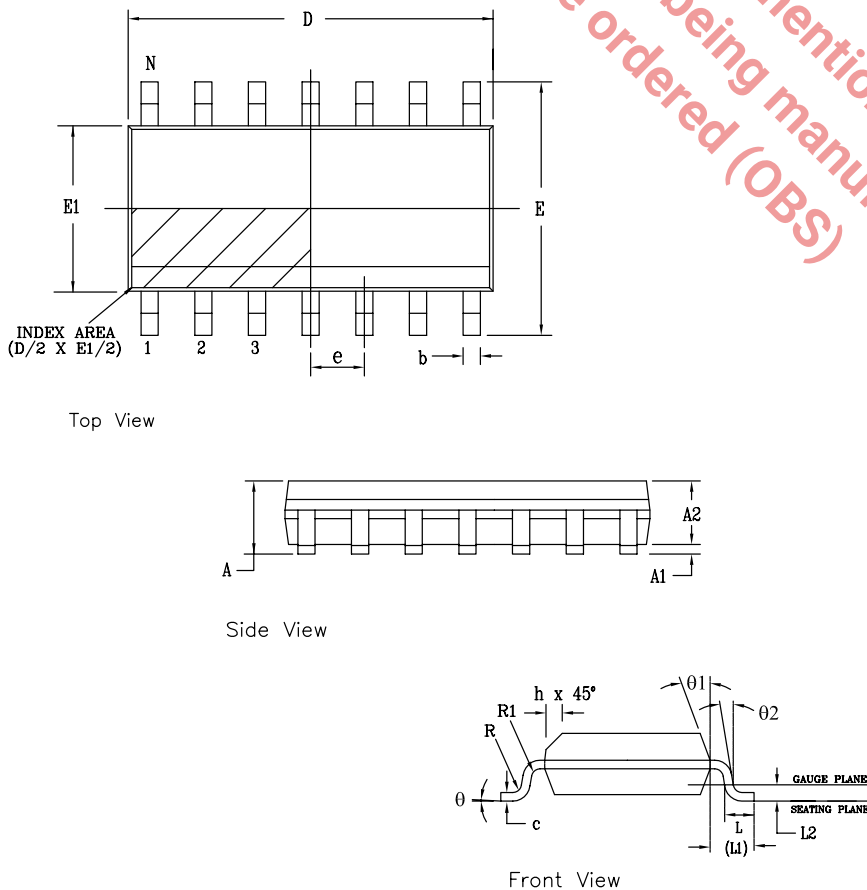


SOIC-8 Package



| 8 Pin SOICN JEDEC MS-012 Variation AA | | | | | | |
|---------------------------------------|---------------------------------|-----|------|-------------------------------------|-----|-------|
| SYMBOLS | DIMENSIONS IN MM (Control Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.35 | — | 1.75 | 0.053 | — | 0.069 |
| A1 | 0.10 | — | 0.25 | 0.004 | — | 0.010 |
| A2 | 1.25 | — | 1.65 | 0.049 | — | 0.065 |
| b | 0.31 | — | 0.51 | 0.012 | — | 0.020 |
| c | 0.17 | — | 0.25 | 0.007 | — | 0.010 |
| E | 6.00 BSC | | | 0.236 BSC | | |
| E1 | 3.90 BSC | | | 0.154 BSC | | |
| e | 1.27 BSC | | | 0.050 BSC | | |
| h | 0.25 | — | 0.50 | 0.010 | — | 0.020 |
| L | 0.40 | — | 1.27 | 0.016 | — | 0.050 |
| L1 | 1.04 REF | | | 0.041 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R | 0.07 | — | — | 0.003 | — | — |
| R1 | 0.07 | — | — | 0.003 | — | — |
| theta | 0° | | 8° | 0° | | 8° |
| theta1 | 5° | | 15° | 5° | | 15° |
| theta2 | 0° | | — | 0° | | — |
| D | 4.90 BSC | | | 0.193 BSC | | |
| N | 8 | | | 8 | | |

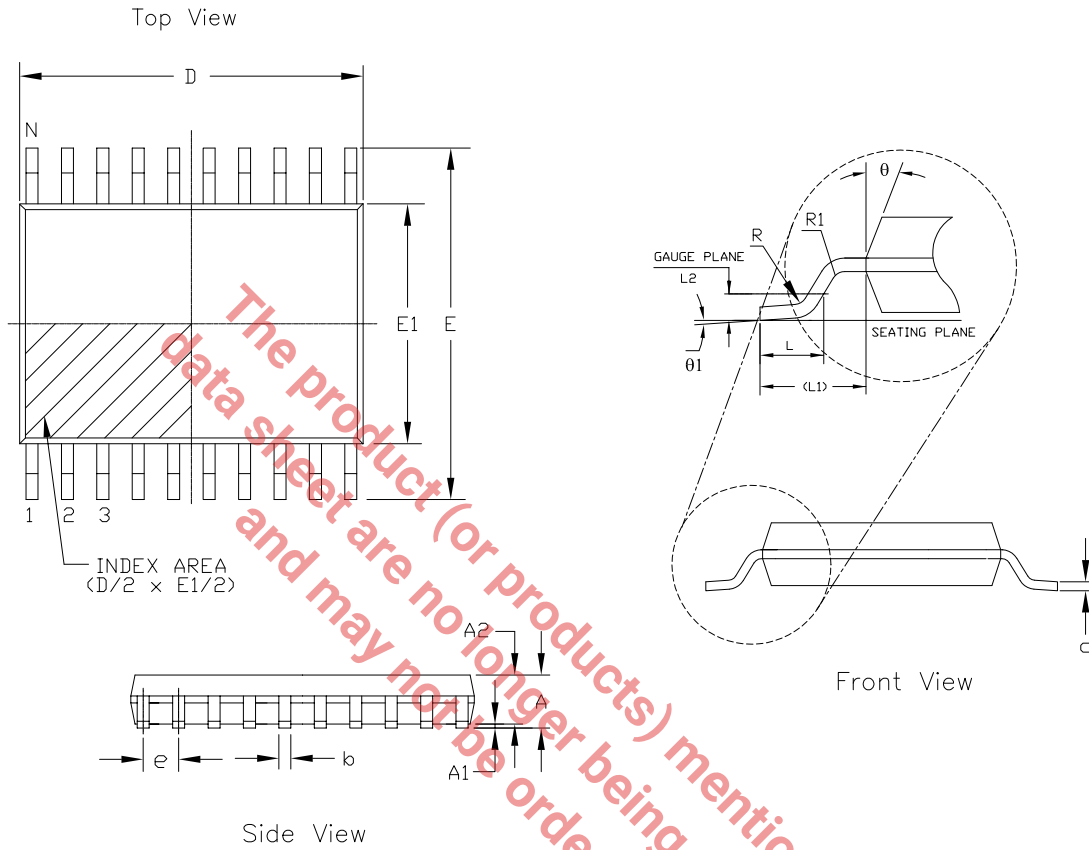
SOIC-14 Package



| PACKAGE OUTLINE NSOIC .150" BODY JEDEC MS-012 | | | | | | |
|---|--|-----|------|--|-----|-------|
| SYMBOLS | COMMON DIMENSIONS IN MM (Control Unit) | | | COMMON DIMENSIONS IN INCH (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.35 | — | 1.75 | 0.053 | — | 0.069 |
| A1 | 0.10 | — | 0.25 | 0.004 | — | 0.010 |
| A2 | 1.25 | — | 1.65 | 0.049 | — | 0.065 |
| b | 0.31 | — | 0.51 | 0.012 | — | 0.020 |
| c | 0.17 | — | 0.25 | 0.007 | — | 0.010 |
| E | 6.00 BSC | | | 0.236 BSC | | |
| E1 | 3.90 BSC | | | 0.154 BSC | | |
| e | 1.27 BSC | | | 0.050 BSC | | |
| h | 0.25 | — | 0.50 | 0.010 | — | 0.020 |
| L | 0.40 | — | 1.27 | 0.016 | — | 0.050 |
| L1 | 1.04 REF | | | 0.041 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R | 0.07 | — | — | 0.003 | — | — |
| R1 | 0.07 | — | — | 0.003 | — | — |
| theta | 0° | | 8° | 0° | | 8° |
| theta1 | 5° | | 15° | 5° | | 15° |
| theta2 | 0° | | — | 0° | | — |
| D | SEE VARIATIONS | | | SEE VARIATIONS | | |
| N | SEE VARIATIONS | | | SEE VARIATIONS | | |

| VARIATION D | | | | | | |
|-------------|---------------------------------|-----|-----|-------------------------------------|-----|-----|
| SYMBOLS | DIMENSIONS IN MM (Control Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| AA | 4.90 BSC | | | 0.193 BSC | | |
| AB | 8.65 BSC | | | 0.341 BSC | | |
| AC | 9.90 BSC | | | 0.390 BSC | | |

TSSOP-14 Package



The product (or products) mentioned in this data sheet are no longer being manufactured (OBSOLETE) and may not be ordered.

| 14 Pin TSSOP JEDEC MO-153 Variation AB-1 | | | | | | |
|--|------------------------------------|------|------|--|-------|-------|
| SYMBOLS | DIMENSIONS IN MM (Control Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 0.80 | 1.00 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | — | 0.30 | 0.007 | — | 0.012 |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| E | 6.40 BSC | | | 0.252 BSC | | |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.177 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R | 0.09 | — | — | 0.035 | — | — |
| R1 | 0.09 | — | — | 0.035 | — | — |
| θ | 12° REF | | | 12° REF | | |
| $\theta1$ | 0° | — | 8° | 0° | — | 8° |
| D | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.200 |
| N | 14 | | | 14 | | |

Ordering Information

| Part Number | Package | Green | Operating Temperature Range | Packaging |
|------------------------------|------------------|-------|-----------------------------|------------------|
| CLC1007 Ordering Information | | | | |
| CLC1007IST5X | TSOT-5 | Yes | -40°C to +125°C | Tape & Reel |
| CLC1007IST5MTR | TSOT-5 | Yes | -40°C to +125°C | Mini Tape & Reel |
| CLC1007IST5EVB | Evaluation Board | N/A | N/A | N/A |
| CLC1007ISO8X | SOIC-8 | Yes | -40°C to +125°C | Tape & Reel |
| CLC1007ISO8MTR | SOIC-8 | Yes | -40°C to +125°C | Mini Tape & Reel |
| CLC1007ISO8EVB | Evaluation Board | N/A | N/A | N/A |
| CLC2007 Ordering Information | | | | |
| CLC2007ISO8X | SOIC-8 | Yes | -40°C to +125°C | Tape & Reel |
| CLC2007ISO8MTR | SOIC-8 | Yes | -40°C to +125°C | Mini Tape & Reel |
| CLC2007ISO8EVB | Evaluation Board | N/A | N/A | N/A |
| CLC2007IMP8X | MSOP-8 | Yes | -40°C to +125°C | Tape & Reel |
| CLC2007IMP8MTR | MSOP-8 | Yes | -40°C to +125°C | Mini Tape & Reel |
| CLC2007IMP8EVB | Evaluation Board | N/A | N/A | N/A |
| CLC4007 Ordering Information | | | | |
| CLC4007ITP14X | TSSOP-14 | Yes | -40°C to +125°C | Tape & Reel |
| CLC4007ITP14MTR | TSSOP-14 | Yes | -40°C to +125°C | Mini Tape & Reel |
| CLC4007ITP14EVB | Evaluation Board | N/A | N/A | N/A |
| CLC4007ISO14X | SOIC-14 | Yes | -40°C to +125°C | Tape & Reel |
| CLC4007ISO14MTR | SOIC-14 | Yes | -40°C to +125°C | Mini Tape & Reel |
| CLC4007ISO14EVB | Evaluation Board | N/A | N/A | N/A |

Moisture sensitivity level for all parts is MSL-1.

Revision History

| Revision | Date | Description |
|------------------|---------------|---|
| 1D (ECN 1451-07) | December 2014 | Reformat into Exar data sheet template. Updated ordering information table to include MTR and EVB part numbers. Increased "I" temperature range from +85 to +125°C. Removed "A" temp grade parts, since "I" is now equivalent. Updated thermal resistance numbers and package outline drawings. |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

For Further Assistance:

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Exar Technical Documentation: <http://www.exar.com/techdoc/>

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A New Direction in Mixed-Signal

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