

GENERAL DESCRIPTION

The XRT83SH38 is a fully integrated 8-channel short-haul line interface unit (LIU) that operates from a single 3.3V power supply. Using internal termination, the LIU provides one bill of materials to operate in T1, E1, or J1 mode with minimum external components. The LIU features are programmed through a standard microprocessor interface, serial interface or controlled through Hardware mode. EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays.

The on-chip clock synthesizer generates T1/E1/J1 clock rates from a selectable external clock frequency and outputs a clock reference of the line rate chosen.

Additional features include RLOS, a 16-bit LCV counter for each channel, AIS, QRSS generation/detection, TAOS, DMO, and diagnostic loopback modes.

APPLICATIONS

- T1 Digital Cross-Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks

FIGURE 1. BLOCK DIAGRAM OF THE XRT83SH38 T1/E1/J1 LIU (HOST MODE)

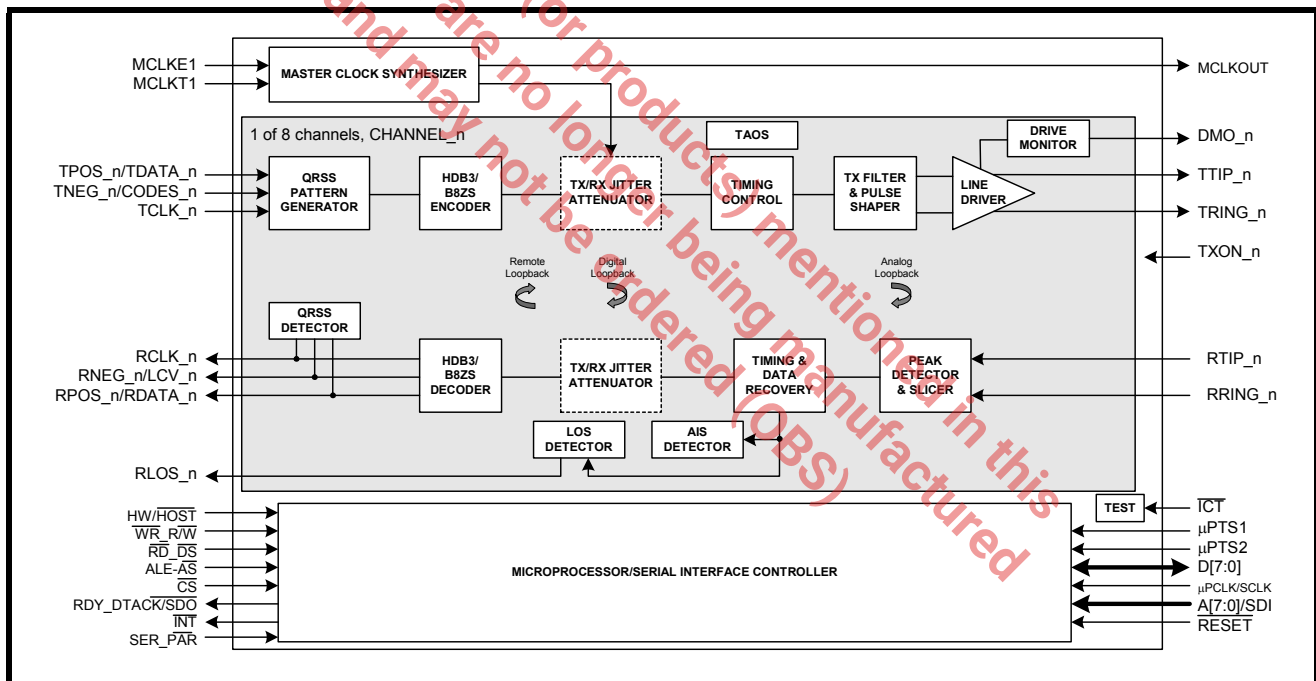
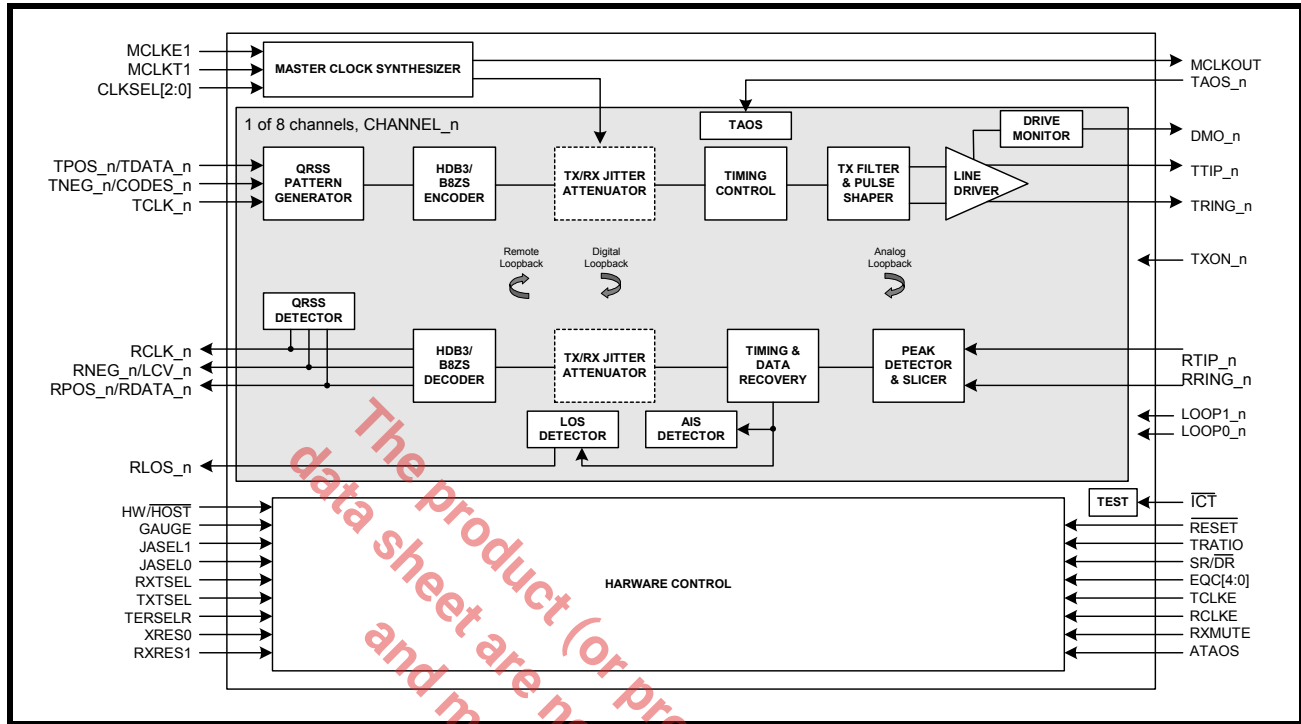


FIGURE 2. BLOCK DIAGRAM OF THE XRT83SH38 T1/E1/J1 LIU (HARDWARE MODE)



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FEATURES

- Fully integrated eight channel short-haul transceivers for E1, T1 or J1 applications
- Programmable Transmit Pulse Shaper for E1, T1 or J1 short-haul interfaces
- Five fixed transmit pulse settings for T1 short-haul applications
- Receive monitor mode handles 0 to 29dB resistive attenuation along with 0 to 6dB of cable attenuation for E1 and 0 to 3dB of cable attenuation for T1 modes
- Internal impedance matching for 75Ω, 100Ω, 110Ω and 120Ω
- Tri-State transmit output and receive input capability for redundancy applications
- Provides High Impedance for Tx and Rx during power off
- Transmit return loss meets or exceeds ETSI 300-166 standard
- On-chip digital clock recovery circuit for high input jitter tolerance
- Crystal-less digital jitter attenuator with 32-bit or 64-bit FIFO selectable either in transmit or receive path
- On-chip frequency multiplier generates T1 or E1 Master clocks from variety of external clock sources
- High receiver interference immunity
- On-chip transmit short-circuit protection and limiting, and driver fail monitor output (DMO)
- Receive loss of signal (RLOS) output
- On-chip HDB3/B8ZS/AMI encoder/decoder functions
- QRSS pattern generator and detection for testing and monitoring
- Error and Bipolar Violation Insertion and Detection
- Transmit All Ones (TAOS) Generators and Detectors
- Supports Local Analog, Remote, Digital and Dual Loop-Back Modes
- Meets or exceeds T1 and E1 short-haul network access specifications in ITU G.703, G.775, G.736 and G.823; TR-TSY-000499; ANSI T1.403 and T1.408; ETSI 300-166 and AT&T Pub 62411
- Supports both **Hardware** and **Host** (parallel Microprocessor or Serial) interface for programming
- JTAG Support
- Programmable Interrupt
- Low power dissipation
- Logic inputs accept either 3.3V or 5V levels
- Single 3.3V Supply Operation
- 225 ball BGA package
- -40°C to +85°C Temperature Range

ORDERING INFORMATION

| PART NUMBER | PACKAGE | OPERATING TEMPERATURE RANGE |
|-------------|--------------|-----------------------------|
| XRT83SH38IB | 225 Ball BGA | -40°C to +85°C |

XRT83SH38

8-CHANNEL T1/E1/J1 SHORT-HAUL LINE INTERFACE UNIT

| | | | | | | | | | | | | | | | | | | |
|---|---------|----------|----------|----------|--------|-----------|--------|----------|----------|----------|---------|--------|--------|--------|---------|---------|-----------|-----------|
| A | NC1 | RNEG_0 | TCLK_1 | TPOS_1 | TAOS_2 | RDY_DTACK | ALE_AS | CLKSEL0 | DVDD | A[1] | A[3] | A[7] | TXON_0 | JASEL0 | TCLK_2 | RLOS_3 | RCLK_3 | NC4 |
| B | NC5 | RPOS_0 | RCLK_0 | TCLK_0 | TNEG_1 | TAOS_1 | CS | CLKSEL1 | DGND | A[2] | A[6] | TXON_3 | JASEL1 | TPOS_2 | TNEG_3 | RNEG_3 | RPOS_3 | NC12 |
| C | RTIP_0 | RVDD_0 | RLOS_0 | TNEG_0 | TPOS_0 | TAOS_3 | RD_DS | CLKSEL2 | DGND_PDR | A[0] | A[5] | TXON_2 | DMO_3 | TCLK_3 | DMO_2 | TTIP_3 | TGND_3 | RTIP_3 |
| D | RRING_0 | RGND_0 | TGND_0 | DMO_1 | DMO_0 | TAOS_0 | WR_RW | DGND_DR | DVDD_DR | DVDD_PDR | A[4] | TXON_1 | TNEG_2 | TPOS_3 | RPOS_2 | RVDDD_3 | RGND_3 | RRING_3 |
| E | NC6 | TRING_0 | TTIP_0 | TVDD_0 | RVDD_1 | | | | | | | | | | TGND_2 | TRING_3 | TVDD_3 | NC11 |
| F | RRING_1 | TGND_1 | TRING_1 | TVDD_1 | | | | | | | | | | | TRING_2 | TVDD_2 | TTIP_2 | RRING_2 |
| G | RTIP_1 | RPOS_1 | RGND_1 | TTIP_1 | | | | | | | | | | | DGND_DR | RVDD_2 | RGND_2 | RTIP_2 |
| H | MCLKOUT | RNEG_1 | RCLK_1 | RLOS_1 | | | | | | | | | | | RLOS_2 | RCLK_2 | DGND_UJP | RNEG_2 |
| J | MCLKE1 | VDDPLL_2 | VDDPLL_1 | DVDD_DR | | | | | | | | | | | RLOS_6 | PTS1 | AGND_BIAS | GAUGE |
| K | MCLKT1 | DGND_DR | GNDPLL_1 | SR_DR | | | | | | | | | | | DVDD_DR | RXON | AVDD_BIAS | DVDDD_UJP |
| L | RTIP_5 | RLOS_5 | RCLK_5 | GNDPLL_2 | | | | | | | | | | | PTS2 | INT | RPOS_6 | RTIP_6 |
| M | RRING_5 | RGND_5 | RPOS_5 | RNEG_5 | | | | | | | | | | | RCLK_6 | RNEG_6 | RGND_6 | RRING_6 |
| N | NC7 | TTIP_5 | RVDD_5 | TRING_5 | | | | | | | | | | | TVDD_6 | TTIP_6 | RVDD_6 | NC10 |
| P | TVDD_5 | TRING_4 | TGND_5 | DMO_5 | | | | | | | | | | | TVDD_7 | TTIP_7 | TRING_7 | NC9 |
| R | NC8 | TTIP_4 | TGND_4 | TVDD_4 | DMO_4 | TAOS_7 | D[0] | DGND_PDR | DVDD_DR | RXRES1 | TERSEL0 | TXON_6 | TXON_7 | TNEG_7 | TRING_6 | TGND_7 | RGND_7 | RRING_7 |
| T | RRING_4 | RGND_4 | TCLK_4 | RNEG_4 | TCLK_5 | TAOS_4 | D[7] | RESET | DGND_DR | HW_FOST | TERSEL1 | RXMUTE | uPCLK | TPOS_7 | RLOS_7 | TGND_6 | RPOS_7 | RTIP_7 |
| U | RTIP_4 | RPOS_4 | RCLK_4 | TNEG_4 | TPOS_5 | TAOS_5 | D[6] | D[2] | D[1] | DVDD_PDR | RXTSEL | TEST | TXON_5 | TNEG_6 | TCLK_7 | RCLK_7 | DMO_6 | RVDD_7 |
| V | NC2 | RVDD_4 | RLOS_4 | TPOS_4 | TNEG_5 | TAOS_6 | D[5] | D[4] | D[3] | RXRES0 | TXTSEL | ICT | TXON_4 | DMO_7 | TPOS_6 | TCLK_6 | RNEG_7 | NC3 |

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XRT83SH38
(Top View)
225 Ball BGA

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PIN DESCRIPTION BY FUNCTION

RECEIVE SECTION

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|--|--|------|--|
| RXON | K16 | I | <p>Receiver On <u>Hardware Mode Only</u></p> <p>This pin is used to enable the receivers for all channels. By default, the receivers are turned on in hardware mode. To turn the receivers off, this "Low".</p> <p><i>NOTE: Internally pulled "High" with 50kΩ resistor.</i></p> |
| RLOS0 RLOS1 RLOS2 RLOS3 RLOS4 RLOS5 RLOS6 RLOS7 | C3 H4 H15 A16 V3 L2 J15 T15 | O | <p>Receive Loss of Signal</p> <p>When a receive loss of signal occurs according to ITU-T G.775, the RLOS pin will go "High" for a minimum of one RCLK cycle. RLOS will remain "High" until the loss of signal condition clears. See the Receive Loss of Signal section of this datasheet for more details.</p> <p><i>NOTE: This pin can be used for redundancy applications to initiate an automatic switch to a backup card.</i></p> |
| RCLK0 RCLK1 RCLK2 RCLK3 RCLK4 RCLK5 RCLK6 RCLK7 | B3 H3 H16 A17 U3 L3 M15 U16 | O | <p>Receive Clock Output</p> <p>RCLK is the recovered clock from the incoming data stream. If the incoming signal is absent or RTIP/RRING are in "High-Z", RCLK maintains its timing by using an internal master clock as its reference. RPOS/RNEG data can be updated on either edge of RCLK selected by RCLKE.</p> <p><i>NOTE: RCLKE is a global setting that applies to all 8 channels.</i></p> |
| RNEG/LCV0 RNEG/LCV1 RNEG/LCV2 RNEG/LCV3 RNEG/LCV4 RNEG/LCV5 RNEG/LCV6 RNEG/LCV7 | A2 H2 H18 B16 T4 M4 M16 V17 | O | <p>RNEG/LCV_OF Output</p> <p>In dual rail mode, this pin is the receive negative data output. In single rail mode, this pin is a Line Code Violation / Counter Overflow indicator. If LCV is selected by programming the appropriate global register and if a line code violation, a bi-polar violation, or excessive zeros occur, the LCV pin will pull "High" for a minimum of one RCLK cycle. LCV will remain "High" until there are no more violations. However, if OF (Overflow) is selected the LCV pin will pull "High" if the internal LCV counter is saturated. The LCV pin will remain "High" until the LCV counter is reset.</p> |
| RPOS0 RPOS1 RPOS2 RPOS3 RPOS4 RPOS5 RPOS6 RPOS7 | B2 G2 D15 B17 U2 M3 L17 T17 | O | <p>RPOS/RDATA Output</p> <p>Receive digital output pin. In dual rail mode, this pin is the receive positive data output. In single rail mode, this pin is the receive non-return to zero (NRZ) data output.</p> |

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|--|--|------|---|
| RTIP0 RTIP1 RTIP2 RTIP3 RTIP4 RTIP5 RTIP6 RTIP7 | C1 G1 G18 C18 U1 L1 L18 T18 | I | Receive Differential Tip Input RTIP is the positive differential input from the line interface. Along with the RRING signal, these pins should be coupled to a 1:1 transformer for proper operation. |
| RRING0 RRING1 RRING2 RRING3 RRING4 RRING5 RRING6 RRING7 | D1 F1 F18 D18 T1 M1 M18 R18 | I | Receive Differential Ring Input RRING is the negative differential input from the line interface. Along with the RTIP signal, these pins should be coupled to a 1:1 transformer for proper operation. |
| RXMUTE | T12 | I | Receive Data Muting <u>Hardware Mode Only</u> This pin is AND-ed with each of the RLOS functions on a per channel basis. Therefore, if this pin is pulled "High" and a given channel experiences a loss of signal, then the RPOS/RNEG output pins are automatically pulled "Low" to prevent data chattering. To disable this feature, the RxMUTE pin must be pulled "Low". NOTE: This pin is internally pulled "High" with a 50kΩ resistor |

The product (components) mentioned in this data sheet may no longer be ordered (OBS)

8-CHANNEL T1/E1/J1 SHORT-HAUL LINE INTERFACE UNIT

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|------------------|------------|------|---|
| RXRES1 RXRES0 | R10 V10 | I | <p>Receive External Resistor Control Pins <u>Hardware mode Only</u></p> <p>These pins are used in the Receive Internal Impedance mode for unique applications where an accurate resistor can be used to achieve optimal return loss. When RxRES[1:0] are used, the LIU automatically sets the internal impedance to match the line build out. For example: if 240Ω is selected, the LIU chooses an internal impedance such that the parallel combination equals the impedance chosen by TERSEL[1:0].</p> <p>"00" = No External Fixed Resistor "01" = 240Ω "10" = 210Ω "11" = 150Ω</p> <p>NOTE: These pins are internally pulled "Low" with a 50kΩ resistor. This feature is available in Host mode by programming the appropriate channel register.</p> |
| RCLKE/ μPTS1 | J16 | I | <p>Receive Clock Edge <u>Hardware Mode</u></p> <p>This pin is used to select which edge of the recovered clock is used to update data to the receiver on the RPOS/RNEG outputs. By default, data is updated on the rising edge. To update data on the falling edge, this pin must be pulled "High".</p> <p><u>Host Mode</u></p> <p>μPTS[2:1] pins are used to select the type of microprocessor to be used for Host communication.</p> <p>"00" = 8051 Intel Asynchronous "01" = 68K Motorola Asynchronous "10" = x86 Intel Synchronous "11" = 860 Motorola Synchronous</p> <p>NOTE: This pin is internally pulled "Low" with a 50kΩ resistor.</p> |

The product(s) mentioned in this data sheet are no longer being manufactured (OBS)

TRANSMIT SECTION

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|--|--|------|---|
| TCLKE/ μ PTS2 | L15 | I | <p>Transmit Clock Edge</p> <p><u>Hardware Mode</u> This pin is used to select which edge of the transmit clock is used to sample data on the transmitter on the TPOS/TNEG inputs. By default, data is sampled on the falling edge. To sample data on the rising edge, this pin must be pulled "High".</p> <p><u>Host Mode</u> μPTS[2:1] pins are used to select the type of microprocessor to be used for Host communication. "00" = 8051 Intel Asynchronous "01" = 68K Motorola Asynchronous "10" = x86 Intel Synchronous "11" = 860 Motorola Synchronous NOTE: This pin is internally pulled "Low" with a 50kΩ resistor.</p> |
| TTIP0 TTIP1 TTIP2 TTIP3 TTIP4 TTIP5 TTIP6 TTIP7 | E3 G4 F17 C16 R2 N2 N16 P16 | O | <p>Transmit Differential Tip Output</p> <p>TTIP is the positive differential output to the line interface. Along with the TRING signal, these pins should be coupled to a 1:2 step up transformer for proper operation.</p> |
| TRING0 TRING1 TRING2 TRING3 TRING4 TRING5 TRING6 TRING7 | E2 F3 F15 E16 P2 N4 R15 P17 | O | <p>Transmit Differential Ring Output</p> <p>TRING is the negative differential output to the line interface. Along with the TTIP signal, these pins should be coupled to a 1:2 step up transformer for proper operation.</p> |
| TPOS0 TPOS1 TPOS2 TPOS3 TPOS4 TPOS5 TPOS6 TPOS7 | C5 A4 B14 D14 V4 U5 V15 T14 | I | <p>TPOS/TDATA Input</p> <p>Transmit digital input pin. In dual rail mode, this pin is the transmit positive data input. In single rail mode, this pin is the transmit non-return to zero (NRZ) data input. NOTE: Internally pulled "Low" with a 50KΩ resistor.</p> |
| TNEG0 TNEG1 TNEG2 TNEG3 TNEG4 TNEG5 TNEG6 TNEG7 | C4 B5 D13 B15 U4 V5 U14 R14 | I | <p>Transmitter Negative NRZ Data Input</p> <p>In dual rail mode, this signal is the negative-rail input data for the transmitter. In single rail mode, this pin can be left unconnected while in Host mode. However, in Hardware mode, this pin is used to select the type of encoding/decoding for the E1/T1 data format. Connecting this pin "Low" enables HDB3 in E1 or B8ZS in T1. Connecting this pin "High" selects AMI data format. NOTE: Internally pulled "Low" with a 50kΩ resistor.</p> |

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|--|--|------|---|
| TCLK0 TCLK1 TCLK2 TCLK3 TCLK4 TCLK5 TCLK6 TCLK7 | B4 A3 A15 C14 T3 T5 V16 U15 | I | <p>Transmit Clock Input</p> <p>TCLK is the input facility clock used to sample the incoming TPOS/TNEG data. If TCLK is absent, pulled "Low", or pulled "High", the transmitter outputs at TTIP/TRING sends an all zero signal to the line. TPOS/TNEG data can be sampled on either edge of TCLK selected by TCLKE.</p> <p>NOTE: <i>TCLKE is a global setting that applies to all 8 channels.</i></p> |
| TAOS0 TAOS1 TAOS2 TAOS3 TAOS4 TAOS5 TAOS6 TAOS7 | D6 B6 A5 C6 T6 U6 V6 R6 | I | <p>Transmit All Ones for Channel</p> <p><u>Hardware Mode Only</u></p> <p>Setting this pin "High" enables the transmission of an all ones pattern to the line from TTIP/TRING. If this pin is pulled "Low", the transmitters operate in normal throughput mode.</p> <p>NOTE: <i>Internally pulled "Low" with a 50kΩ resistor for all channels. This feature is available in Host mode by programming the appropriate channel register.</i></p> |
| TXON0 TXON1 TXON2 TXON3 TXON4 TXON5 TXON6 TXON7 | A13 D12 C12 B12 V13 U13 R12 R13 | I | <p>Transmit On/Off Input</p> <p>Upon power up, the transmitters are powered off. Turning the transmitters On or Off is selected through the microprocessor interface by programming the appropriate channel register while in Host mode. However, if TxONCNTL is set "High" in the appropriate global register or if in Hardware mode, the activity of the transmitter outputs is controlled by the TxON pins.</p> <p>NOTE: <i>TxON is ideal for redundancy applications. See the Redundancy Applications Section of this datasheet for more details. Internally pulled "Low" with a 50KΩ resistor.</i></p> |

The Product (or Products) mentioned in this data sheet and/or not being manufactured (OBS)

MICROPROCESSOR INTERFACE

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|-------------------------|------------|------|---|
| HW/HOST | T10 | I | Mode Control Input This pin is used to select Host mode or Hardware mode. By default, the LIU is set in Hardware mode. To use Host mode, this pin must be pulled "Low". <i>NOTE: Internally pulled "High" with a 50kΩ resistor.</i> |
| WR _{R/W} /EQC0 | D7 | I | Write Input(R/W)/Equalizer Control Signal 0 <u>Host Mode</u> This pin is used to communicate a Read or Write operation according to the which microprocessor is chosen. See the Microprocessor Section of this datasheet for details. <u>Hardware Mode</u> EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See Table 22 for more details. <i>NOTE: Internally pulled "Low" with a 50kΩ resistor.</i> |
| RD _{DS} /EQC1 | C7 | I | Read Input (Data Strobe)/Equalizer Control Signal 1 <u>Host Mode</u> This pin is used to communicate a Read or Write operation according to the which microprocessor is chosen. See the Microprocessor Section of this datasheet for details. <u>Hardware Mode</u> EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See Table 22 for more details. <i>NOTE: Internally pulled "Low" with a 50kΩ resistor.</i> |
| ALE/EQC2 | A7 | I | Address Latch Input (Address Strobe) <u>Host Mode</u> This pin is used to latch the address contents into the internal registers within the LIU device. See the Microprocessor Section of this datasheet for details. <u>Hardware Mode</u> EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See Table 22 for more details. <i>NOTE: Internally pulled "Low" with a 50kΩ resistor.</i> |
| CS _{CS} /EQC3 | B7 | I | Chip Select Input - Host mode: <u>Host Mode</u> This pin is used to initiate communication with the microprocessor interface. See the Microprocessor Section of this datasheet for details. <u>Hardware Mode</u> EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See Table 22 for more details. <i>NOTE: Internally pulled "Low" with a 50kΩ resistor.</i> |

8-CHANNEL T1/E1/J1 SHORT-HAUL LINE INTERFACE UNIT

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|--|--|------|---|
| $\overline{\text{RDY}}/\text{EQC4}$ | A6 | I/O | <p>Ready Output (Data Transfer Acknowledge)</p> <p><u>Host Mode (Parallel Microprocessor)</u> If Pin SER_PAR is pulled "Low", this output pin from the microprocessor block is used to inform the local μP that the Read or Write operation has been completed and is waiting for the next command. See the Microprocessor Section of this datasheet for details.</p> <p><u>Host Mode (Serial Interface)</u> If Pin SER_PAR is pulled "High", this output pin from the serial interface is used to read back the register contents. See the Microprocessor Section of this datasheet for details.</p> <p><u>Hardware Mode</u> EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See Table 22 for more details. NOTE: Internally pulled "Low" with a 50kΩ resistor.</p> |
| D[7]/Loop14 D[6]/Loop04 D[5]/Loop15 D[4]/Loop05 D[3]/Loop16 D[2]/Loop06 D[1]/Loop17 D[0]/Loop07 | T7 U7 V7 V8 V9 U8 U9 R7 | I/O | <p>Bi-Directional Data Bus/Loopback Mode Select</p> <p><u>Host Mode</u> These pins are used for the 8-bit bi-directional data bus to allow data transfer to and from the microprocessor interface.</p> <p><u>Hardware Mode (Channels 4 through 7)</u> These pins are used to select the loopback mode. Each channel has two loopback pins Loop[1:0]. "00" = No Loopback "01" = Analog Local Loopback "10" = Remote Loopback "11" = Digital Loopback NOTE: Internally pulled "Low" with a 50kΩ resistor.</p> |
| A[7]/Loop13 A[6]/Loop03 A[5]/Loop12 A[4]/Loop02 A[3]/Loop11 A[2]/Loop01 A[1]/Loop10 A[0]/Loop00 | A12 B11 C11 D11 A11 B10 A10 C10 | I | <p>Direct Address Bus/Loopback Mode Select</p> <p><u>Host Mode</u> These pins are used for the 8-bit direct address bus to allow access to the internal registers within the microprocessor interface.</p> <p><u>Hardware Mode (Channels 0 through 3)</u> These pins are used to select the loopback mode. Each channel has two loopback pins Loop[1:0]. "00" = No Loopback "01" = Analog Local Loopback "10" = Remote Loopback "11" = Digital Loopback NOTE: Internally pulled "Low" with a 50kΩ resistor.</p> |

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|-------------------------|------------|------|--|
| μ PCLK/ATAOS | T13 | I | <p>Synchronous Microprocessor Clock/Automatic Transmit All Ones Host Mode</p> <p>This synchronous input clock is used as the internal master clock to the microprocessor interface when configured for in a synchronous mode.</p> <p><u>Hardware Mode</u></p> <p>This pin is used select an all ones signal to the line interface through TTIP/TRING any time that a loss of signal occurs. This feature is available in Host mode by programming the appropriate global register.</p> <p>NOTE: Internally pulled "Low" with a 50kΩ resistor.</p> |
| $\overline{\text{INT}}$ | L16 | O | <p>Interrupt Output/Turns Ratio Select (External Impedance Mode)</p> <p><u>Host Mode</u></p> <p>This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". GIE (Global Interrupt Enable) must be set "High" in the appropriate global register to enable interrupt generation.</p> <p>NOTES:</p> <ol style="list-style-type: none"> This pin is an open-drain output that requires an external 10KΩ pull-up resistor. Internally pulled "Low" with a 50kΩ resistor. |

JITTER ATTENUATOR

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|------------|----------|--|--------|--------|---------|-----------|--|-----------|----|----|---|---|----------|-------|-------|-------|---|---|----------|---|----|-------|---|---|---------|---|----|-------|---|---|---------|---|-----|-------|
| JASEL0 JASEL1 | A14 B13 | I | <p>Jitter Attenuator Select Pins Hardware Mode</p> <p>JASEL[1:0] pins are used to place the jitter attenuator in the transmit path, the receive path or to disable it.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">JASEL1</th> <th rowspan="2">JASEL0</th> <th rowspan="2">JA Path</th> <th colspan="2">JA BW Hz</th> <th rowspan="2">FIFO Size</th> </tr> <tr> <th>T1</th> <th>E1</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Disabled</td> <td>-----</td> <td>-----</td> <td>-----</td> </tr> <tr> <td>0</td> <td>1</td> <td>Transmit</td> <td>3</td> <td>10</td> <td>32/32</td> </tr> <tr> <td>1</td> <td>0</td> <td>Receive</td> <td>3</td> <td>10</td> <td>32/32</td> </tr> <tr> <td>1</td> <td>1</td> <td>Receive</td> <td>3</td> <td>1.5</td> <td>64/64</td> </tr> </tbody> </table> <p>NOTE: These pins are internally pulled "Low" with 50kΩ resistors.</p> | JASEL1 | JASEL0 | JA Path | JA BW Hz | | FIFO Size | T1 | E1 | 0 | 0 | Disabled | ----- | ----- | ----- | 0 | 1 | Transmit | 3 | 10 | 32/32 | 1 | 0 | Receive | 3 | 10 | 32/32 | 1 | 1 | Receive | 3 | 1.5 | 64/64 |
| JASEL1 | JASEL0 | JA Path | JA BW Hz | | | | FIFO Size | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | T1 | E1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Disabled | ----- | ----- | ----- | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Transmit | 3 | 10 | 32/32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Receive | 3 | 10 | 32/32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Receive | 3 | 1.5 | 64/64 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

CLOCK SYNTHESIZER

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|-------------|------------|------|--|
| MCLKOUT | H1 | O | <p>Synthesized Master Clock Output</p> <p>This signal is the output of the Master Clock Synthesizer PLL which is at T1 or E1 rate based upon the mode of operation.</p> |

8-CHANNEL T1/E1/J1 SHORT-HAUL LINE INTERFACE UNIT

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------------|----------------|---------|--|------------|------------|-------------|---------|---------|----------|-------------|------|------|---|---|---|---|------|------|------|---|---|---|---|------|------|------|---|---|---|---|------|------|------|---|---|---|---|------|------|------|---|---|---|---|------|------|------|---|---|---|---|------|---|---|---|---|---|---|------|---|---|---|---|---|---|------|----|---|---|---|---|---|------|----|---|---|---|---|---|------|----|---|---|---|---|---|------|----|---|---|---|---|---|------|----|---|---|---|---|---|------|----|---|---|---|---|---|------|-----|---|---|---|---|---|------|-----|---|---|---|---|---|------|-----|---|---|---|---|---|------|-----|---|---|---|---|---|------|
| MCLKT1 | K1 | I | <p>T1 Master Clock Input</p> <p>This signal is an independent 1.544MHz clock for T1 systems with accuracy better than ±50ppm and duty cycle within 40% to 60%. MCLKT1 is used in the T1 mode.</p> <p><i>NOTE: All channels must operate at the same clock rate, either T1, E1 or J1. This pin is internally pulled "Low" with a 50kΩ resistor.</i></p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MCLKE1 | J1 | I | <p>E1 Master Clock Input</p> <p>A 2.048MHz clock for with an accuracy of better than ±50ppm and a duty cycle of 40% to 60% can be provided at this pin. In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation.</p> <p><i>NOTE: All channels of the XRT83SH38 must be operated at the same clock rate, either T1, E1 or J1. This pin is internally pulled "Low" with a 50kΩ resistor.</i></p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CLKSEL0 CLKSEL1 CLKSEL2 | A8 B8 C8 | I | <p>Clock Select inputs for Master Clock Synthesizer</p> <p><u>Hardware Mode Only</u></p> <p>CLKSEL[2:0] are input signals to a programmable frequency synthesizer that can be used to generate a master clock from an external accurate clock source according to the table below. MCLKRATE is automatically generated from the state of the EQC[4:0] pins.</p> <table border="1"> <thead> <tr> <th>MCLKE1 kHz</th> <th>MCLKT1 kHz</th> <th>CLKSEL2</th> <th>CLKSEL1</th> <th>CLKSEL0</th> <th>MCLKRATE</th> <th>CLKOUT/ kHz</th> </tr> </thead> <tbody> <tr><td>2048</td><td>2048</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2048</td></tr> <tr><td>2048</td><td>2048</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1544</td></tr> <tr><td>2048</td><td>1544</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2048</td></tr> <tr><td>1544</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1544</td></tr> <tr><td>1544</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2048</td></tr> <tr><td>2048</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1544</td></tr> <tr><td>8</td><td>X</td><td>0</td><td>1</td><td>0</td><td>0</td><td>2048</td></tr> <tr><td>8</td><td>X</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1544</td></tr> <tr><td>16</td><td>X</td><td>0</td><td>1</td><td>1</td><td>0</td><td>2048</td></tr> <tr><td>16</td><td>X</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1544</td></tr> <tr><td>56</td><td>X</td><td>1</td><td>0</td><td>0</td><td>0</td><td>2048</td></tr> <tr><td>56</td><td>X</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1544</td></tr> <tr><td>64</td><td>X</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2048</td></tr> <tr><td>64</td><td>X</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1544</td></tr> <tr><td>128</td><td>X</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2048</td></tr> <tr><td>128</td><td>X</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1544</td></tr> <tr><td>256</td><td>X</td><td>1</td><td>1</td><td>1</td><td>0</td><td>2048</td></tr> <tr><td>256</td><td>X</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1544</td></tr> </tbody> </table> <p><i>NOTE: These pins are internally pulled "Low" with a 50kΩ resistor.</i></p> | MCLKE1 kHz | MCLKT1 kHz | CLKSEL2 | CLKSEL1 | CLKSEL0 | MCLKRATE | CLKOUT/ kHz | 2048 | 2048 | 0 | 0 | 0 | 0 | 2048 | 2048 | 2048 | 0 | 0 | 0 | 1 | 1544 | 2048 | 1544 | 0 | 0 | 0 | 0 | 2048 | 1544 | 1544 | 0 | 0 | 1 | 1 | 1544 | 1544 | 1544 | 0 | 0 | 1 | 0 | 2048 | 2048 | 1544 | 0 | 0 | 1 | 1 | 1544 | 8 | X | 0 | 1 | 0 | 0 | 2048 | 8 | X | 0 | 1 | 0 | 1 | 1544 | 16 | X | 0 | 1 | 1 | 0 | 2048 | 16 | X | 0 | 1 | 1 | 1 | 1544 | 56 | X | 1 | 0 | 0 | 0 | 2048 | 56 | X | 1 | 0 | 0 | 1 | 1544 | 64 | X | 1 | 0 | 1 | 0 | 2048 | 64 | X | 1 | 0 | 1 | 1 | 1544 | 128 | X | 1 | 1 | 0 | 0 | 2048 | 128 | X | 1 | 1 | 0 | 1 | 1544 | 256 | X | 1 | 1 | 1 | 0 | 2048 | 256 | X | 1 | 1 | 1 | 1 | 1544 |
| MCLKE1 kHz | MCLKT1 kHz | CLKSEL2 | CLKSEL1 | CLKSEL0 | MCLKRATE | CLKOUT/ kHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2048 | 2048 | 0 | 0 | 0 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2048 | 2048 | 0 | 0 | 0 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2048 | 1544 | 0 | 0 | 0 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1544 | 1544 | 0 | 0 | 1 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1544 | 1544 | 0 | 0 | 1 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2048 | 1544 | 0 | 0 | 1 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | X | 0 | 1 | 0 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | X | 0 | 1 | 0 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 16 | X | 0 | 1 | 1 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 16 | X | 0 | 1 | 1 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 56 | X | 1 | 0 | 0 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 56 | X | 1 | 0 | 0 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 64 | X | 1 | 0 | 1 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 64 | X | 1 | 0 | 1 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 128 | X | 1 | 1 | 0 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 128 | X | 1 | 1 | 0 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 256 | X | 1 | 1 | 1 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 256 | X | 1 | 1 | 1 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

ALARM FUNCTIONS/REDUNDANCY SUPPORT

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|--|--|------|--|
| GAUGE | J18 | I | Twisted Pair Cable Wire Gauge Select <u>Hardware Mode Only</u> This pin is used to match the frequency characteristics according to the gauge of wire used in Telecom circuits. By default, the LIU is matched to 22 gauge or 24 gauge wire. To select 26 gauge, this pin must be pulled "High". <i>NOTE: Internally pulled "Low" with a 50kΩ resistor.</i> |
| DMO0 DMO1 DMO2 DMO3 DMO4 DMO5 DMO6 DMO7 | D5 D4 C15 C13 R5 P4 U17 V14 | O | Digital Monitor Output When no transmit output pulse is detected for more than 128 TCLK cycles within the transmit output buffer, the DMO pin will go "High" for a minimum of one TCLK cycle. DMO will remain "High" until the transmitter sends a valid pulse. <i>NOTE: This pin can be used for redundancy applications to initiate an automatic switch to a backup card.</i> |
| $\overline{\text{RESET}}$ | T8 | I | Hardware Reset Input Active low signal. When this pin is pulled "Low" for more than 10μS, the internal registers are set to their default state. See the register description for the default values. <i>NOTE: Internally pulled "High" with a 50KΩ resistor.</i> |
| $\overline{\text{SR/DR}}$ | K4 | I | Single-Rail/Dual-Rail Data Format <u>Hardware Mode Only</u> This pin is used to control the data format on the facility side of the LIU to interface to a Framer or Mapper/ASIC device. By default, dual rail mode is selected which relies upon the Framer to handle the encoding/decoding functions. To select single rail mode, this pin must be pulled "High". If single rail mode is selected, the LIU can encode/decode AMI or B8ZS/HDB3 data formats. <i>NOTE: Internally pulled "Low" with a 50kΩ resistor.</i> |
| RXTSEL | U11 | I | Receiver Termination Select <u>Hardware Mode</u> This pin is used to select between the internal and external impedance modes for the receive path. By default, the receivers are configured for external impedance mode, which is ideal for redundancy applications without relays. To select internal impedance, this pin must be pulled "High". <u>Host Mode</u> Internal/External impedance can be selected by programming the appropriate channel registers. However, to assist in redundancy applications, this pin can be used for a hard switch if the RxTCNTL bit is set "High" in the appropriate global register. If RxTCNTL is set "High", the individual RXTSEL register bits are ignored. <i>NOTE: This pin is internally pulled "Low" with a 50kΩ resistor.</i> |
| TXTSEL | V11 | I | Transmitter Termination Select <u>Hardware Mode</u> This pin is used to select between the internal and external impedance modes for the transmit path. By default, the receivers are configured for external impedance mode, which is ideal for redundancy applications without relays. To select internal impedance, this pin must be pulled "High". <i>NOTE: This pin is internally pulled "Low".</i> |

8-CHANNEL T1/E1/J1 SHORT-HAUL LINE INTERFACE UNIT

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|-------------------------|------------|------|--|
| TERSEL1 TERSEL0 | T11 R11 | I | <p>Termination Impedance Select <u>Hardware Mode Only</u></p> <p>These pins are used to select the transmitter and receiver impedance. By default, the impedance is set to 100Ω.</p> <p>"00" = 100Ω "01" = 110Ω "10" = 75Ω "11" = 120Ω</p> <p><i>NOTE: These pins are internally pulled "Low" with a 50kΩ resistor.</i></p> |
| TEST | U12 | I | <p>Factory Test Mode</p> <p>For normal operation, the TEST pin should be tied to ground.</p> <p><i>NOTE: Internally pulled "Low" with a 50kΩ resistor.</i></p> |
| $\overline{\text{ICT}}$ | V12 | I | <p>In Circuit Testing</p> <p>When this pin is tied "Low", all output pins are forced to "High" impedance for in circuit testing.</p> <p><i>NOTE: Internally pulled "High" with a 50kΩ resistor.</i></p> |

The Product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

SERIAL PORT AND JTAG

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|---------------------|--------------------------------------|------|---|
| SER_PAR | P18 | I | <p>Serial/Parallel Select Input (Host Mode Only)</p> <p>This pin is used in the Host mode to select between the parallel microprocessor or serial interface. By default, the Host mode operates in the parallel microprocessor mode. To configure the device for a serial interface, this pin must be pulled "High".</p> <p><i>NOTE: Internally pulled "Low" with a 50kΩ resistor.</i></p> |
| SCLK | T13 | I | <p>Serial Clock Input (Host Mode Only)</p> <p>If Pin SER_PAR is pulled "High", this input pin is used the timing reference for the serial microprocessor interface. See the Microprocessor Section of this datasheet for details.</p> |
| SDI | C10 | I | <p>Serial Data Input (Host Mode Only)</p> <p>If Pin SER_PAR is pulled "High", this input pin from the serial interface is used to input the serial data for Read and Write operations. See the Microprocessor Section of this datasheet for details.</p> |
| SDO | R7 | O | <p>Serial Data Output (Host Mode Only)</p> <p>If Pin SER_PAR is pulled "High", this output pin from the serial interface is used to read back the register contents. See the Microprocessor Section of this datasheet for details.</p> |
| JTAGtip JTAGring | E18 B18 | | <p>Analog JTAG Positive Pin Analog JTAG Negative Pin</p> |
| TDO | B1 | | <p>Test Data Out</p> <p>This pin is used as the output data pin for the boundary scan chain.</p> |
| TDI | R1 | | <p>Test Data In</p> <p>This pin is used as the input data pin for the boundary scan chain.</p> |
| TCK | N1 | | <p>Test Clock Input</p> <p>This pin is used as the input clock source for the boundary scan chain.</p> |
| TMS | E1 | | <p>Test Mode Select</p> <p>This pin is used as the input mode select for the boundary scan chain.</p> |
| NC | A1 A18 N18 P18 V1 V18 | **** | <p>No Connect Pins</p> |

POWER AND GROUND

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|--|--|------|--|
| TGND0 TGND1 TGND2 TGND3 TGND4 TGND5 TGND6 TGND7 | D3 F2 E15 C17 R3 P3 T16 R16 | **** | Transmitter Analog Ground It's recommended that all ground pins of this device be tied together. |
| TVDD0 TVDD1 TVDD2 TVDD3 TVDD4 TVDD5 TVDD6 TVDD7 | E4 F4 F16 E17 R4 P1 N15 P15 | **** | Transmit Analog Power Supply (3.3V ±5%) TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1µF capacitor. |
| RVDD0 RVDD1 RVDD2 RVDD3 RVDD4 RVDD5 RVDD6 RVDD7 | C2 E5 G16 D16 V2 N3 N17 U18 | **** | Receive Analog Power Supply (3.3V ±5%) RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1µF capacitor. |
| RGND0 RGND1 RGND2 RGND3 RGND4 RGND5 RGND6 RGND7 | D2 G3 G17 D17 T2 M2 M17 R17 | **** | Receiver Analog Ground It's recommended that all ground pins of this device be tied together. |
| AVDD | K17 J3 J2 | **** | Analog Power Supply (3.3V ±5%) AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1µF capacitor. |
| AGND | J17 K3 L4 | **** | Analog Ground It's recommended that all ground pins of this device be tied together. |

| SIGNAL NAME | BGA LEAD # | TYPE | DESCRIPTION |
|-------------|--|------|---|
| DVDD | R9 U10 K18 D9 D10 K15 A9 J4 | **** | Digital Power Supply (3.3V ±5%) DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1µF capacitor. |
| DGND | R8 T9 H17 B9 D8 C9 G15 K2 | **** | Digital Ground It's recommended that all ground pins of this device be tied together. |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FUNCTIONAL DESCRIPTION

The XRT83SH38 is a fully integrated 8-channel short-haul line interface unit (LIU) that operates from a single 3.3V power supply. Using internal termination, the LIU provides one bill of materials to operate in T1, E1, or J1 mode with minimum external components. The LIU features are programmed through a standard microprocessor interface or controlled through Hardware mode. EXAR’s LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays. The on-chip clock synthesizer generates T1/E1/J1 clock rates from a selectable external clock frequency and outputs a clock reference of the line rate chosen. Additional features include RLOS, a 16-bit LCV counter for each channel, AIS, QRSS generation/detection, Network Loop Code generation/detection, TAOS, DMO, and diagnostic loopback modes.

1.0 HARDWARE MODE VS HOST MODE

The LIU supports a parallel or (serial) microprocessor interface (Host mode) for programming the internal features, or a Hardware mode that can be used to configure the device.

1.1 Feature Differences in Hardware Mode

Some features within the Hardware mode are not supported on a per channel basis. The differences between Hardware mode and Host mode are described below in **Table 1**.

TABLE 1: DIFFERENCES BETWEEN HARDWARE MODE AND HOST MODE

| FEATURE | HOST MODE | HARDWARE MODE |
|------------------|-----------------|--|
| Tx Test Patterns | Fully Supported | QRSS diagnostic patterns are not available in Hardware mode. The TAOS feature is available. |
| RxRES[1:0] | Per Channel | In Hardware mode, RxRES[1:0] is a global setting that applies to all channels. |
| TERSEL[1:0] | Per Channel | In Hardware mode, TERSEL[1:0] is a global setting that applies to all channels. |
| EQC[4:0] | Per Channel | In Hardware mode, the EQC[4:0] is a global setting that applies to all channels. <i>NOTE: In Host mode, all channels have to operate at one line rate T1 or E1, however each channel can have an individual line build out.</i> |
| Dual Loopback | Fully Supported | In Hardware mode, dual loopback mode is not supported. Remote, Analog local, and digital loopback modes are available. |
| JASEL[1:0] | Per Channel | In Hardware mode, the jitter attenuator selection is a global setting that applies to all channels. |
| RxTSEL | Per Channel | In Hardware mode, the receive termination select is a global setting that applies to all channels. |
| TxTSEL | Per Channel | In Hardware mode, the transmit termination select is a global setting that applies to all channels. |

2.0 MASTER CLOCK GENERATOR

Using a variety of external clock sources, the on-chip frequency synthesizer generates the T1 (1.544MHz) or E1 (2.048MHz) master clocks necessary for the transmit pulse shaping and receive clock recovery circuit. There are two master clock inputs MCLKE1 and MCLKT1. In systems where both T1 and E1 master clocks are available these clocks can be connected to the respective pins. All channels of a given XRT83SH38 must be operated at the same clock rate, either T1, E1 or J1 modes. In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation. T1 or E1 master clocks can be generated from 8kHz, 16kHz, 56kHz, 64kHz, 128kHz and 256kHz external clocks under the control of CLKSEL[2:0] inputs according to EQC[4:0] determine the T1/E1 operating mode. See for details.

FIGURE 3. TWO INPUT CLOCK SOURCE

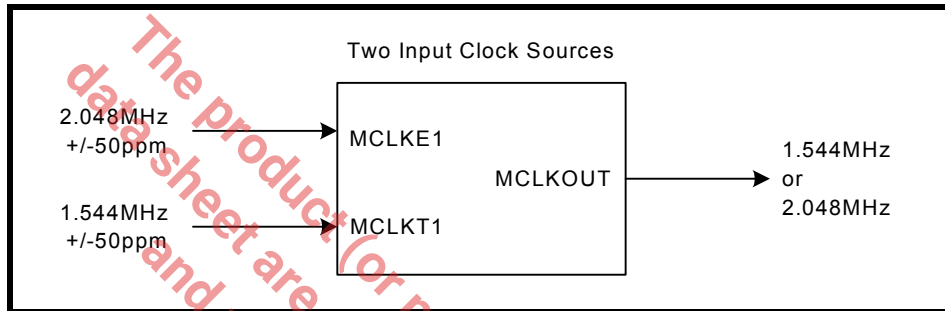


FIGURE 4. ONE INPUT CLOCK SOURCE

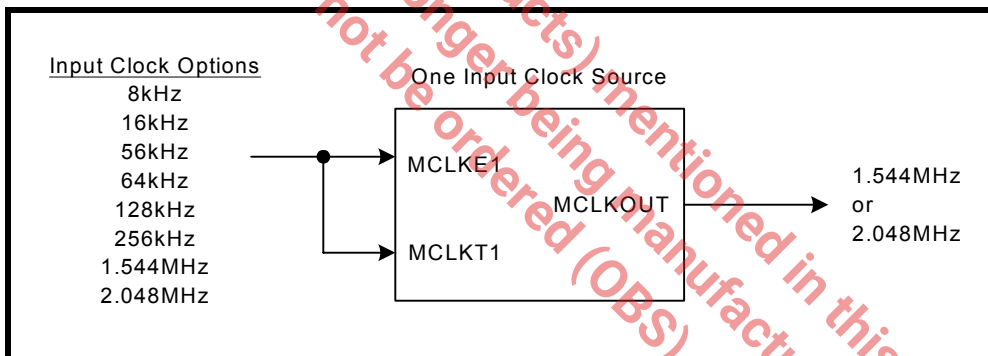


TABLE 2: MASTER CLOCK GENERATOR

| MCLKE1 kHz | MCLKT1 kHz | CLKSEL2 | CLKSEL1 | CLKSEL0 | MCLKRATE | MASTER CLOCK kHz |
|---------------|---------------|---------|---------|---------|----------|---------------------|
| 2048 | 2048 | 0 | 0 | 0 | 0 | 2048 |
| 2048 | 2048 | 0 | 0 | 0 | 1 | 1544 |
| 2048 | 1544 | 0 | 0 | 0 | 0 | 2048 |
| 1544 | 1544 | 0 | 0 | 1 | 1 | 1544 |
| 1544 | 1544 | 0 | 0 | 1 | 0 | 2048 |
| 2048 | 1544 | 0 | 0 | 1 | 1 | 1544 |
| 8 | x | 0 | 1 | 0 | 0 | 2048 |
| 8 | x | 0 | 1 | 0 | 1 | 1544 |

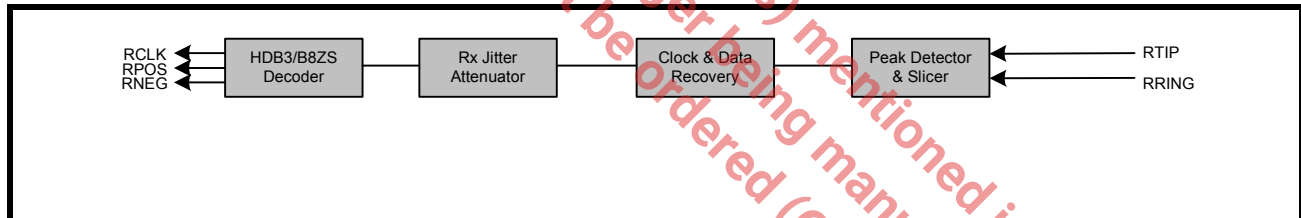
TABLE 2: MASTER CLOCK GENERATOR

| MCLKE1 kHz | MCLKT1 kHz | CLKSEL2 | CLKSEL1 | CLKSEL0 | MCLKRATE | MASTER CLOCK kHz |
|---------------|---------------|---------|---------|---------|----------|---------------------|
| 16 | x | 0 | 1 | 1 | 0 | 2048 |
| 16 | x | 0 | 1 | 1 | 1 | 1544 |
| 56 | x | 1 | 0 | 0 | 0 | 2048 |
| 56 | x | 1 | 0 | 0 | 1 | 1544 |
| 64 | x | 1 | 0 | 1 | 0 | 2048 |
| 64 | x | 1 | 0 | 1 | 1 | 1544 |
| 128 | x | 1 | 1 | 0 | 0 | 2048 |
| 128 | x | 1 | 1 | 0 | 1 | 1544 |
| 256 | x | 1 | 1 | 1 | 0 | 2048 |
| 256 | x | 1 | 1 | 1 | 1 | 1544 |

3.0 RECEIVE PATH LINE INTERFACE

The receive path of the XRT83SH38 LIU consists of 8 independent T1/E1/J1 receivers. The following section describes the complete receive path from RTIP/RRING inputs to RCLK/RPOS/RNEG outputs. A simplified block diagram of the receive path is shown in Figure 5.

FIGURE 5. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH



3.1 Line Termination (RTIP/RRING)

3.1.1 CASE 1: Internal Termination

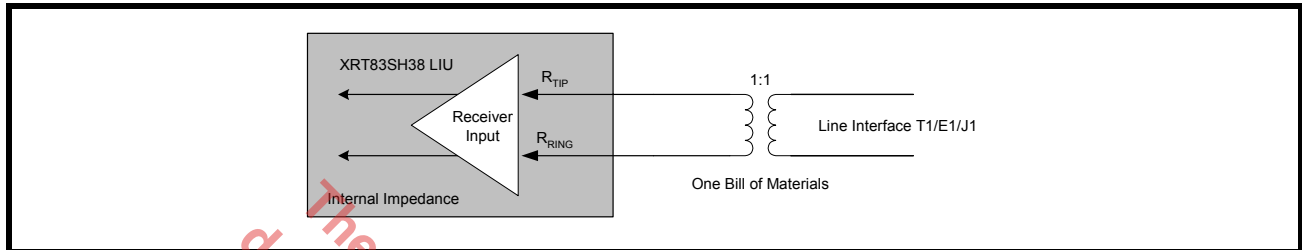
The input stage of the receive path accepts standard T1/E1/J1 twisted pair or E1 coaxial cable inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The receive termination impedance is selected by programming TERSEL[1:0] to match the line impedance. Selecting the internal impedance is shown in Table 3.

TABLE 3: SELECTING THE INTERNAL IMPEDANCE

| TERSEL[1:0] | RECEIVE TERMINATION |
|-------------|---------------------|
| 0h (00) | 100Ω |
| 1h (01) | 110Ω |
| 2h (10) | 75Ω |
| 3h (11) | 120Ω |

The XRT83SH38 has the ability to switch the internal termination to "High" impedance by programming RxTSEL in the appropriate channel register. For internal termination, set RxTSEL to "1". By default, RxTSEL is set to "0" ("High" impedance). For redundancy applications, a dedicated hardware pin (RxTSEL) is also available to control the receive termination for all channels simultaneously. This hardware pin takes priority over the register setting if RxTCNTL is set to "1" in the appropriate global register. If RxTCNTL is set to "0", the state of this pin is ignored. See **Figure 6** for a typical connection diagram using the internal termination.

FIGURE 6. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



3.1.2 CASE 2: Internal Termination With One External Fixed Resistor for All Modes

Along with the internal termination, a high precision external fixed resistor can be used to optimize the return loss. This external resistor can be used for all modes of operation ensuring one bill of materials. There are three resistor values that can be used by setting the RxRES[1:0] bits in the appropriate channel register. Selecting the value for the external fixed resistor is shown in **Table 4**.

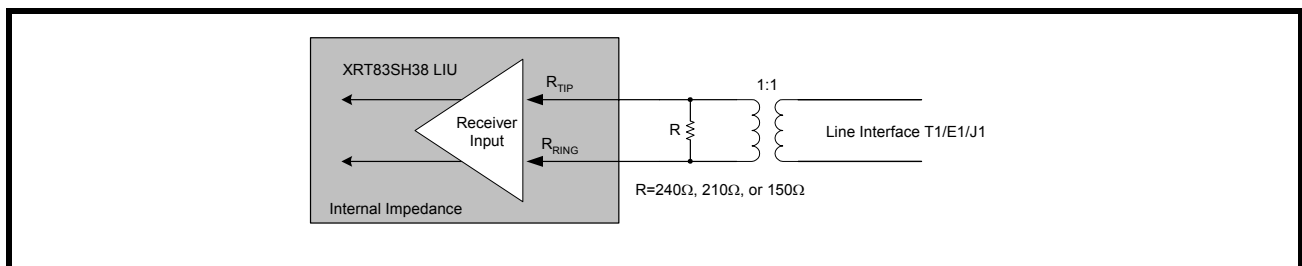
TABLE 4: SELECTING THE VALUE OF THE EXTERNAL FIXED RESISTOR

| RxRES[1:0] | EXTERNAL FIXED RESISTOR |
|------------|-------------------------|
| 0h (00) | None |
| 1h (01) | 240Ω |
| 2h (10) | 210Ω |
| 3h (11) | 150Ω |

By default, RxRES[1:0] is set to "None" for no external fixed resistor. If an external fixed resistor is used, the XRT83SH38 uses the parallel combination of the external fixed resistor and the internal termination as the input impedance. See **Figure 7** for a typical connection diagram using the external fixed resistor.

NOTE: Without the external resistor, the XRT83SH38 meets all return loss specifications. This mode was created to add flexibility for optimizing return loss by using a high precision external resistor.

FIGURE 7. TYPICAL CONNECTION DIAGRAM USING ONE EXTERNAL FIXED RESISTOR



3.2 Clock and Data Recovery

The receive clock (RCLK) is recovered by the clock and data recovery circuitry. An internal PLL locks on the incoming data stream and outputs a clock that's in phase with the incoming signal. This allows for multi-channel T1/E1/J1 signals to arrive from different timing sources and remain independent. In the absence of an incoming signal, RCLK maintains its timing by using the internal master clock as its reference. The recovered

8-CHANNEL T1/E1/J1 SHORT-HAUL LINE INTERFACE UNIT

data can be updated on either edge of RCLK. By default, data is updated on the rising edge of RCLK. To update data on the falling edge of RCLK, set RCLKE to "1" in the appropriate global register. Figure 8 is a timing diagram of the receive data updated on the rising edge of RCLK. Figure 9 is a timing diagram of the receive data updated on the falling edge of RCLK. The timing specifications are shown in Table 5.

FIGURE 8. RECEIVE DATA UPDATED ON THE RISING EDGE OF RCLK

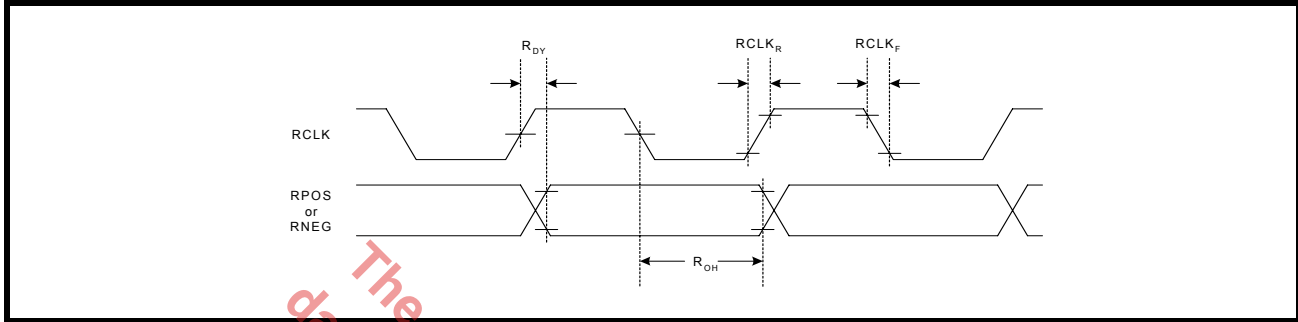


FIGURE 9. RECEIVE DATA UPDATED ON THE FALLING EDGE OF RCLK

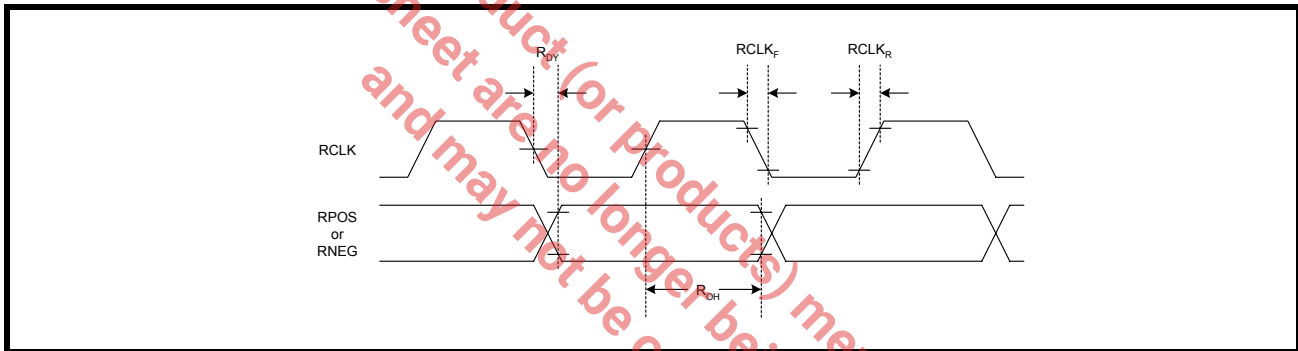


TABLE 5: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|-------------------|-----|-----|-----|-------|
| RCLK Duty Cycle | R _{CDU} | 45 | 50 | 55 | % |
| Receive Data Setup Time | R _{SU} | 150 | - | - | ns |
| Receive Data Hold Time | R _{HO} | 150 | - | - | ns |
| RCLK to Data Delay | R _{DY} | - | - | 40 | ns |
| RCLK Rise Time (10% to 90%) with 25pF Loading | RCLK _R | - | - | 40 | ns |
| RCLK Fall Time (90% to 10%) with 25pF Loading | RCLK _F | - | - | 40 | ns |

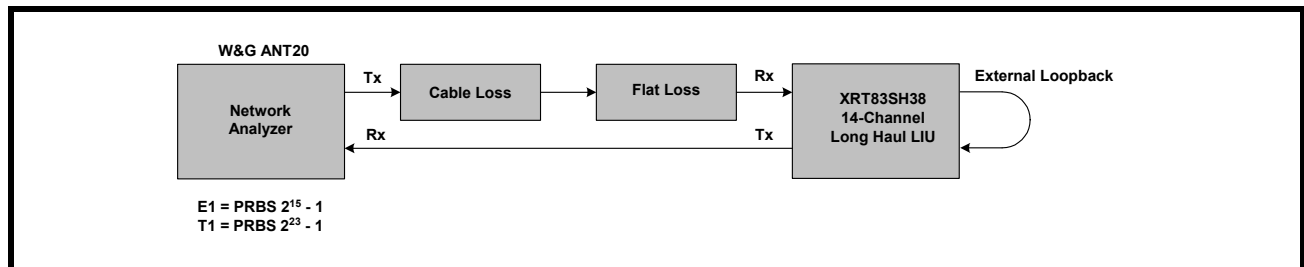
NOTE: VDD=3.3V ±5%, T_A=25°C, Unless Otherwise Specified

3.2.1 Receive Sensitivity

To meet short haul requirements, the XRT83SH38 can accept T1/E1/J1 signals that have been attenuated by 12dB of flat loss in E1 mode or by 655 feet of cable loss along with 6dB of flat loss in T1 mode. However, the XRT83SH38 can tolerate cable loss and flat loss beyond the industry specifications. The receive sensitivity in the short haul mode is approximately 4,000 feet without experiencing bit errors, LOF, pattern synchronization, etc. Although data integrity is maintained, the RLOS function (if enabled) will report an RLOS condition

according to the receiver loss of signal section in this datasheet. The test configuration for measuring the receive sensitivity is shown in **Figure 10**.

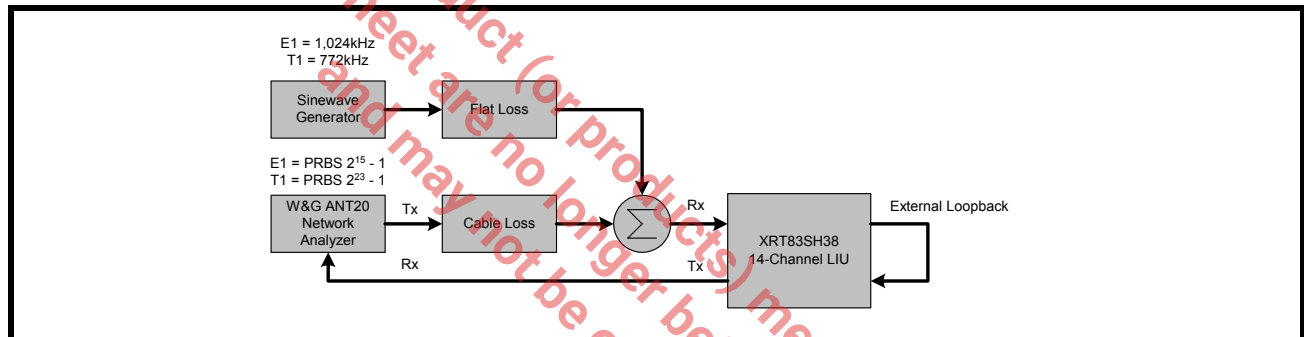
FIGURE 10. TEST CONFIGURATION FOR MEASURING RECEIVE SENSITIVITY



3.2.2 Interference Margin

The interference margin for the XRT83SH38 will be added when the first revision of silicon arrives. The test configuration for measuring the interference margin is shown in **Figure 11**.

FIGURE 11. TEST CONFIGURATION FOR MEASURING INTERFERENCE MARGIN



3.2.3 General Alarm Detection and Interrupt Generation

The receive path detects RLOS, AIS, QRPD and FLS. These alarms can be individually masked to prevent the alarm from triggering an interrupt. To enable interrupt generation, the Global Interrupt Enable (GIE) bit must be set "High" in the appropriate global register. Any time a change in status occurs (if the alarms are enabled), the interrupt pin will pull "Low" to indicate an alarm has occurred. Once the status registers have been read, the INT pin will return "High". The status registers are Reset Upon Read (RUR). The interrupts are categorized in a hierarchical process block. **Figure** is a simplified block diagram of the interrupt generation process.

NOTE: The interrupt pin is an open-drain output that requires a 10kΩ external pull-up resistor.

3.2.3.1 RLOS (Receiver Loss of Signal)

In T1 mode, RLOS is declared if an incoming signal has no transitions over a period of 175 +/-75 contiguous pulse intervals. However, the XRT83SH38 LIU has a built in analog RLOS so that the user can be notified when the amplitude of the incoming signal has been attenuated -9dB below the equalizer gain setting. For example: In T1 or E1 short haul mode, the equalizer gain setting is 15dB. Once the input reaches an amplitude of -24dB below nominal, the LIU will declare RLOS. The RLOS circuitry clears when the input reaches +3dB relative to where it was declared. This +3dB value is a pre-determined hysteresis so that transients will not cause the RLOS to clear. In E1 mode, RLOS is declared if an incoming signal has no transitions for N consecutive pulse intervals, where $10 \leq N \leq 255$. According to G.775, no transitions in E1 mode is defined between -9dB and -35dB below nominal. **Figure 12** is a simplified block diagram of the analog RLOS function. **Table 6** summarizes the analog RLOS values for the different equalizer gain settings.

FIGURE 12. ANALOG RECEIVE LOS OF SIGNAL FOR T1/E1/J1

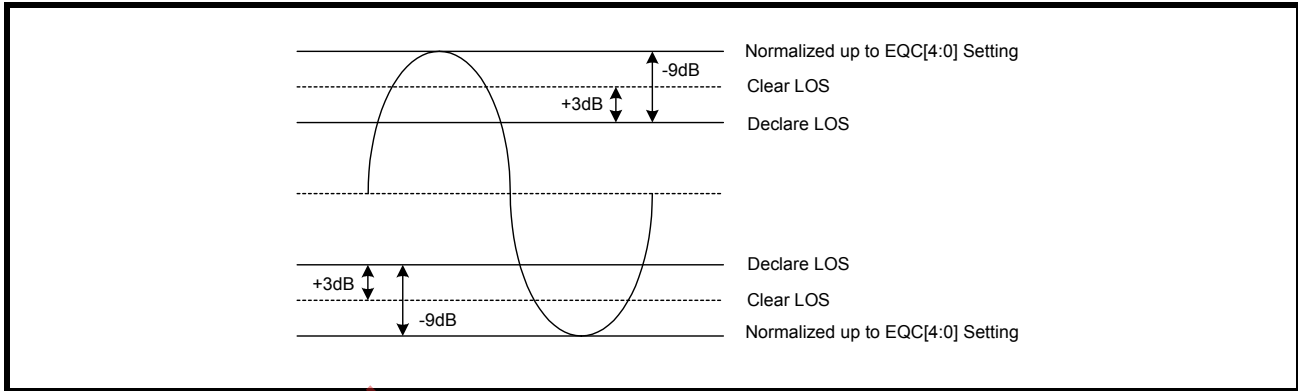


TABLE 6: ANALOG RLOS DECLARE/CLEAR (TYPICAL VALUES) FOR T1/E1

| GAIN SETTING | DECLARE | CLEAR |
|-----------------------------|---------|-------|
| 15dB (Short Haul Mode) | -24dB | -21dB |
| 29dB (Monitoring Gain Mode) | -38dB | -35dB |

NOTE: For programming the equalizer gain setting on a per channel basis, see the microprocessor register map for details.

3.2.3.2 EXLOS (Extended Loss of Signal)

By enabling the extended loss of signal by programming the appropriate channel register, the digital RLOS is extended to count 4,096 consecutive zeros before declaring RLOS in T1 and E1 mode. By default, EXLOS is disabled and RLOS operates in normal mode.

3.2.3.3 AIS (Alarm Indication Signal)

The XRT83SH38 adheres to the ITU-T G.775 specification for an all ones pattern. The alarm indication signal is set to "1" if an all ones pattern (at least 99.9% ones density) is present for T, where T is 3ms to 75ms in T1 mode. AIS will clear when the ones density is not met within the same time period T. In E1 mode, the AIS is set to "1" if the incoming signal has 2 or less zeros in a 512-bit window. AIS will clear when the incoming signal has 3 or more zeros in the 512-bit window.

3.2.3.4 FLSD (FIFO Limit Status Detection)

The purpose of the FIFO limit status is to indicate when the Read and Write FIFO pointers are within a pre-determined range (over-flow or under-flow indication). The FLSD is set to "1" if the FIFO Read and Write Pointers are within ±3-Bits.

3.2.3.5 LCVD (Line Code Violation Detection)

The LIU contains 8 independent, 16-bit LCV counters. When the counters reach full-scale, they remain saturated at FFFFh until they are reset globally or on a per channel basis. For performance monitoring, the counters can be updated globally or on a per channel basis to place the contents of the counters into holding registers. The LIU uses an indirect address bus to access a counter for a given channel. Once the contents of the counters have been placed in holding registers, they can be individually read out 8-bits at a time according to the BYTEsel bit in the appropriate global register. By default, the LSB is placed in the holding register until the BYTEsel is pulled "High" where upon the MSB will be placed in the holding register for read back. Once both bytes have been read, the next channel may be selected for read back.

By default, the LVC/OFD will be set to a "1" if the receiver is currently detecting line code violations or excessive zeros for HDB3 (E1 mode) or B8ZS (T1 mode). In AMI mode, the LCVD will be set to a "1" if the receiver is currently detecting bipolar violations or excessive zeros. However, if the LIU is configured to

monitor the 16-bit LCV counter by programming the appropriate global register, the LCV/OFD will be set to a "1" if the counter saturates.

3.3 Receive Jitter Attenuator

The receive path has a dedicated jitter attenuator that reduces phase and frequency jitter in the recovered clock. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth of 32-bit or 64-bit. If the LIU is used for line synchronization (loop timing systems), the JA should be enabled. When the Read and Write pointers of the FIFO are within 2-Bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this condition occurs, the jitter attenuator will not attenuate input jitter until the Read/Write pointer's position is outside the 2-Bit window. In T1 mode, the bandwidth of the JA is always set to 3Hz. In E1 mode, the bandwidth is programmable to either 10Hz or 1.5Hz (1.5Hz automatically selects the 64-Bit FIFO depth). The JA has a clock delay equal to 1/2 of the FIFO bit depth.

NOTE: If the LIU is used in a multiplexer/mapper application where stuffing bits are typically removed, the transmit path has a dedicated jitter attenuator to smooth out the gapped clock. See the Transmit Section of this datasheet.

3.4 HDB3/B8ZS Decoder

In single rail mode, RPOS can decode AMI or HDB3/B8ZS signals. For E1 mode, HDB3 is defined as any block of 4 successive zeros replaced with OOOV or BOOV, so that two successive V pulses are of opposite polarity to prevent a DC component. In T1 mode, 8 successive zeros are replaced with OOOVBOVB. If the HDB3/B8ZS decoder is selected, the receive path removes the V and B pulses so that the original data is output to RPOS.

3.5 RPOS/RNEG/RCLK

The digital output data can be programmed to either single rail or dual rail formats. **Figure 13** is a timing diagram of a repeating "0011" pattern in single-rail mode. **Figure 14** is a timing diagram of the same fixed pattern in dual rail mode.

FIGURE 13. SINGLE RAIL MODE WITH A FIXED REPEATING "0011" PATTERN

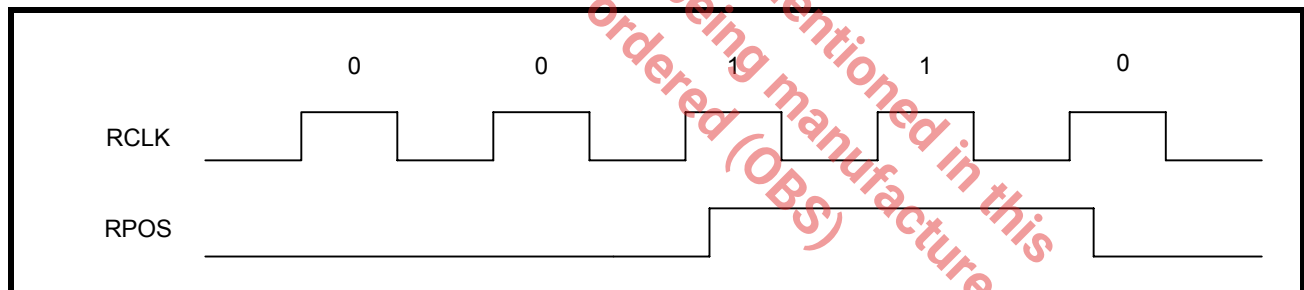
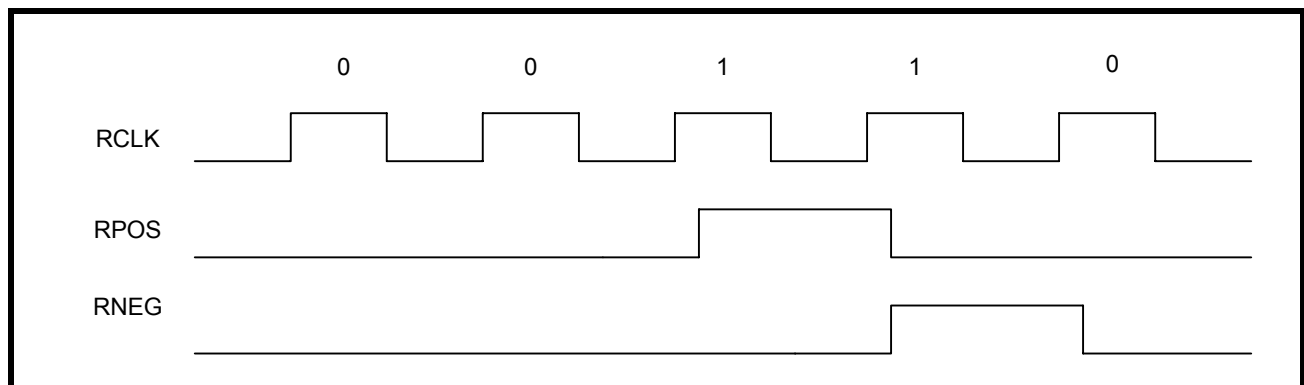


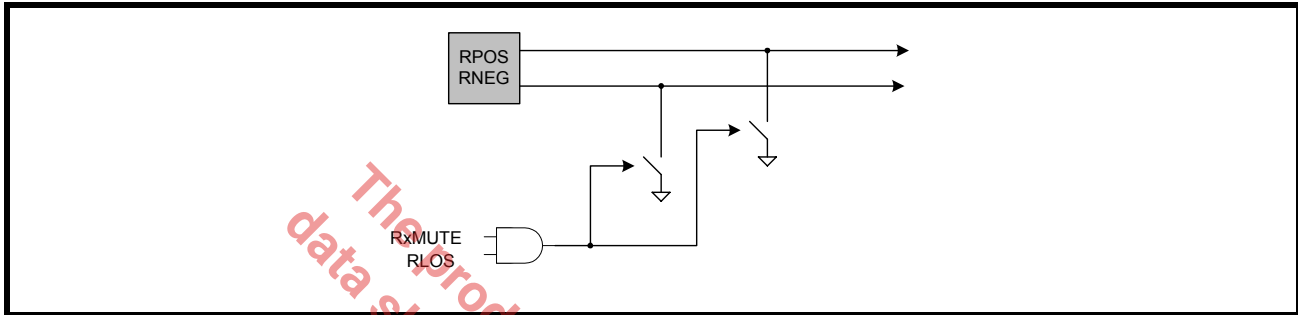
FIGURE 14. DUAL RAIL MODE WITH A FIXED REPEATING "0011" PATTERN



3.6 RxMUTE (Receiver LOS with Data Muting)

The receive muting function can be selected by setting RxMUTE to "1" in the appropriate global register. If selected, any channel that experiences an RLOS condition will automatically pull RPOS and RNEG "Low" to prevent data chattering. If RLOS does not occur, the RxMUTE will remain inactive until an RLOS on a given channel occurs. The default setting for RxMUTE is "0" which is disabled. A simplified block diagram of the RxMUTE function is shown in **Figure 15**.

FIGURE 15. SIMPLIFIED BLOCK DIAGRAM OF THE RxMUTE FUNCTION

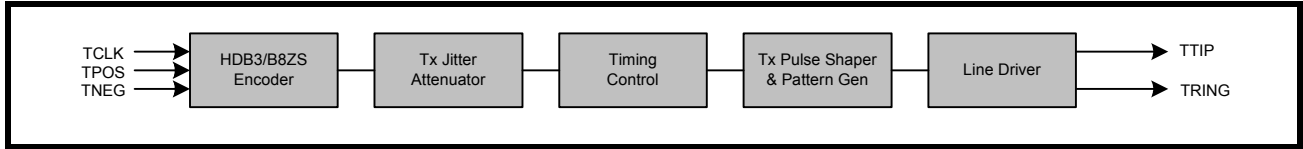


The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

4.0 TRANSMIT PATH LINE INTERFACE

The transmit path of the XRT83SH38 LIU consists of 8 independent T1/E1/J1 transmitters. The following section describes the complete transmit path from TCLK/TPOS/TNEG inputs to TTIP/TRING outputs. A simplified block diagram of the transmit path is shown in **Figure 16**.

FIGURE 16. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT PATH



4.1 TCLK/TPOS/TNEG Digital Inputs

In dual rail mode, TPOS and TNEG are the digital inputs for the transmit path. In single rail mode, TNEG has no function and can be left unconnected. The XRT83SH38 can be programmed to sample the inputs on either edge of TCLK. By default, data is sampled on the falling edge of TCLK. To sample data on the rising edge of TCLK, set TCLKE to "1" in the appropriate global register. **Figure 17** is a timing diagram of the transmit input data sampled on the falling edge of TCLK. **Figure 18** is a timing diagram of the transmit input data sampled on the rising edge of TCLK. The timing specifications are shown in **Table 7**.

FIGURE 17. TRANSMIT DATA SAMPLED ON FALLING EDGE OF TCLK

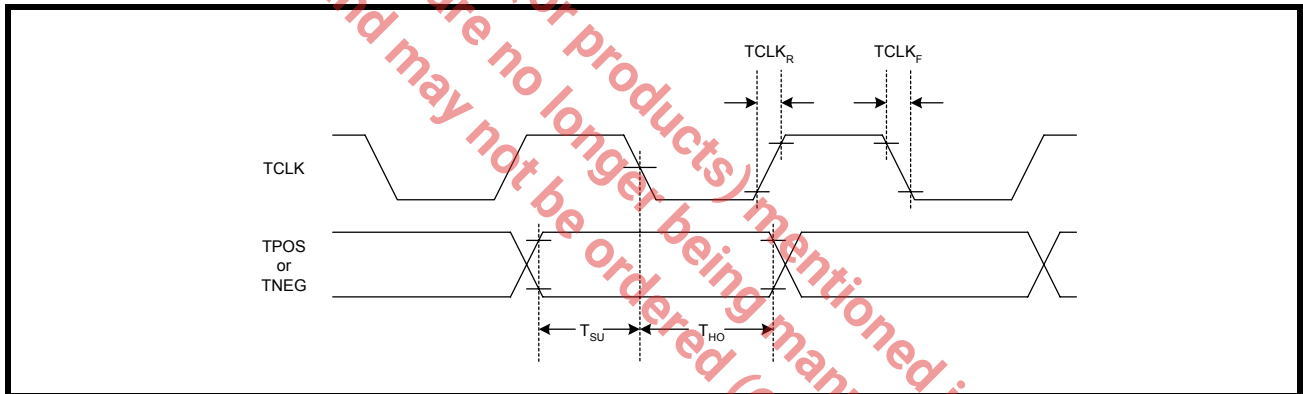


FIGURE 18. TRANSMIT DATA SAMPLED ON RISING EDGE OF TCLK

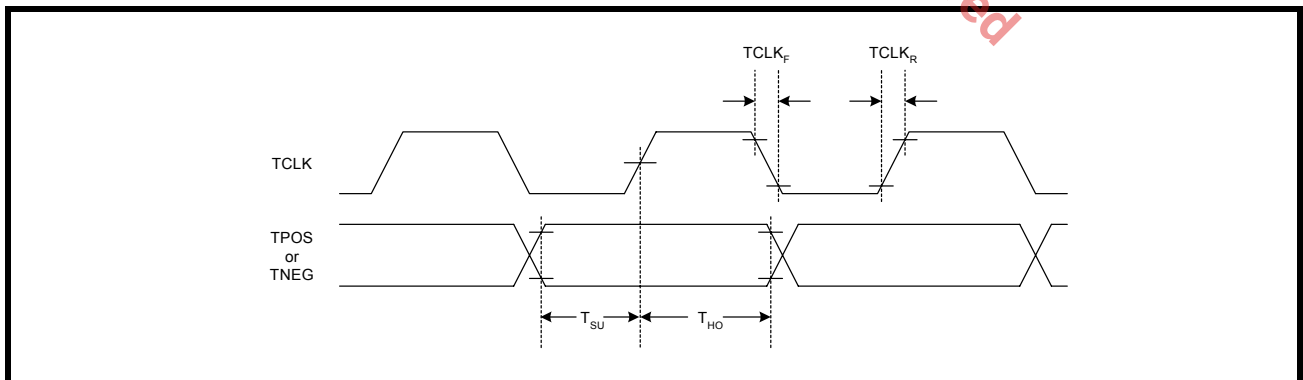


TABLE 7: TIMING SPECIFICATIONS FOR TCLK/TPOS/TNEG

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|-----------------------------|-------------------|-----|-----|-----|-------|
| TCLK Duty Cycle | T _{CDU} | 30 | 50 | 70 | % |
| Transmit Data Setup Time | T _{SU} | 50 | - | - | ns |
| Transmit Data Hold Time | T _{HO} | 30 | - | - | ns |
| TCLK Rise Time (10% to 90%) | TCLK _R | - | - | 40 | ns |
| TCLK Fall Time (90% to 10%) | TCLK _F | - | - | 40 | ns |

NOTE: VDD=3.3V ±5%, T_A=25°C, Unless Otherwise Specified

4.2 HDB3/B8ZS Encoder

In single rail mode, the LIU can encode the TPOS input signal to AMI or HDB3/B8ZS data. In E1 mode and HDB3 encoding selected, any sequence with four or more consecutive zeros in the input will be replaced with 000V or B00V, where "B" indicates a pulse conforming to the bipolar rule and "V" representing a pulse violating the rule. An example of HDB3 encoding is shown in **Table 8**. In T1 mode and B8ZS encoding selected, an input data sequence with eight or more consecutive zeros will be replaced using the B8ZS encoding rule. An example with Bipolar with 8 Zero Substitution is shown in **Table 9**.

TABLE 8: EXAMPLES OF HDB3 ENCODING

| | NUMBER OF PULSES BEFORE NEXT 4 ZEROS | |
|---------------|--------------------------------------|------|
| Input | | 0000 |
| HDB3 (Case 1) | Odd | 000V |
| HDB3 (Case 2) | Even | B00V |

TABLE 9: EXAMPLES OF B8ZS ENCODING

| CASE 1 | PRECEDING PULSE | NEXT 8 BITS |
|---------------|-----------------|-------------|
| Input | + | 00000000 |
| B8ZS | | 000VB0VB |
| AMI Output | + | 000+-0-+ |
| Case 2 | | |
| Input | - | 00000000 |
| B8ZS | | 000VB0VB |
| AMI Output | - | 000-+0+- |

4.3 Transmit Jitter Attenuator

The XRT83SH38 LIU is ideal for multiplexer or mapper applications where the network data crosses multiple timing domains. As the higher data rates are de-multiplexed down to T1 or E1 data, stuffing bits are typically removed which can leave gaps in the incoming data stream. The transmit path has a dedicated jitter attenuator with a 32-Bit or 64-Bit FIFO that is used to smooth the gapped clock into a steady T1 or E1 output. The maximum gap width of the 8-Channel LIU is shown in **Table 10**.

TABLE 10: MAXIMUM GAP WIDTH FOR MULTIPLEXER/MAPPER APPLICATIONS

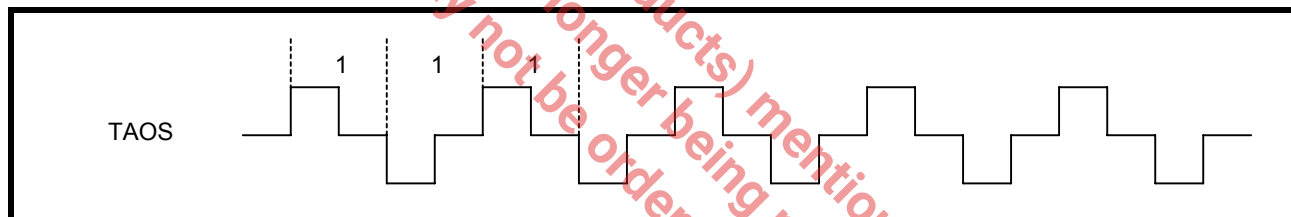
| FIFO DEPTH | MAXIMUM GAP WIDTH |
|------------|-------------------|
| 32-Bit | 20 UI |
| 64-Bit | 50 UI |

NOTE: If the LIU is used in a loop timing system, the receive path has a dedicated jitter attenuator. See the Receive Section of this datasheet.

4.4 TAOS (Transmit All Ones)

The XRT83SH38 has the ability to transmit all ones on a per channel basis by programming the appropriate channel register. This function takes priority over the digital data present on the TPOS/TNEG inputs. For example: If a fixed "0011" pattern is present on TPOS in single rail mode and TAOS is enabled, the transmitter will output all ones. In addition, if digital or dual loopback is selected, the data on the RPOS output will be equal to the data on the TPOS input. **Figure 19** is a diagram showing the all ones signal at TTIP and TRING.

FIGURE 19. TAOS (TRANSMIT ALL ONES)



4.5 Transmit Diagnostic Features

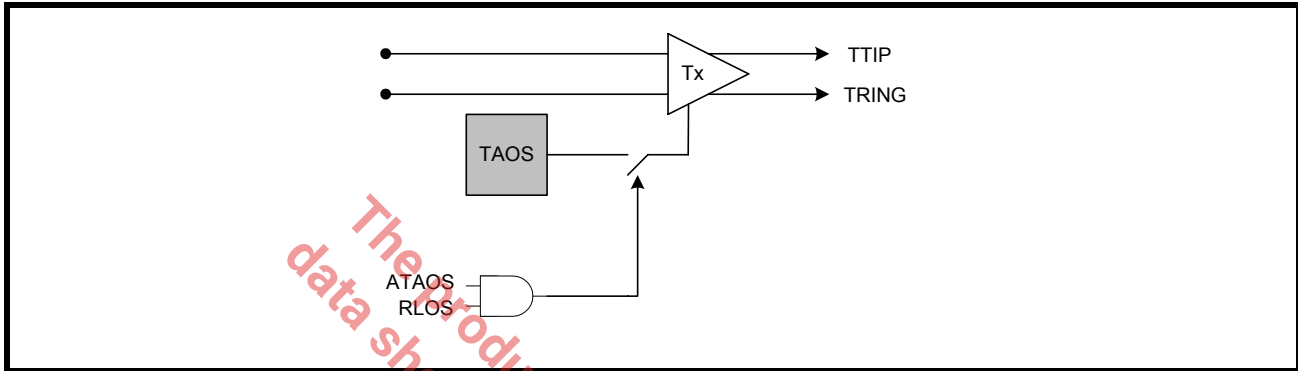
In addition to TAOS, the XRT83SH38 offers diagnostic features for analyzing network integrity such as ATAOS and QRSS on a per channel basis by programming the appropriate registers. These diagnostic features take priority over the digital data present on TPOS/TNEG inputs. The transmitters will send the diagnostic code to the line and will be maintained in the digital loopback if selected. When the LIU is responsible for sending diagnostic patterns, the LIU is automatically placed in the single rail mode.

8-CHANNEL T1/E1/J1 SHORT-HAUL LINE INTERFACE UNIT

4.5.1 ATAOS (Automatic Transmit All Ones)

If ATAOS is selected by programming the appropriate global register, an AMI all ones signal will be transmitted for each channel that experiences an RLOS condition. If RLOS does not occur, the ATAOS will remain inactive until an RLOS on a given channel occurs. A simplified block diagram of the ATAOS function is shown in Figure 20.

FIGURE 20. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION



4.5.2 QRSS Generation

The XRT83SH38 can transmit a QRSS random sequence to a remote location from TTIP/TRING. The polynomial is shown in Table 11.

TABLE 11: RANDOM BIT SEQUENCE POLYNOMIALS

| RANDOM PATTERN | T1 | E1 |
|----------------|--------------|--------------|
| QRSS | $2^{20} - 1$ | $2^{15} - 1$ |

4.5.3 T1 Short Haul Line Build Out (LBO)

The short haul transmitter output pulses are generated using a 7-Bit internal DAC (6-Bit plus the MSB sign bit). The line build out can be set to interface to five different ranges of cable attenuation by programming the appropriate channel register. The pulse shape is divided into eight discrete time segments which are set to fixed values to comply with the pulse template. To program the eight segments individually to optimize a special line build out, see the arbitrary pulse section of this datasheet. The short haul LBO settings are shown in Table 12.

TABLE 12: SHORT HAUL LINE BUILD OUT

| LBO SETTING EQC[4:0] | RANGE OF CABLE ATTENUATION |
|----------------------|----------------------------|
| 08h (01000) | 0 - 133 Feet |
| 09h (01001) | 133 - 266 Feet |
| 0Ah (01010) | 266 - 399 Feet |
| 0Bh (01011) | 399 - 533 Feet |
| 0Ch (01100) | 533 - 655 Feet |

4.5.4 Arbitrary Pulse Generator For T1 and E1

The arbitrary pulse generator divides the pulse into eight individual segments. Each segment is set by a 7-Bit binary word by programming the appropriate channel register. This allows the system designer to set the overshoot, amplitude, and undershoot for a unique line build out. The MSB (bit 7) is a sign-bit. If the sign-bit is set to "0", the segment will move in a positive direction relative to a flat line (zero) condition. If this sign-bit is set to "1", the segment will move in a negative direction relative to a flat line condition. The resolution of the DAC is typically 60mV per LSB. Thus, writing 7-bit = 1111111 will clamp the output at either voltage rail corresponding to a maximum amplitude. A pulse with numbered segments is shown in **Figure 21**.

FIGURE 21. ARBITRARY PULSE SEGMENT ASSIGNMENT



NOTE: By default, the arbitrary segments are programmed to 0x00h. The transmitter outputs will result in an all zero pattern to the line interface.

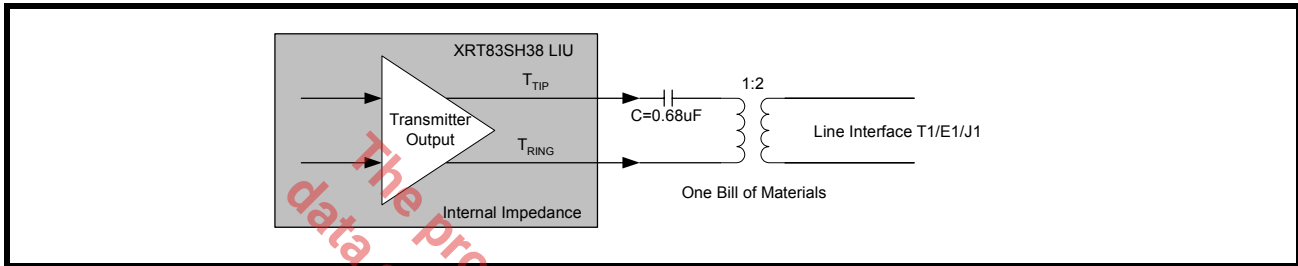
4.6 DMO (Digital Monitor Output)

The driver monitor circuit is used to detect transmit driver failures by monitoring the activities at TTIP/TRING outputs. Driver failure may be caused by a short circuit in the primary transformer or system problems at the transmit inputs. If the transmitter of a channel has no output for more than 128 clock cycles, DMO goes "High" until a valid transmit pulse is detected. If the DMO interrupt is enabled, the change in status of DMO will cause the interrupt pin to go "Low". Once the status register is read, the interrupt pin will return "High" and the status register will be reset (RUR).

4.7 Line Termination (TTIP/TRING)

The output stage of the transmit path generates standard return-to-zero (RZ) signals to the line interface for T1/E1/J1 twisted pair or E1 coaxial cable. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The transmitter outputs only require one DC blocking capacitor of 0.68 μ F. For redundancy applications (or simply to tri-state the transmitters), set TxTSEL to a "1" in the appropriate channel register. A typical transmit interface is shown in **Figure 22**.

FIGURE 22. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



5.0 T1/E1 APPLICATIONS

This applications section describes common T1/E1 system considerations along with references to application notes available for reference where applicable.

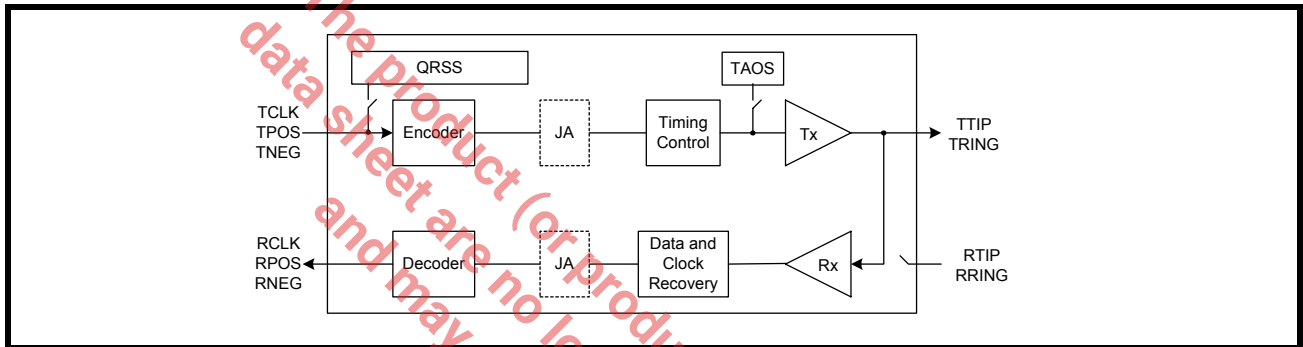
5.1 Loopback Diagnostics

The XRT83SH38 supports several loopback modes for diagnostic testing. The following section describes the local analog loopback, remote loopback, digital loopback, and dual loopback modes.

5.1.1 Local Analog Loopback

With local analog loopback activated, the transmit output data at TTIP/TRING is internally looped back to the analog inputs at RTIP/RRING. External inputs at RTIP/RRING are ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of local analog loopback is shown in **Figure 23**.

FIGURE 23. SIMPLIFIED BLOCK DIAGRAM OF LOCAL ANALOG LOOPBACK

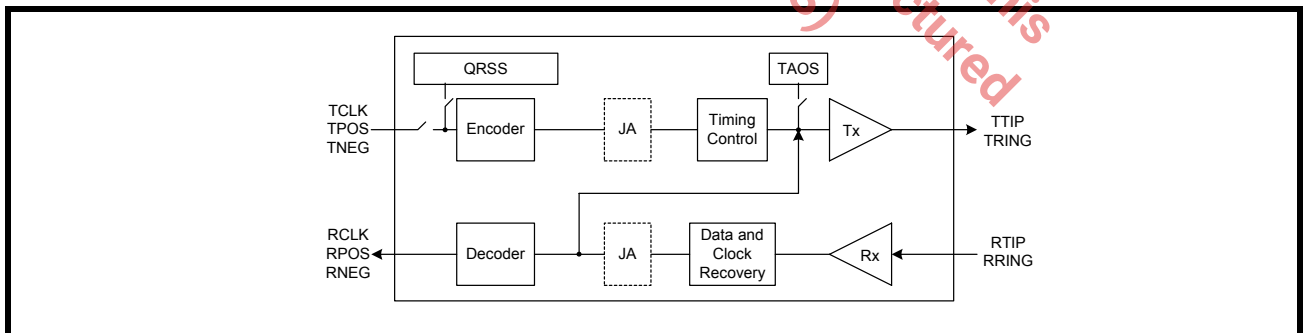


NOTE: The transmit diagnostic features such as TAOS and QRSS take priority over the transmit input data at TCLK/TPOS/TNEG.

5.1.2 Remote Loopback

With remote loopback activated, the receive input data at RTIP/RRING is internally looped back to the transmit output data at TTIP/TRING. The remote loopback includes the Receive JA (if enabled). The transmit input data at TCLK/TPOS/TNEG are ignored while valid receive output data continues to be sent to the system. A simplified block diagram of remote loopback is shown in **Figure 24**.

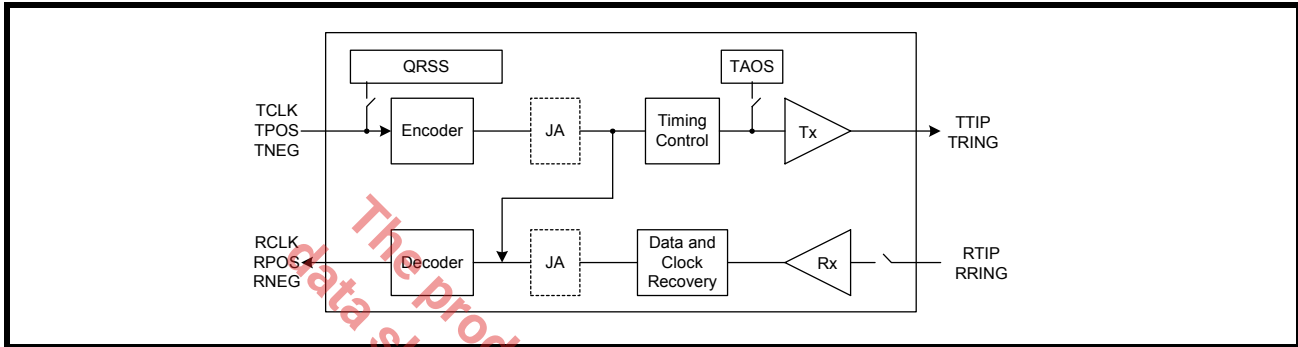
FIGURE 24. SIMPLIFIED BLOCK DIAGRAM OF REMOTE LOOPBACK



5.1.3 Digital Loopback

With digital loopback activated, the transmit input data at TCLK/TPOS/TNEG is looped back to the receive output data at RCLK/RPOS/RNEG. The digital loopback mode includes the Transmit JA (if enabled). The receive input data at RTIP/RRING is ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of digital loopback is shown in **Figure 25**.

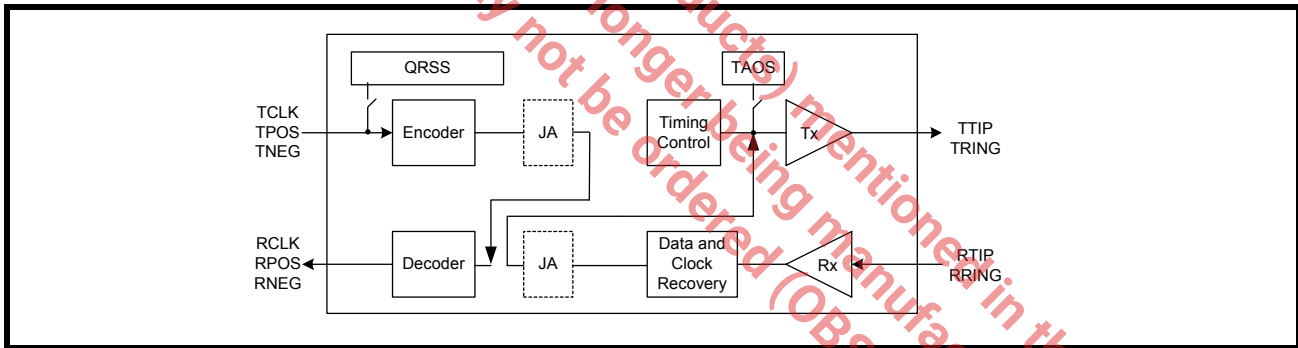
FIGURE 25. SIMPLIFIED BLOCK DIAGRAM OF DIGITAL LOOPBACK



5.1.4 Dual Loopback

With dual loopback activated, the remote loopback is combined with the digital loopback. A simplified block diagram of dual loopback is shown in **Figure 26**.

FIGURE 26. SIMPLIFIED BLOCK DIAGRAM OF DUAL LOOPBACK



5.2 Line Card Redundancy

Telecommunication system design requires signal integrity and reliability. When a T1/E1 primary line card has a failure, it must be swapped with a backup line card while maintaining connectivity to a backplane without losing data. System designers can achieve this by implementing common redundancy schemes with the XRT83SH38 LIU. EXAR offers features that are tailored to redundancy applications while reducing the number of components and providing system designers with solid reference designs.

RLOS and DMO

If an RLOS or DMO condition occurs, the XRT83SH38 reports the alarm to the individual status registers on a per channel basis. However, for redundancy applications, an RLOS or DMO alarm can be used to initiate an automatic switch to the back up card. For this application, two global pins RLOS and DMO are used to indicate that one of the 8-channels has an RLOS or DMO condition.

Typical Redundancy Schemes

- 1:1 One backup card for every primary card (Facility Protection)
- 1+1 One backup card for every primary card (Line Protection)
- ·N+1 One backup card for N primary cards

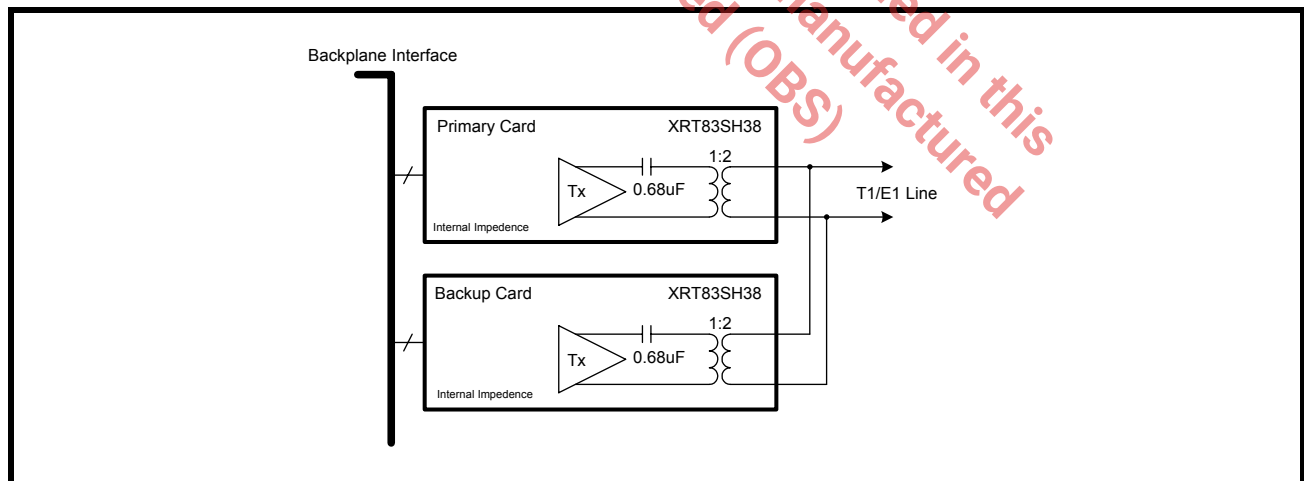
5.2.1 1:1 and 1+1 Redundancy Without Relays

The 1:1 facility protection and 1+1 line protection have one backup card for every primary card. When using 1:1 or 1+1 redundancy, the backup card has its transmitters tri-stated and its receivers in high impedance. This eliminates the need for external relays and provides one bill of materials for all interface modes of operation. For 1+1 line protection, the receiver inputs on the backup card have the ability to monitor the line for bit errors while in high impedance. The transmit and receive sections of the LIU device are described separately.

5.2.2 Transmit Interface with 1:1 and 1+1 Redundancy

The transmitters on the backup card should be tri-stated. Select the appropriate impedance for the desired mode of operation, T1/E1/J1. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See **Figure 27**. for a simplified block diagram of the transmit section for a 1:1 and 1+1 redundancy.

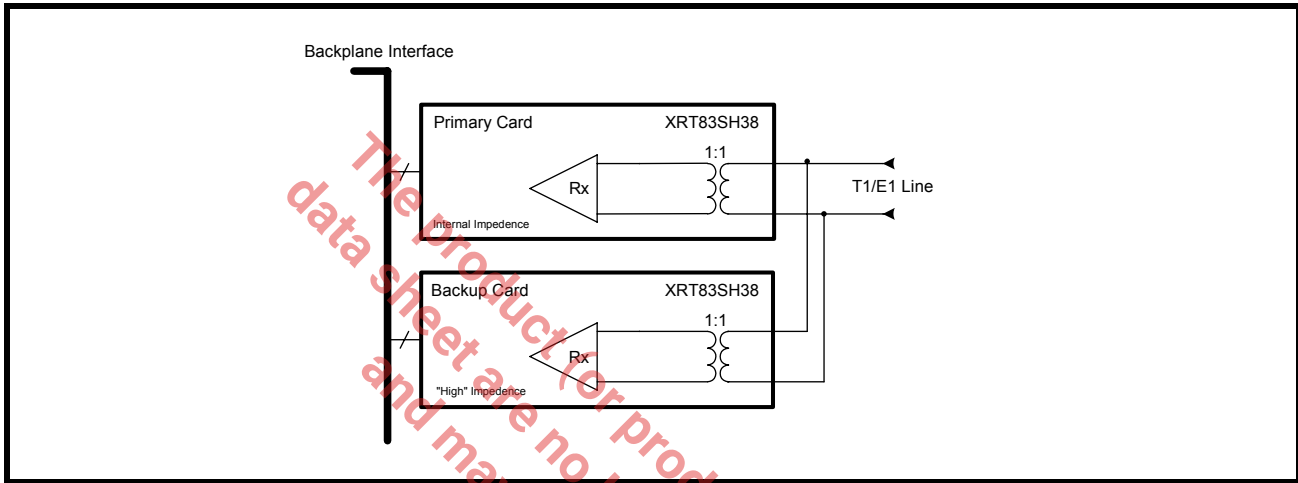
FIGURE 27. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR 1:1 AND 1+1 REDUNDANCY



5.2.3 Receive Interface with 1:1 and 1+1 Redundancy

The receivers on the backup card should be programmed for "High" impedance. Since there is no external resistor in the circuit, the receivers on the backup card will not load down the line interface. This key design feature eliminates the need for relays and provides one bill of materials for all interface modes of operation. Select the impedance for the desired mode of operation, T1/E1/J1. To swap the primary card, set the backup card to internal impedance, then the primary card to "High" impedance. See **Figure 28**. for a simplified block diagram of the receive section for a 1:1 redundancy scheme.

FIGURE 28. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR 1:1 AND 1+1 REDUNDANCY



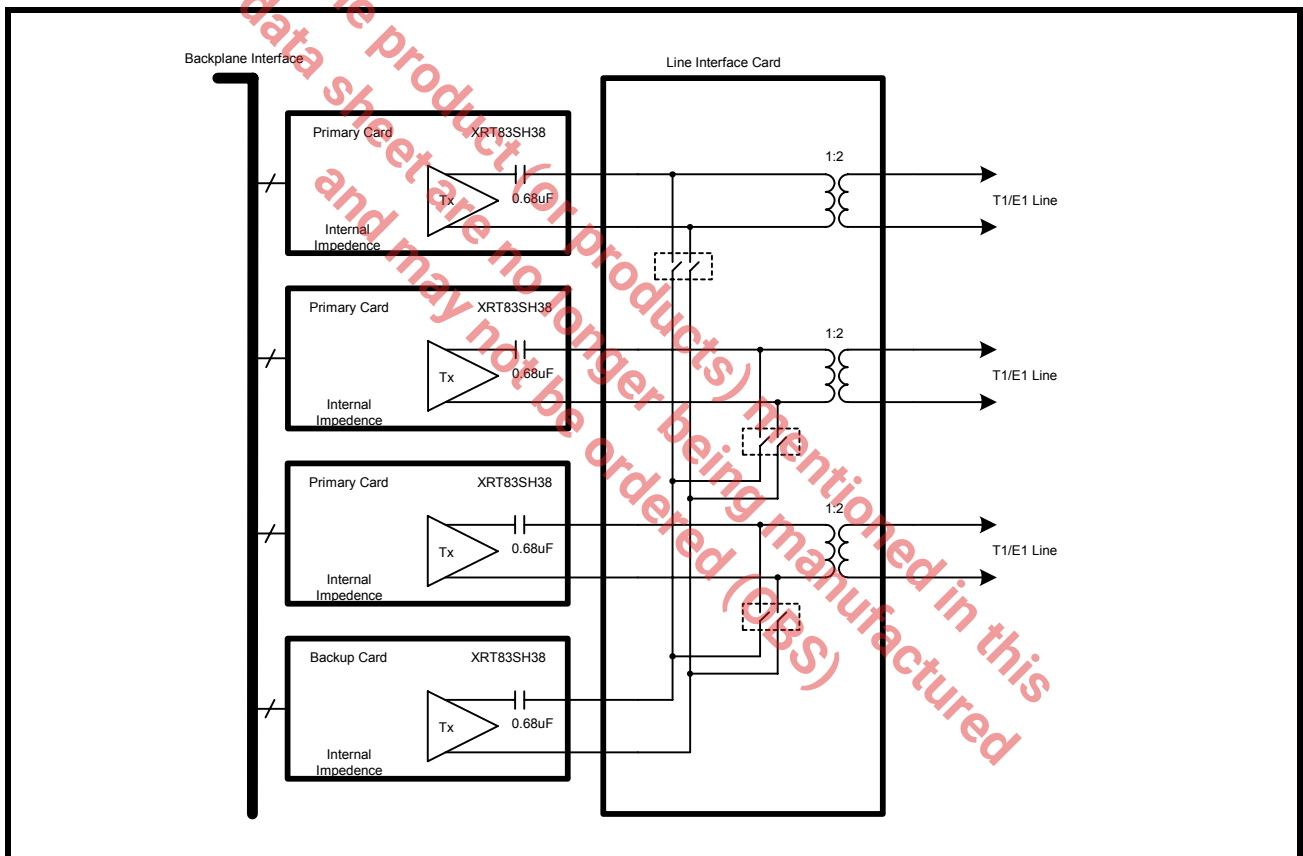
5.2.4 N+1 Redundancy Using External Relays

N+1 redundancy has one backup card for N primary cards. Due to impedance mismatch and signal contention, external relays are necessary when using this redundancy scheme. The relays create complete isolation between the primary cards and the backup card. This allows all transmitters and receivers on the primary cards to be configured in internal impedance, providing one bill of materials for all interface modes of operation. The transmit and receive sections of the LIU device are described separately.

5.2.5 Transmit Interface with N+1 Redundancy

For N+1 redundancy, the transmitters on all cards should be programmed for internal impedance. The transmitters on the backup card do not have to be tri-stated. To swap the primary card, close the desired relays, and tri-state the transmitters on the failed primary card. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See **Figure 29** for a simplified block diagram of the transmit section for an N+1 redundancy scheme.

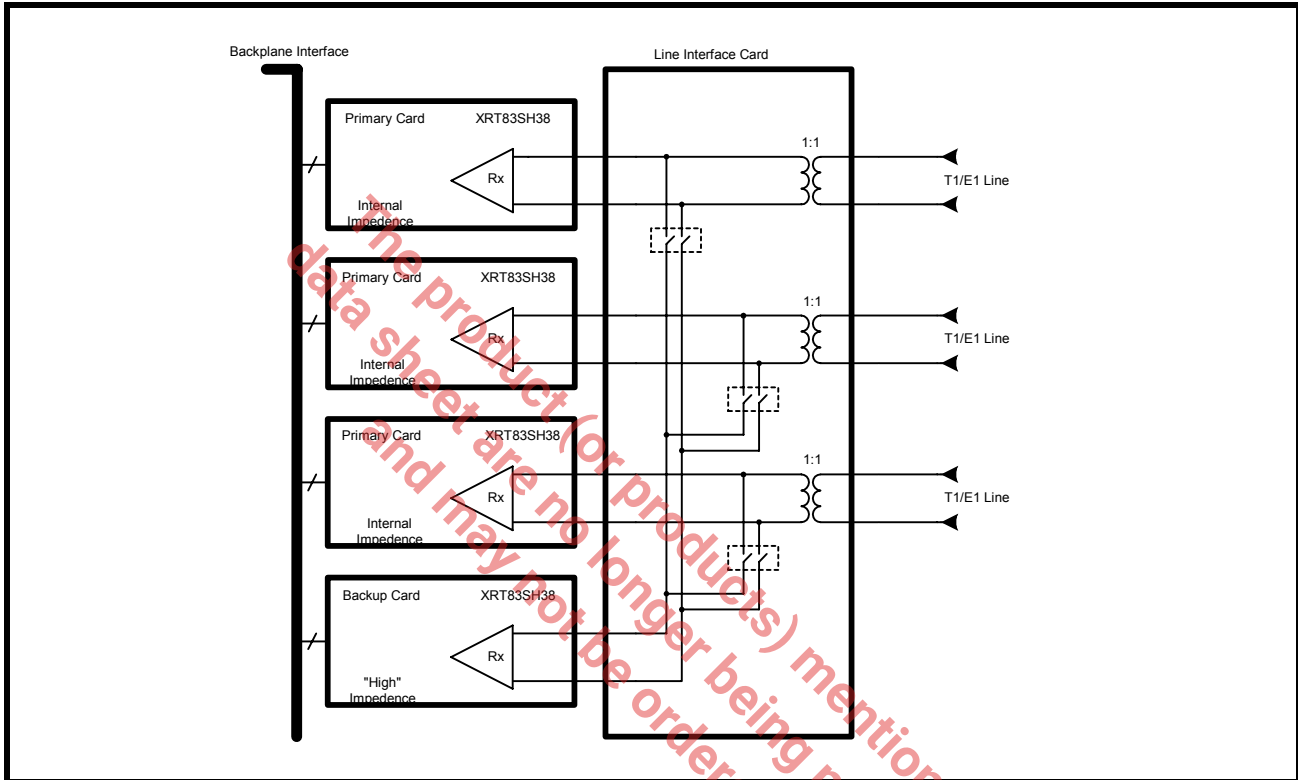
FIGURE 29. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR N+1 REDUNDANCY



5.2.6 Receive Interface with N+1 Redundancy

For N+1 redundancy, the receivers on the primary cards should be programmed for internal impedance. The receivers on the backup card should be programmed for "High" impedance mode. To swap the primary card, set the backup card to internal impedance, then the primary card to "High" impedance. See **Figure 30** for a simplified block diagram of the receive section for a N+1 redundancy scheme.

FIGURE 30. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR N+1 REDUNDANCY



5.3 Power Failure Protection

For 1:1 or 1+1 line card redundancy in T1/E1 applications, power failure could cause a line card to change the characteristics of the line impedance, causing a degradation in system performance. The XRT83SH38 was designed to ensure reliability during power failures. The LIU has patented high impedance circuits that allow the receiver inputs and the transmitter outputs to be in "High" impedance when the LIU experiences a power failure or when the LIU is powered off.

NOTE: For power failure protection, a transformer must be used to couple to the line interface. See the TAN-56 application note for more details.

5.4 Overvoltage and Overcurrent Protection

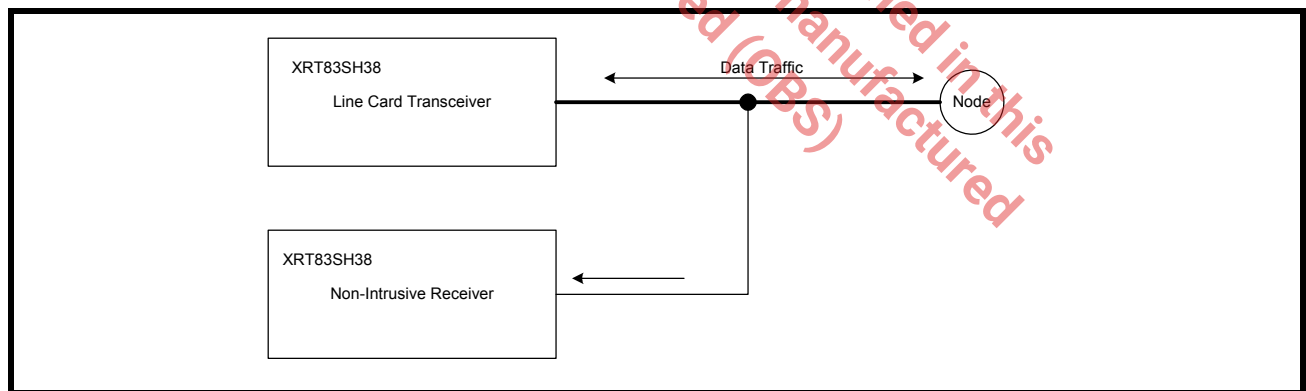
Physical layer devices such as LIUs that interface to telecommunications lines are exposed to overvoltage transients posed by environmental threats. An Overvoltage transient is a pulse of energy concentrated over a small period of time, usually under a few milliseconds. These pulses are random and exceed the operating conditions of CMOS transceiver ICs. Electronic equipment connecting to data lines are susceptible to many forms of overvoltage transients such as lightning, AC power faults and electrostatic discharge (ESD). There are three important standards when designing a telecommunications system to withstand overvoltage transients.

- UL1950 and FCC Part 68
- Telcordia (Bellcore) GR-1089
- ITU-T K.20, K.21 and K.41

5.5 Non-Intrusive Monitoring

In non-intrusive monitoring applications, the transmitters are shut off by setting TxON "Low". The receivers must be actively receiving data without interfering with the line impedance. The XRT83SH38's internal termination ensures that the line termination meets T1/E1 specifications for 75Ω, 100Ω or 120Ω while monitoring the data stream. System integrity is maintained by placing the non-intrusive receiver in "High" impedance, equivalent to that of a 1+1 redundancy application. A simplified block diagram of non-intrusive monitoring is shown in **Figure 31**.

FIGURE 31. SIMPLIFIED BLOCK DIAGRAM OF A NON-INTRUSIVE MONITORING APPLICATION



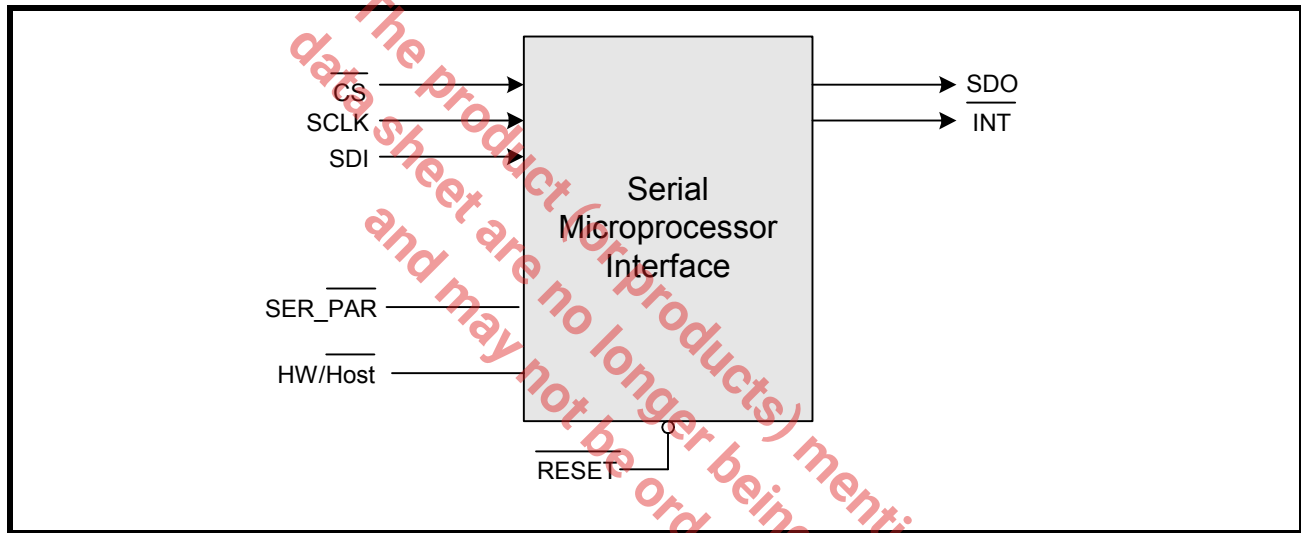
6.0 MICROPROCESSOR INTERFACE

The microprocessor interface can be accessed through a standard serial interface (BGA Package Only) or a standard parallel microprocessor interface. The SER_PAR pin is used to select between the two. By default, the chip is configured in the Parallel Microprocessor interface. For Serial communication, this pin must be pulled "High".

6.1 Serial Microprocessor Interface Block

The serial microprocessor uses a standard 3-pin serial port with CS, SCLK, and SDI for programming the LIU. Optional pins such as SDO, INT, and RESET allow the ability to read back contents of the registers, monitor the LIU via an interrupt pin, and reset the LIU to its default configuration by pulling reset "Low" for more than 10µS. A simplified block diagram of the Serial Microprocessor is shown in **Figure 32**.

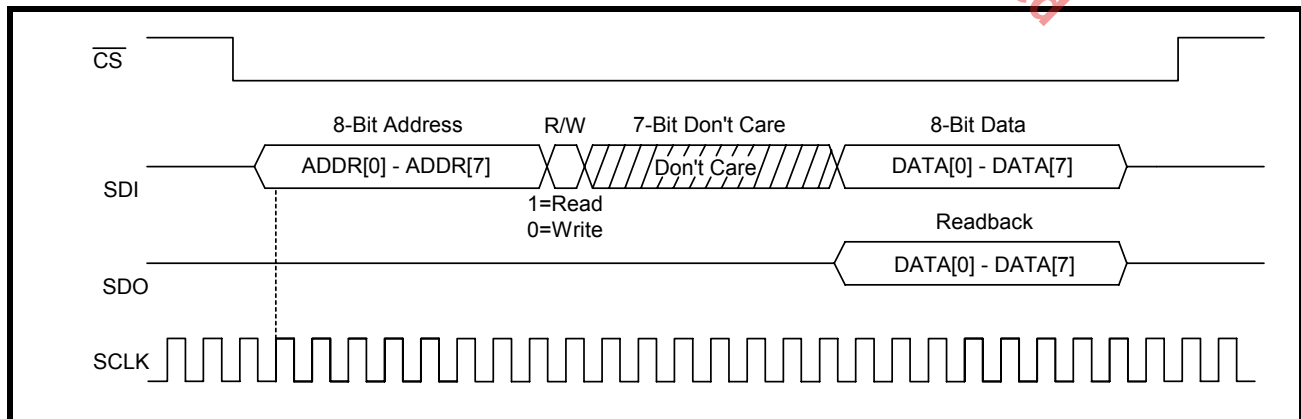
FIGURE 32. SIMPLIFIED BLOCK DIAGRAM OF THE SERIAL MICROPROCESSOR INTERFACE



6.1.1 Serial Timing Information

The serial port requires 24 bits of data applied to the SDI (Serial Data Input) pin. The Serial Microprocessor samples SDI on the rising edge of SCLK (Serial Clock Input). The data is not latched into the device until all 24 bits of serial data have been sampled. A timing diagram of the Serial Microprocessor is shown in **Figure 33**.

FIGURE 33. TIMING DIAGRAM FOR THE SERIAL MICROPROCESSOR INTERFACE



NOTE: For applications without a free running SCLK, a minimum of 1 SCLK pulse must be applied when CS is "High", before pulling CS "Low".

6.1.2 24-Bit Serial Data Input Description

The serial data input is sampled on the rising edge of SCLK. In readback mode, the serial data output is updated on the falling edge of SCLK. The serial data must be applied to the LIU LSB first. The 24 bits of serial data are described below.

6.1.3 ADDR[7:0] (SCLK1 - SCLK8)

The first 8 SCLK cycles are used to provide the address to which a Read or Write operation will occur. ADDR[0] (LSB) must be sent to the LIU first followed by ADDR[1] and so forth until all 8 address bits have been sampled by SCLK.

6.1.4 R/W (SCLK9)

The next serial bit applied to the LIU informs the microprocessor that a Read or Write operation is desired. If the R/W bit is set to "0", the microprocessor is configured for a Write operation. If the R/W bit is set to "1", the microprocessor is configured for a Read operation.

6.1.5 Dummy Bits (SCLK10 - SCLK16)

The next 7 SCLK cycles are used as dummy bits. Seven bits were chosen so that the serial interface can easily be divided into three 8-bit words to be compliant with standard serial interface devices. The state of these bits are ignored and can hold either "0" or "1" during both Read and Write operations.

6.1.6 DATA[7:0] (SCLK17 - SCLK24)

The next 8 SCLK cycles are used to provide the data to be written into the internal register chosen by the address bits. DATA[0] (LSB) must be sent to the LIU first followed by DATA[1] and so forth until all 8 data bits have been sampled by SCLK. Once 24 SCLK cycles have been completed, the LIU holds the data until \overline{CS} is pulled "High" whereby, the serial microprocessor latches the data into the selected internal register.

6.1.7 8-Bit Serial Data Output Description

The serial data output is updated on the falling edge of SCLK17 - SCLK24 if R/W is set to "1". DATA[0] (LSB) is provided on SCLK17 to the SDO pin first followed by DATA[1] and so forth until all 8 data bits have been updated. The SDO pin allows the user to read the contents stored in individual registers by providing the desired address on the SDI pin during the Read cycle.

FIGURE 34. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

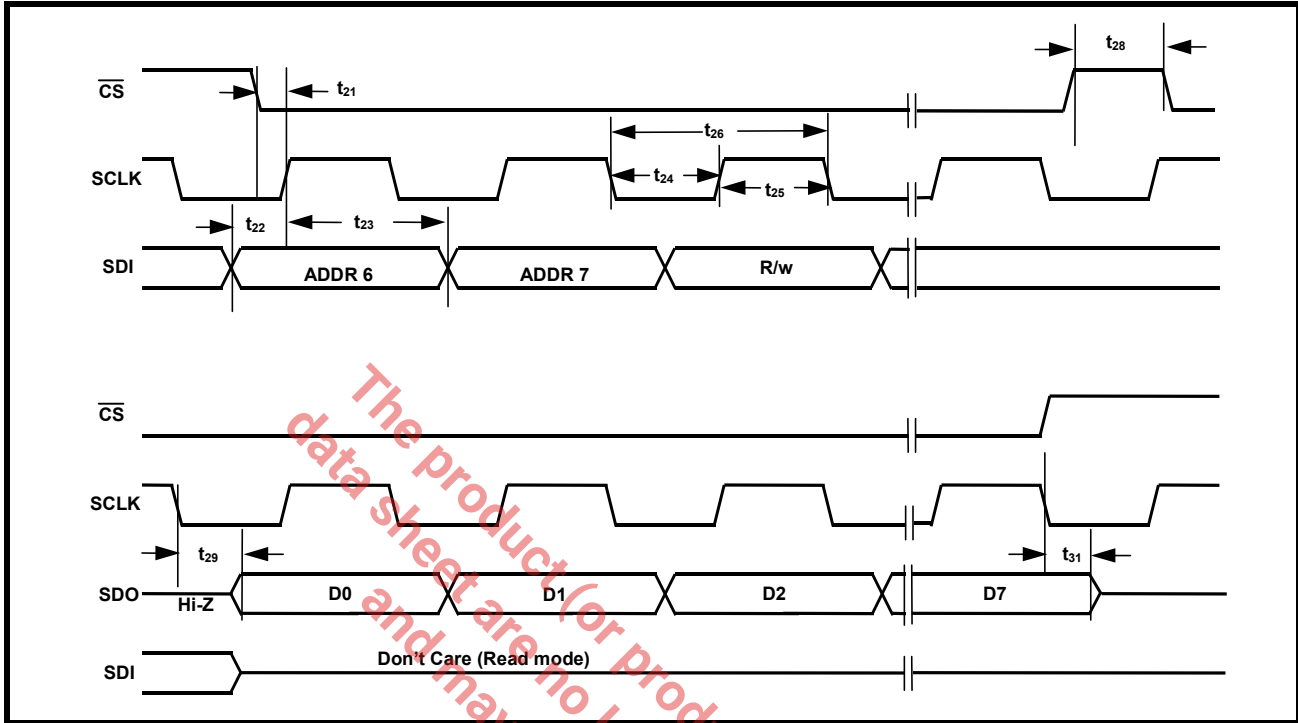


TABLE 13: MICROPROCESSOR SERIAL INTERFACE TIMINGS ($T_A = 25^{\circ}C$, $V_{DD} = 3.3V \pm 5\%$ AND LOAD = 10PF)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS |
|----------|--|------|------|------|-------|
| t_{21} | \overline{CS} Low to Rising Edge of SClk | 5 | | | ns |
| t_{22} | SDI to Rising Edge of SClk | 5 | | | ns |
| t_{23} | SDI to Rising Edge of SClk Hold Time | 5 | | | ns |
| t_{24} | SCLK "Low" Time | 20 | | | ns |
| t_{25} | SCLK "High" Time | 20 | | | ns |
| t_{26} | SCLK Period | 40 | | | ns |
| t_{28} | \overline{CS} Inactive Time | 40 | | | ns |
| t_{29} | Falling Edge of SClk to SDO Valid Time | | | 5 | ns |
| t_{31} | Rising edge of \overline{CS} to High Z | | | 5 | ns |

6.2 Parallel Microprocessor Interface Block

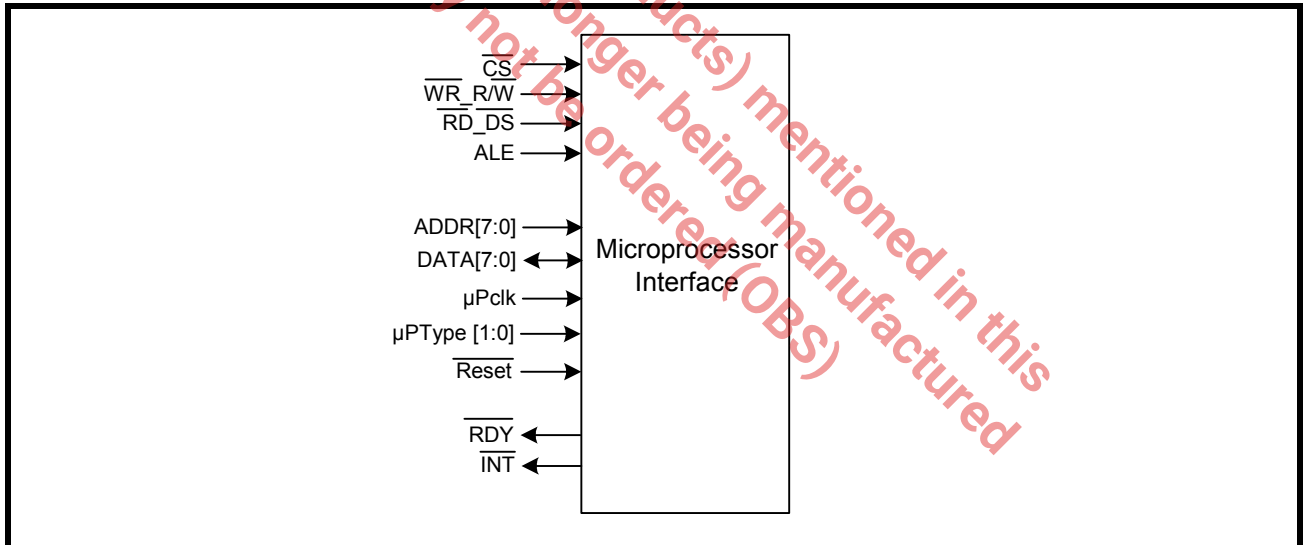
The Parallel Microprocessor Interface section supports communication between the local microprocessor (μ P) and the LIU. The XRT83SH38 supports an Intel asynchronous interface, Motorola 68K asynchronous, and an Intel/Motorola interface. The microprocessor interface is selected by the state of the μ PTS[1:0] input pins. Selecting the microprocessor interface is shown in **Table 14**.

TABLE 14: SELECTING THE MICROPROCESSOR INTERFACE MODE

| μ PTS[1:0] | MICROPROCESSOR MODE |
|----------------|---|
| 0h (00) | Intel 68HC11, 8051, 80C188 (Asynchronous) |
| 1h (01) | Motorola 68K (Asynchronous) |
| 2h (10) | Intel x86 (Synchronous) |
| 3h (11) | 860 Motorola (Synchronous) |

The XRT83SH38 uses multipurpose pins to configure the device appropriately. The local μ P configures the LIU by writing data into specific addressable, on-chip Read/Write registers. The microprocessor interface provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The microprocessor interface also supports polled and interrupt driven environments. A simplified block diagram of the microprocessor interface is shown in **Figure 35**.

FIGURE 35. SIMPLIFIED BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK



6.3 The Microprocessor Interface Block Signals

The LIU may be configured into different operating modes and have its performance monitored by software through a standard microprocessor using data, address and control signals. These interface signals are described below in [Table 15](#), [Table 16](#), and [Table 17](#). The microprocessor interface can be configured to operate in Intel mode or Motorola mode. When the microprocessor interface is operating in Intel mode, some of the control signals function in a manner required by the Intel 80xx family of microprocessors. Likewise, when the microprocessor interface is operating in Motorola mode, then these control signals function in a manner as required by the Motorola microprocessors. (For using a Motorola 68K asynchronous processor, see [Figure 37](#) and [Table 19](#)) [Table 15](#) lists and describes those microprocessor interface signals whose role is constant across the two modes. [Table 16](#) describes the role of some of these signals when the microprocessor interface is operating in the Intel mode. Likewise, [Table 17](#) describes the role of these signals when the microprocessor interface is operating in the Motorola Power PC mode.

TABLE 15: XRT83SH38 MICROPROCESSOR INTERFACE SIGNALS THAT EXHIBIT CONSTANT ROLES IN BOTH INTEL AND MOTOROLA MODES

| PIN NAME | TYPE | DESCRIPTION |
|------------------------|------|--|
| μ PTS[1:0] | I | Microprocessor Interface Mode Select Input pins These three pins are used to specify the microprocessor interface mode. The relationship between the state of these three input pins, and the corresponding microprocessor mode is presented in Table 14 . |
| DATA[7:0] | I/O | Bi-Directional Data Bus for register "Read" or "Write" Operations. |
| ADDR[7:0] | I | Eight-Bit Address Bus Inputs The XRT83SH38 LIU microprocessor interface uses a direct address bus. This address bus is provided to permit the user to select an on-chip register for Read/Write access. |
| $\overline{\text{CS}}$ | I | Chip Select Input This active low signal selects the microprocessor interface of the XRT83SH38 LIU and enables Read/Write operations with the on-chip register locations. |

TABLE 16: INTEL MODE: MICROPROCESSOR INTERFACE SIGNALS

| XRT83SH38 PIN NAME | INTEL EQUIVALENT PIN | TYPE | DESCRIPTION |
|-------------------------------------|-------------------------|------|--|
| ALE | ALE | I | Address-Latch Enable: This active high signal is used to latch the contents on the address bus ADDR[7:0]. The contents of the address bus are latched into the ADDR[7:0] inputs on the falling edge of ALE. |
| $\overline{\text{RD}}_{\text{DS}}$ | $\overline{\text{RD}}$ | I | Read Signal: This active low input functions as the read signal from the local μ P. When this pin is pulled "Low" (if $\overline{\text{CS}}$ is "Low") the LIU is informed that a read operation has been requested and begins the process of the read cycle. |
| $\overline{\text{WR}}_{\text{R/W}}$ | $\overline{\text{WR}}$ | I | Write Signal: This active low input functions as the write signal from the local μ P. When this pin is pulled "Low" (if $\overline{\text{CS}}$ is "Low") the LIU is informed that a write operation has been requested and begins the process of the write cycle. |
| $\overline{\text{RDY}}$ | $\overline{\text{RDY}}$ | O | Ready Output: This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command. |

TABLE 17: MOTOROLA MODE: MICROPROCESSOR INTERFACE SIGNALS

| XRT83SH38 PIN NAME | MOTOROLA EQUIVALENT PIN | TYPE | DESCRIPTION |
|-------------------------------|------------------------------------|-------------|--|
| ALE | AS | I | Address Strobe: This active high signal is used to latch the contents on the address bus ADDR[7:0]. The contents of the address bus are latched into the ADDR[7:0] inputs on the falling edge of TS. |
| $\overline{WR_R/W}$ | R/\overline{W} | I | Read/Write: This input pin from the local μP is used to inform the LIU whether a Read or Write operation has been requested. When this pin is pulled "High", DS will initiate a read operation. When this pin is pulled "Low", DS will initiate a write operation. |
| $\overline{RD_DS}$ | DS | I | Data Strobe: This active low input functions as the read or write signal from the local μP dependent on the state of R/\overline{W} . When DS is pulled "Low" (If \overline{CS} is "Low") the LIU begins the read or write operation. |
| \overline{RDY} | \overline{DTACK} | O | Data Transfer Acknowledge: This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command. |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

XRT83SH38

8-CHANNEL T1/E1/J1 SHORT-HAUL LINE INTERFACE UNIT

6.4 Intel Mode Programmed I/O Access (Asynchronous)

If the LIU is interfaced to an Intel type μ P, then it should be configured to operate in the Intel mode. Intel type Read and Write operations are described below.

Intel Mode Read Cycle

Whenever an Intel-type μ P wishes to read the contents of a register, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[7:0].
2. While the μ P is placing this address value on the address bus, the address decoding circuitry should assert the \overline{CS} pin of the LIU, by toggling it "Low". This action enables further communication between the μ P and the LIU microprocessor interface block.
3. Toggle the ALE input pin "High". This step enables the address bus input drivers, within the microprocessor interface block of the LIU.
4. The μ P should then toggle the ALE pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
5. Next, the μ P should indicate that this current bus cycle is a Read operation by toggling the \overline{RD} input pin "Low". This action also enables the bi-directional data bus output drivers of the LIU.
6. After the μ P toggles the Read signal "Low", the LIU will toggle the \overline{RDY} output pin "Low". The LIU does this in order to inform the μ P that the data is available to be read by the μ P, and that it is ready for the next command.
7. After the μ P detects the \overline{RDY} signal and has read the data, it can terminate the Read Cycle by toggling the \overline{RD} input pin "High".

NOTE: \overline{ALE} can be tied "High" if this signal is not available.

The Intel Mode Write Cycle

Whenever an Intel type μ P wishes to write a byte or word of data into a register within the LIU, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[7:0].
2. While the μ P is placing this address value on the address bus, the address decoding circuitry should assert the \overline{CS} pin of the LIU, by toggling it "Low". This action enables further communication between the μ P and the LIU microprocessor interface block.
3. Toggle the ALE input pin "High". This step enables the address bus input drivers, within the microprocessor interface block of the LIU.
4. The μ P should then toggle the ALE pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
5. The μ P should then place the byte or word that it intends to write into the target register, on the bi-directional data bus DATA[7:0].
6. Next, the μ P should indicate that this current bus cycle is a Write operation by toggling the \overline{WR} input pin "Low". This action also enables the bi-directional data bus input drivers of the LIU.
7. After the μ P toggles the Write signal "Low", the LIU will toggle the \overline{RDY} output pin "Low". The LIU does this in order to inform the μ P that the data has been written into the internal register location, and that it is ready for the next command.

NOTE: \overline{ALE} can be tied "High" if this signal is not available.

The Intel Read and Write timing diagram is shown in [Figure 36](#). The timing specifications are shown in [Table 18](#).

FIGURE 36. INTEL μ P INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

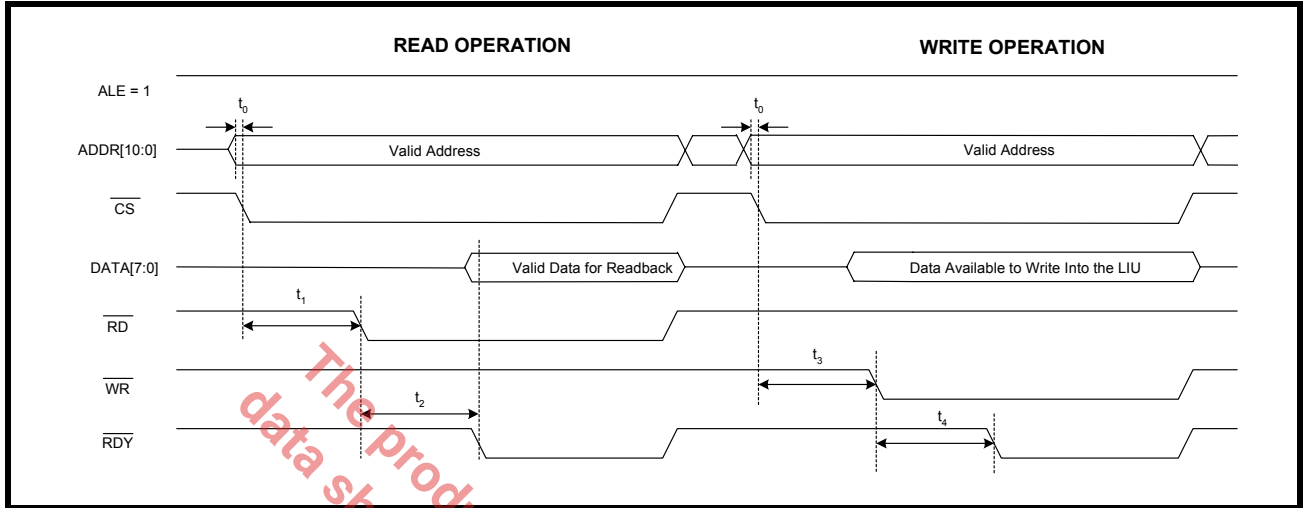


TABLE 18: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|--------|--|-----|-----|-------|
| t_0 | Valid Address to \overline{CS} Falling Edge | 0 | - | ns |
| t_1 | \overline{CS} Falling Edge to \overline{RD} Assert | 65 | - | ns |
| t_2 | \overline{RD} Assert to \overline{RDY} Assert | - | 90 | ns |
| NA | \overline{RD} Pulse Width (t_2) | 90 | - | ns |
| t_3 | \overline{CS} Falling Edge to \overline{WR} Assert | 65 | - | ns |
| t_4 | \overline{WR} Assert to \overline{RDY} Assert | - | 90 | ns |
| NA | \overline{WR} Pulse Width (t_4) | 90 | - | ns |

XRT83SH38

8-CHANNEL T1/E1/J1 SHORT-HAUL LINE INTERFACE UNIT

6.5 Motorola Mode Programmed I/O Access (Asynchronous)

If the LIU is interfaced to a Motorola type μ P, it should be configured to operate in the Motorola mode. Motorola type programmed I/O Read and Write operations are described below.

Motorola Mode Read Cycle

Whenever a Motorola type μ P wishes to read the contents of a register, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[7:0].
2. While the μ P is placing this address value on the address bus, the address decoding circuitry should assert the \overline{CS} pin of the LIU, by toggling it "Low". This action enables further communication between the μ P and the LIU microprocessor interface block.
3. The μ P should then toggle the AS pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
4. Next, the μ P should indicate that this current bus cycle is a Read operation by pulling the $\overline{R/W}$ input pin "High".
5. Toggle the DS input pin "Low". This action enables the bi-directional data bus output drivers of the LIU.
6. After the μ P toggles the DS signal "Low", the LIU will toggle the \overline{DTACK} output pin "Low". The LIU does this in order to inform the μ P that the data is available to be read by the μ P, and that it is ready for the next command.
7. After the μ P detects the \overline{DTACK} signal and has read the data, it can terminate the Read Cycle by toggling the DS input pin "High".

Motorola Mode Write Cycle

Whenever a motorola type μ P wishes to write a byte or word of data into a register within the LIU, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[7:0].
2. While the μ P is placing this address value on the address bus, the address decoding circuitry should assert the \overline{CS} pin of the LIU, by toggling it "Low". This action enables further communication between the μ P and the LIU microprocessor interface block.
3. The μ P should then toggle the AS pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
4. Next, the μ P should indicate that this current bus cycle is a Write operation by pulling the $\overline{R/W}$ input pin "Low".
5. Toggle the DS input pin "Low". This action enables the bi-directional data bus output drivers of the LIU.
6. After the μ P toggles the DS signal "Low", the LIU will toggle the \overline{DTACK} output pin "Low". The LIU does this in order to inform the μ P that the data has been written into the internal register location, and that it is ready for the next command.
7. After the μ P detects the \overline{DTACK} signal and has read the data, it can terminate the Read Cycle by toggling the DS input pin "High".

The Motorola Read and Write timing diagram is shown in **Figure 37**. The timing specifications are shown in **Table 19**.

FIGURE 37. MOTOROLA 68K μ P INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

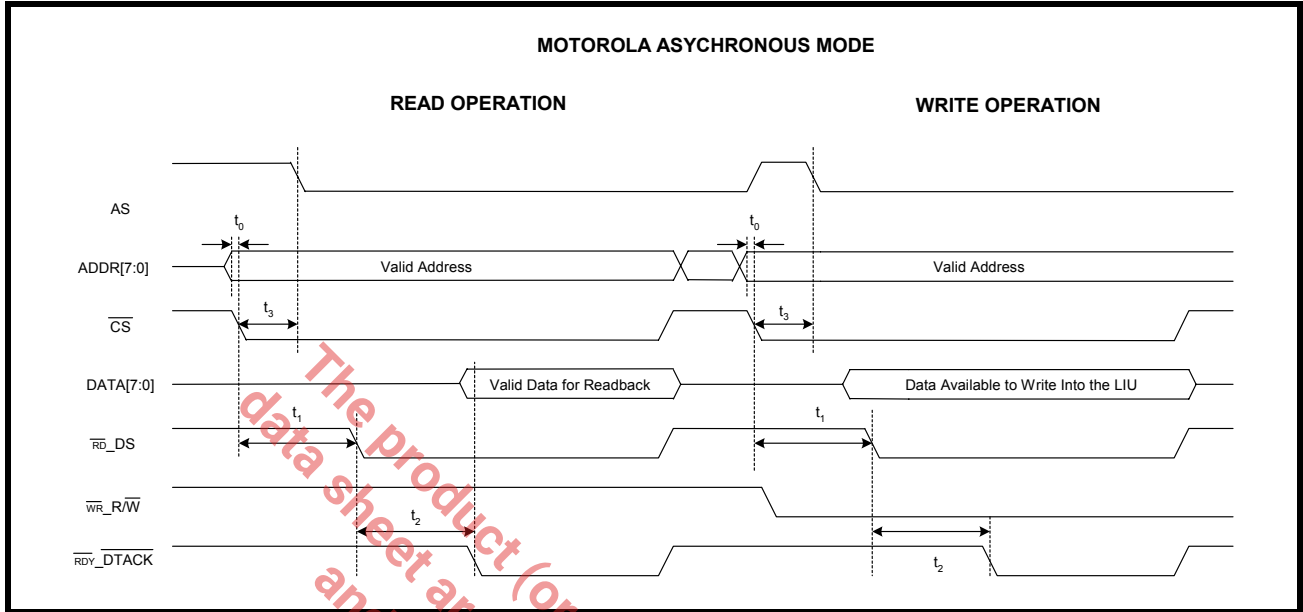


TABLE 19: MOTOROLA 68K MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|--------|---|-----|-----|-------|
| t_0 | Valid Address to \overline{CS} Falling Edge | 0 | - | ns |
| t_1 | \overline{CS} Falling Edge to \overline{DS} (Pin $\overline{RD_DS}$) Assert | 65 | - | ns |
| t_2 | DS Assert to \overline{DTACK} Assert | - | 90 | ns |
| NA | DS Pulse Width (t_2) | 90 | - | ns |
| t_3 | \overline{CS} Falling Edge to \overline{AS} (Pin ALE) Falling Edge | 0 | - | ns |

REGISTER INFORMATION

TABLE 20: MICROPROCESSOR REGISTER ADDRESS (ADDR[7:0])

| REGISTER NUMBER | ADDRESS (HEX) | FUNCTION |
|-----------------|---------------|--|
| 0 - 15 | 0x00 - 0x0F | Channel 0 Control Registers |
| 16 - 31 | 0x10 - 0x1F | Channel 1 Control Registers |
| 32 - 47 | 0x20 - 0x2F | Channel 2 Control Registers |
| 48 - 63 | 0x30 - 0x3F | Channel 3 Control Registers |
| 64 - 79 | 0x40 - 0x4F | Channel 4 Control Registers |
| 80 - 95 | 0x50 - 0x5F | Channel 5 Control Registers |
| 96 - 111 | 0x60 - 0x6F | Channel 6 Control Registers |
| 112 - 127 | 0x70 - 0x7F | Channel 7 Control Registers |
| 128 - 142 | 0x80 - 0x8E | Global Control Registers Applied to All 8 Channels |
| 192 | 0xC0 | Global Control Register Applied to All 8 Channels |
| 143 - 253 | 0x8F - 0xFD | R/W Registers Reserved for Testing (Except 0xC0h) |
| 254 | 0xFE | Device "ID" |
| 255 | 0xFF | Device "Revision ID" |

TABLE 21: MICROPROCESSOR REGISTER CHANNEL DESCRIPTION

| REG | ADDR | TYPE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--|------|------|-----------|------------|----------|----------|----------|----------|----------|----------|
| Channel 0 Control Registers (0x00 - 0x0F) | | | | | | | | | | |
| 0 | 0x00 | R/W | QRSS/PRBS | PRBS_Rx/Tx | RxON | EQC4 | EQC3 | EQC2 | EQC1 | EQC0 |
| 1 | 0x01 | R/W | RxTSEL | TxTSEL | TERSEL1 | TERSEL0 | JASEL1 | JASEL0 | JABW | FIFOS |
| 2 | 0x02 | R/W | INVQRSS | TxTEST2 | TxTEST1 | TxTEST0 | TxON | LOOP2 | LOOP1 | LOOP0 |
| 3 | 0x03 | R/W | Reserved | Reserved | CODES | RxRES1 | RxRES0 | INSBPV | INSBER | Reserved |
| 4 | 0x04 | R/W | Reserved | DMOIE | FLSIE | LCV/OFE | Reserved | AISDIE | RLOSIE | QRPDIE |
| 5 | 0x05 | RO | Reserved | DMO | FLS | LCV/OF | Reserved | AIS | RLOS | QRPD |
| 6 | 0x06 | RUR | Reserved | DMOIS | FLSIS | LCV/OFIS | Reserved | AISIS | RLOSIS | QRPDIS |
| 7 | 0x07 | RO | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| 8 | 0x08 | R/W | Reserved | 1SEG6 | 1SEG5 | 1SEG4 | 1SEG3 | 1SEG2 | 1SEG1 | 1SEG0 |
| 9 | 0x09 | R/W | Reserved | 2SEG6 | 2SEG5 | 2SEG4 | 2SEG3 | 2SEG2 | 2SEG1 | 2SEG0 |
| 10 | 0x0A | R/W | Reserved | 3SEG6 | 3SEG5 | 3SEG4 | 3SEG3 | 3SEG2 | 3SEG1 | 3SEG0 |
| 11 | 0x0B | R/W | Reserved | 4SEG6 | 4SEG5 | 4SEG4 | 4SEG3 | 4SEG2 | 4SEG1 | 4SEG0 |
| 12 | 0x0C | R/W | Reserved | 5SEG6 | 5SEG5 | 5SEG4 | 5SEG3 | 5SEG2 | 5SEG1 | 5SEG0 |
| 13 | 0x0D | R/W | Reserved | 6SEG6 | 6SEG5 | 6SEG4 | 6SEG3 | 6SEG2 | 6SEG1 | 6SEG0 |
| 14 | 0x0E | R/W | Reserved | 7SEG6 | 7SEG5 | 7SEG4 | 7SEG3 | 7SEG2 | 7SEG1 | 7SEG0 |

TABLE 21: MICROPROCESSOR REGISTER CHANNEL DESCRIPTION

| REG | ADDR | TYPE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--|------|------|----------------------|----------|----------|----------|-----------|----------|----------|----------|
| 15 | 0x0F | R/W | Reserved | 8SEG6 | 8SEG5 | 8SEG4 | 8SEG3 | 8SEG2 | 8SEG1 | 8SEG0 |
| Channel (1 - 7) Control Registers (0x10 - 0x7F) See Channel 0 | | | | | | | | | | |
| Global Control Registers for All 8 Channels | | | | | | | | | | |
| 128 | 0x80 | R/W | SR/DR | ATAOS | RCLKE | TCLKE | DATAP | Reserved | GIE | SRESET |
| 129 | 0x81 | R/W | OVFLO/LCV | CLKSEL2 | CLKSEL1 | CLKSEL0 | MCLKrate | RxMUTE | EXLOS | ICT |
| 130 | 0x82 | R/W | TxONCNTL | TERCNTL | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| 140 | 0x8C | R/W | Reserved | Reserved | Reserved | Reserved | LCVCH3 | LCVCH2 | LCVCH1 | LCVCH0 |
| 141 | 0x8D | R/W | Reserved | Reserved | Reserved | allRST | allUPDATE | BYTEsel | chUPDATE | chRST |
| 142 | 0x8E | RO | LCVCNT7 | LCVCNT6 | LCVCNT5 | LCVCNT4 | LCVCNT3 | LCVCNT2 | LCVCNT1 | LCVCNT0 |
| 192 | 0xC0 | R/W | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | E1arben |
| R/W Registers Reserved for Testing (0x8F - 0xFD) Except 0xC0h | | | | | | | | | | |
| 254 | 0xFE | RO | Device "ID" | | | | | | | |
| 255 | 0xFF | RO | Device "Revision ID" | | | | | | | |

The Product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 22: MICROPROCESSOR REGISTER 0x00H BIT DESCRIPTION

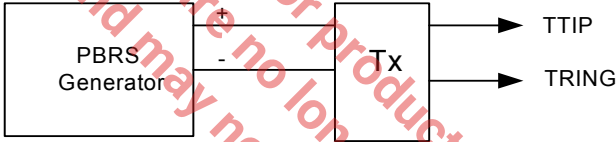
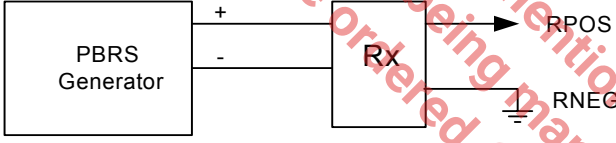
| CHANNEL 0-7 (0x00H-0x70H) | | | | |
|---------------------------|---|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | QRSS/ PRBS | QRSS/PRBS Select Bits These bits are used to select between QRSS and PRBS. 1 = QRSS 0 = PRBS | R/W | 0 |
| D6 | PRBS _{Rx/} $\overline{\text{Tx}}$ | PRBS Receive/Transmit Select: This bit is used to select where the output of the PRBS Generator is directed if PRBS generation is enabled. 0 = Normal Operation - PRBS generator is output on TTIP and TRING if PRBS generation is enabled. 1 = PRBS Generator is output on RPOS; RNEG is internally grounded, if PRBS generation is enabled. Bit 6 = "0"  Bit 6 = "1"  <i>NOTE: If PRBS generation is disabled, user should set this bit to '0' for normal operation.</i> | R/W | 0 |
| D5 | RxON | Receiver ON/OFF Upon power up, the receiver is powered OFF. RxON is used to turn the receiver ON or OFF if the hardware pin RxON is pulled "High". If the hardware pin is pulled "Low", all receivers are turned off. 0 = Receiver is Powered Off 1 = Receiver is Powered On | R/W | 0 |
| D4 | EQC4 | Equalizer Control Bits The equalizer control bits are shown in Table 23 below. | R/W | 0 |
| D3 | EQC3 | | | 0 |
| D2 | EQC2 | | | 0 |
| D1 | EQC1 | | | 0 |
| D0 | EQC0 | | | 0 |

TABLE 23: EQUALIZER CONTROL AND TRANSMIT LINE BUILD OUT

| EQC[4:0] | T1/E1 MODE/RECEIVE SENSITIVITY | TRANSMIT LBO | CABLE | CODING |
|----------|--------------------------------|-------------------------|----------|--------|
| 0x08h | T1 Short Haul/15dB | 0 to 133 feet (0.6dB) | 100Ω TP | B8ZS |
| 0x09h | T1 Short Haul/15dB | 133 to 266 feet (1.2dB) | 100Ω TP | B8ZS |
| 0x0Ah | T1 Short Haul/15dB | 266 to 399 feet (1.8dB) | 100Ω TP | B8ZS |
| 0x0Bh | T1 Short Haul/15dB | 399 to 533 feet (2.4dB) | 100Ω TP | B8ZS |
| 0x0Ch | T1 Short Haul/15dB | 533 to 655 feet (3.0dB) | 100Ω TP | B8ZS |
| 0x0Dh | T1 Short Haul/15dB | Arbitrary Pulse | 100Ω TP | B8ZS |
| 0x1Ch | E1 Short Haul/15dB | ITU G.703 | 75Ω Coax | HDB3 |
| 0x1Dh | E1 Short Haul/15dB | ITU G.703 | 120Ω TP | HDB3 |

TABLE 24: MICROPROCESSOR REGISTER 0x01H BIT DESCRIPTION

| CHANNEL 0-7 (0x01H-0x71H) | | | | |
|---------------------------|--------------------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | RxTSEL | Receive Termination Select Upon power up, the receiver is in "High" impedance. RxTSEL is used to switch between the internal termination and "High" impedance. 0 = "High" Impedance 1 = Internal Termination | R/W | 0 |
| D6 | TxTSEL | Transmit Termination Select Upon power up, the transmitter is in "High" impedance. TxTSEL is used to switch between the internal termination and "High" impedance. 0 = "High" Impedance 1 = Internal Termination | R/W | 0 |
| D5 D4 | TERSEL1 TERSEL0 | Receive Line Impedance Select TERSEL[1:0] are used to select the line impedance for T1/J1/E1. 00 = 100Ω 01 = 110Ω 10 = 75Ω 11 = 120Ω | R/W | 0 0 |
| D[3:2] | JASEL[1:0] | Jitter Attenuator Select JASEL[1:0] are used to select the jitter attenuator in the transmit or receive path. 00 = Disabled 01 = Transmit Path 10 = Receive Path 11 = Receive Path | R/W | 0 |

TABLE 24: MICROPROCESSOR REGISTER 0X01H BIT DESCRIPTION

| CHANNEL 0-7 (0X01H-0X71H) | | | | |
|---------------------------|-------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D1 | JABW | Jitter Bandwidth (E1 Mode Only, T1 is permanently set to 3Hz) The jitter bandwidth is a global setting that is applied to both the receiver and transmitter jitter attenuator. 0 = 10Hz 1 = 1.5Hz | R/W | 0 |
| D0 | FIFOS | FIFO Depth Select The FIFO depth select is used to configure the part for a 32-bit or 64-bit FIFO (within the jitter attenuator blocks). The delay of the FIFO is equal to ½ the FIFO depth. This is a global setting that is applied to both the receiver and transmitter FIFO. 0 = 32-Bit 1 = 64-Bit | R/W | 0 |

TABLE 25: MICROPROCESSOR REGISTER 0X02H BIT DESCRIPTION

| CHANNEL 0-7 (0X02H-0X72H) | | | | |
|---------------------------|-------------------------------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | INVQRSS | QRSS inversion INVQRSS is used to invert the transmit QRSS pattern set by the TxTEST[2:0] bits. By default, INVQRSS is disabled and the QRSS will be transmitted with normal polarity. 0 = Disabled 1 = Enabled | R/W | 0 |
| D6 D5 D4 | TxTEST2 TxTEST1 TxTEST0 | Test Code Pattern TxTEST[2:0] are used to select a diagnostic test pattern to the line (transmit outputs). 0XX = No Pattern 100 = Tx QRSS 101 = Tx TAOS 110 = Reserved 111 = Reserved | R/W | 0 0 0 |

TABLE 25: MICROPROCESSOR REGISTER 0X02H BIT DESCRIPTION

| CHANNEL 0-7 (0X02H-0X72H) | | | | |
|---------------------------|-------------------------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D3 | TxOn | Transmit ON/OFF Upon power up, the transmitters are powered off. This bit is used to turn the transmitter for this channel On or Off if the TxON pin is pulled "High". If the TxON pin is pulled "Low", all 8 transmitters are powered off. 0 = Transmitter is Powered OFF 1 = Transmitter is Powered ON | R/W | 0 |
| D2 D1 D0 | LOOP2 LOOP1 LOOP0 | Loopback Diagnostic Select LOOP[2:0] are used to select the loopback mode. 0XX = No Loopback 100 = Dual Loopback 101 = Analog Loopback 110 = Remote Loopback 111 = Digital Loopback | R/W | 0 0 0 |

TABLE 26: MICROPROCESSOR REGISTER 0X03H BIT DESCRIPTION

| CHANNEL 0-7 (0X03H-0X73H) | | | | |
|---------------------------|------------------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D[7:6] | Reserved | This Register Bit is Not Used. | | |
| D5 | CODES | Encoding/Decoding Select (Single Rail Mode Only) 0 = HDB3 (E1), B8ZS (T1) 1 = AMI Coding | R/W | 0 |
| D4 D3 | RxRES1 RxRES0 | Receive External Fixed Resistor RxRES[1:0] are used to select the value for a high precision external resistor to improve return loss. 00 = None 01 = 240Ω 10 = 210Ω 11 = 150Ω | R/W | 0 0 |
| D2 | INSBPV | Insert Bipolar Violation When this bit transitions from a "0" to a "1", a bipolar violation will be inserted in the transmitted QRSS/PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a "0" to this bit before writing a "1". | R/W | 0 |

TABLE 26: MICROPROCESSOR REGISTER 0x03H BIT DESCRIPTION

| CHANNEL 0-7 (0x03H-0x73H) | | | | |
|---------------------------|-----------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D1 | INSBER | Insert Bit Error When this bit transitions from a "0" to a "1", a bit error will be inserted in the transmitted QRSS/PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a "0" to this bit before writing a "1". | R/W | 0 |
| D0 | Resereved | | | |

TABLE 27: MICROPROCESSOR REGISTER 0x04H BIT DESCRIPTION

| CHANNEL 0-7(0x04H-0x74H) | | | | |
|--------------------------|----------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Reserved | This Register Bit is Not Used. | | |
| D6 | DMOIE | Digital Monitor Output Interrupt Enable 0 = Masks the DMO function 1 = Enables Interrupt Generation | R/W | 0 |
| D5 | FLSIE | FIFO Limit Status Interrupt Enable 0 = Masks the FLS function 1 = Enables Interrupt Generation | R/W | 0 |
| D4 | LCV/OFIE | Line Code Violation / Counter Overflow Interrupt Enable 0 = Masks the LCV/OF function 1 = Enables Interrupt Generation | R/W | 0 |
| D3 | Reserved | This Register Bit is Not Used. | | |
| D2 | AISIE | Alarm Indication Signal Interrupt Enable 0 = Masks the AIS function 1 = Enables Interrupt Generation | R/W | 0 |
| D1 | RLOSIE | Receiver Loss of Signal Interrupt Enable 0 = Masks the RLOS function 1 = Enables Interrupt Generation | R/W | 0 |
| D0 | QRPDIE | Quasi Random Signal Source Interrupt Enable 0 = Masks the QRPD function 1 = Enables Interrupt Generation | R/W | 0 |

NOTE: The GIE bit in the global register 0x80h must be set to "1" in addition to the individual register bits to enable the interrupt pin.

TABLE 28: MICROPROCESSOR REGISTER 0X05H BIT DESCRIPTION

| CHANNEL 0-7 (0X05H-0X75H) | | | | |
|---------------------------|----------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Reserved | This Register Bit is Not Used. | | |
| D6 | DMO | Digital Monitor Output The digital monitor output is always active regardless if the interrupt generation is disabled. This bit indicates the DMO activity. An interrupt will not occur unless the DMOIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0x80h. 0 = No Alarm 1 = Transmit output driver has failures | RO | 0 |
| D5 | FLS | FIFO Limit Status The FIFO limit status is always active regardless if the interrupt generation is disabled. This bit indicates whether the RD/WR pointers are within 3-Bits. An interrupt will not occur unless the FLSIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0x80h. 0 = No Alarm 1 = RD/WR FIFO pointers are within ±3-Bits | RO | 0 |
| D4 | LCV/OF | Line Code Violation / Counter Overflow This bit serves a dual purpose. By default, this bit monitors the line code violation activity. However, if bit 7 in register 0x81h is set to a "1", this bit monitors the overflow status of the internal LCV counter. An interrupt will not occur unless the LCV/OFIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0x80h. 0 = No Alarm 1 = A line code violation, bipolar violation, or excessive zeros has occurred | RO | 0 |
| D3 | Reserved | This Register Bit is Not Used. | | |
| D2 | AISD | Alarm Indication Signal The alarm indication signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the AIS activity. An interrupt will not occur unless the AISIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0x80h. 0 = No Alarm 1 = An all ones signal is detected | RO | 0 |

8-CHANNEL T1/E1/J1 SHORT-HAUL LINE INTERFACE UNIT

NOTE: The GIE bit in the global register 0x80h must be set to "1" in addition to the individual register bits to enable the interrupt pin.

TABLE 28: MICROPROCESSOR REGISTER 0X05H BIT DESCRIPTION

| CHANNEL 0-7 (0X05H-0X75H) | | | | |
|---------------------------|------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D1 | RLOS | <p>Receiver Loss of Signal</p> <p>The receiver loss of signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the RLOS activity. An interrupt will not occur unless the RLOSIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0x80h.</p> <p>0 = No Alarm 1 = An RLOS condition is present</p> | RO | 0 |
| D0 | QRPD | <p>Quasi Random Pattern Detection</p> <p>The quasi random pattern detection is always active regardless if the interrupt generation is disabled. This bit indicates that a QRPD has been detected. An interrupt will not occur unless the QRPDIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0x80h.</p> <p>0 = No Alarm 1 = A QRP is detected</p> | RO | 0 |

TABLE 29: MICROPROCESSOR REGISTER 0X06H BIT DESCRIPTION

| CHANNEL 0-7 (0X06H-0X76H) | | | | |
|---------------------------|----------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Reserved | This Register Bit is Not Used. | | |
| D6 | DMOIS | <p>Digital Monitor Output Status</p> <p>0 = No change 1 = Change in status occurred</p> | RUR | 0 |
| D5 | FLSIS | <p>FIFO Limit Status</p> <p>0 = No change 1 = Change in status occurred</p> | RUR | 0 |
| D4 | LCV/OFIS | <p>Line Code Violation / Overflow Status</p> <p>0 = No change 1 = Change in status occurred</p> | RUR | 0 |
| D3 | Reserved | This Register Bit is Not Used. | | |
| D2 | AISDIS | <p>Alarm Indication Signal Status</p> <p>0 = No change 1 = Change in status occurred</p> | RUR | 0 |

TABLE 29: MICROPROCESSOR REGISTER 0x06H BIT DESCRIPTION

| CHANNEL 0-7 (0x06H-0x76H) | | | | |
|---------------------------|-------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D1 | RLOSI | Receiver Loss of Signal Status 0 = No change 1 = Change in status occurred | RUR | 0 |
| D0 | QRDIS | Quasi Random Pattern Detection Status 0 = No change 1 = Change in status occurred | RUR | 0 |

NOTE: Any change in status will generate an interrupt (if enabled in channel register 0x04h and GIE is set to "1" in the global register 0x80h). The status registers are reset upon read (RUR).

TABLE 30: MICROPROCESSOR REGISTER 0x08H BIT DESCRIPTION

| CHANNEL 0-7 (0x08H-0x78H) | | | | |
|---------------------------|----------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Reserved | This Register Bit is Not Used | X | 0 |
| D6 | 1SEG6 | Arbitrary Pulse Generation The transmit output pulse is divided into 8 individual segments. This register is used to program the first segment which corresponds to the overshoot of the pulse amplitude. There are four segments for the top portion of the pulse and four segments for the bottom portion of the pulse. Segment number 5 corresponds to the undershoot of the pulse. The MSB of each segment is the sign bit. Bit 6 = 0 = Negative Direction Bit 6 = 1 = Positive Direction | R/W | 0 |
| D5 | 1SEG5 | | | 0 |
| D4 | 1SEG4 | | | 0 |
| D3 | 1SEG3 | | | 0 |
| D2 | 1SEG2 | | | 0 |
| D1 | 1SEG1 | | | 0 |
| D0 | 1SEG0 | | | 0 |

TABLE 31: MICROPROCESSOR REGISTER 0x09H BIT DESCRIPTION

| CHANNEL 0-7 (0x09H-0x79H) | | | | |
|---------------------------|-----------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Reserved | This Register Bit is Not Used | X | 0 |
| D[6:0] | 2SEG[6:0] | Segment Number Two, Same Description as Register 0x08h | R/W | |

TABLE 32: MICROPROCESSOR REGISTER 0x0Ah BIT DESCRIPTION

| CHANNEL 0-7 (0x0Ah-0x7Ah) | | | | |
|---------------------------|-----------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Reserved | This Register Bit is Not Used | X | 0 |
| D[6:0] | 3SEG[6:0] | Segment Number Three, Same Description as Register 0x08h | R/W | |

TABLE 33: MICROPROCESSOR REGISTER 0x0Bh BIT DESCRIPTION

| CHANNEL 0-7 (0x0Bh-0x7Bh) | | | | |
|---------------------------|-----------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Reserved | This Register Bit is Not Used | X | 0 |
| D[6:0] | 4SEG[6:0] | Segment Number Four, Same Description as Register 0x08h | R/W | |

TABLE 34: MICROPROCESSOR REGISTER 0x0Ch BIT DESCRIPTION

| CHANNEL 0-7 (0x0Ch-0x7Ch) | | | | |
|---------------------------|-----------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Reserved | This Register Bit is Not Used | X | 0 |
| D[6:0] | 5SEG[6:0] | Segment Number Five, Same Description as Register 0x08h | R/W | |

TABLE 35: MICROPROCESSOR REGISTER 0x0Dh BIT DESCRIPTION

| CHANNEL 0-7 (0x0Dh-0x7Dh) | | | | |
|---------------------------|-----------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Reserved | This Register Bit is Not Used | X | 0 |
| D[6:0] | 6SEG[6:0] | Segment Number Six, Same Description as Register 0x08h | R/W | |

TABLE 36: MICROPROCESSOR REGISTER 0x0EH BIT DESCRIPTION

| CHANNEL 0-7 (0x0EH-0x7EH) | | | | |
|---------------------------|-----------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Reserved | This Register Bit is Not Used | X | 0 |
| D[6:0] | 7SEG[6:0] | Segment Number Seven, Same Description as Register 0x08h | R/W | |

TABLE 37: MICROPROCESSOR REGISTER 0x0FH BIT DESCRIPTION

| CHANNEL 0-7 (0x0FH-0x7FH) | | | | |
|---------------------------|-----------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Reserved | This Register Bit is Not Used | X | 0 |
| D[6:0] | 8SEG[6:0] | Segment Number Eight, Same Description as Register 0x08h | R/W | |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

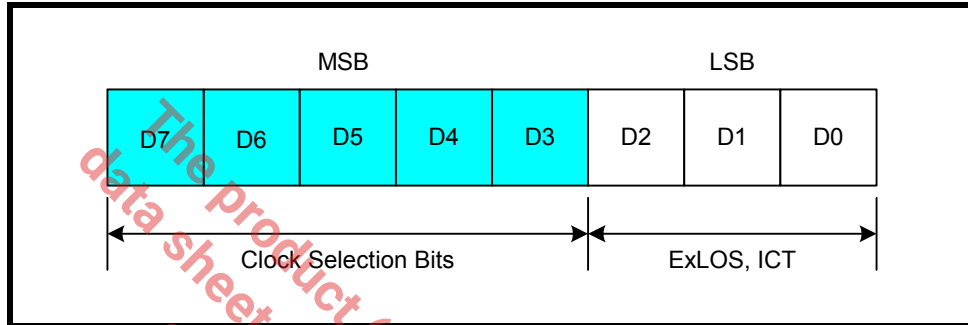
TABLE 38: MICROPROCESSOR REGISTER 0X80H, BIT DESCRIPTION

| REGISTER ADDRESS 0x80H | NAME | FUNCTION | REGISTER TYPE | RESET VALUE |
|---------------------------|----------|--|---------------|-------------|
| BIT # | | | | |
| D7 | SR/DR | Single-rail/Dual-rail Select: Writing a "1" to this bit configures all 8 channels in the XRT83SH38 to operate in the Single-rail mode. Writing a "0" configures the XRT83SH38 to operate in Dual-rail mode. | R/W | 0 |
| D6 | ATAOS | Automatic Transmit All Ones Upon RLOS: Writing a "1" to this bit enables the automatic transmission of All "Ones" data to the line for the channel that detects an RLOS condition. Writing a "0" disables this feature. | R/W | 0 |
| D5 | RCLKE | Receive Clock Edge: Writing a "1" to this bit selects receive output data of all channels to be updated on the negative edge of RCLK. Writing a "0" selects data to be updated on the positive edge of RCLK. | R/W | 0 |
| D4 | TCLKE | Transmit Clock Edge: Writing a "0" to this bit selects transmit data at TPOS_n/TDATA_n and TNEG_n/CODES_n of all channels to be sampled on the falling edge of TCLK_n. Writing a "1" selects the rising edge of the TCLK_n for sampling. | R/W | 0 |
| D3 | DATAP | DATA Polarity: Writing a "0" to this bit selects transmit input and receive output data of all channels to be active "High". Writing a "1" selects an active "Low" state. | R/W | 0 |
| D2 | Reserved | | | 0 |
| D1 | GIE | Global Interrupt Enable: Writing a "1" to this bit globally enables interrupt generation for all channels. Writing a "0" disables interrupt generation. | R/W | 0 |
| D0 | SRESET | Software Reset μP Registers: Writing a "1" to this bit longer than 10 μ s initiates a device reset through the microprocessor interface. All internal circuits are placed in the reset state with this bit set to a "1" except the microprocessor register bits. | R/W | 0 |

CLOCK SELECT REGISTER

The input clock source is used to generate all the necessary clock references internally to the LIU. The microprocessor timing is derived from a PLL output which is chosen by programming the Clock Select Bits and the Master Clock Rate in register 0x81h. Therefore, if the clock selection bits or the MCLRATE bit are being programmed, the frequency of the PLL output will be adjusted accordingly. During this adjustment, it is important to "Not" write to any other bit location within the same register while selecting the input/output clock frequency. For best results, register 0x81h can be broken down into two sub-registers with the MSB being bits D[7:3] and the LSB being bits D[2:0] as shown in **Figure 38**. Note: Bit D[7] is a reserved bit.

FIGURE 38. REGISTER 0X81H SUB REGISTERS



Programming Examples:

Example 1: Changing bits D[7:3]

If bits D[7:3] are the only values within the register that will change in a WRITE process, the microprocessor only needs to initiate ONE write operation.

Example 2: Changing bits D[2:0]

If bits D[2:0] are the only values within the register that will change in a WRITE process, the microprocessor only needs to initiate ONE write operation.

Example 3: Changing bits within the MSB and LSB

In this scenario, one must initiate TWO write operations such that the MSB and LSB do not change within ONE write cycle. It is recommended that the MSB and LSB be treated as two independent sub-registers. One can either change the clock selection (MSB) and then change bits D[2:0] (LSB) on the SECOND write, or vice-versa. No order or sequence is necessary.

TABLE 39: MICROPROCESSOR REGISTER 0x81H, BIT DESCRIPTION

| REGISTER ADDRESS 0x81H | NAME | FUNCTION | REGISTER TYPE | RESET VALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|------------|---|---------------|-------------|----------|-------------|---------|----------|-------------|------|------|---|---|---|---|------|------|------|---|---|---|---|------|------|------|---|---|---|---|------|------|------|---|---|---|---|------|------|------|---|---|---|---|------|------|------|---|---|---|---|------|---|---|---|---|---|---|------|---|---|---|---|---|---|------|----|---|---|---|---|---|------|----|---|---|---|---|---|------|----|---|---|---|---|---|------|----|---|---|---|---|---|------|----|---|---|---|---|---|------|----|---|---|---|---|---|------|-----|---|---|---|---|---|------|-----|---|---|---|---|---|------|-----|---|---|---|---|---|------|-----|---|---|---|---|---|------|-----|---|
| BIT # | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D7 | Reserved | | R/W | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D6 | CLKSEL2 | <p>Clock Select Inputs for Master Clock Synthesizer bit 2: In Host mode, CLKSEL[2:0] are input signals to a programmable frequency synthesizer that can be used to generate a master clock from an external accurate clock source according to the following table;</p> <table border="1"> <thead> <tr> <th>MCLKE1 kHz</th> <th>MCLKT1 kHz</th> <th>CLKSEL2</th> <th>CLKSEL1</th> <th>CLKSEL0</th> <th>MCLKRATE</th> <th>CLKOUT/ kHz</th> </tr> </thead> <tbody> <tr><td>2048</td><td>2048</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2048</td></tr> <tr><td>2048</td><td>2048</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1544</td></tr> <tr><td>2048</td><td>1544</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2048</td></tr> <tr><td>1544</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1544</td></tr> <tr><td>1544</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2048</td></tr> <tr><td>2048</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1544</td></tr> <tr><td>8</td><td>X</td><td>0</td><td>1</td><td>0</td><td>0</td><td>2048</td></tr> <tr><td>8</td><td>X</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1544</td></tr> <tr><td>16</td><td>X</td><td>0</td><td>1</td><td>1</td><td>0</td><td>2048</td></tr> <tr><td>16</td><td>X</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1544</td></tr> <tr><td>56</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2048</td></tr> <tr><td>56</td><td>X</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1544</td></tr> <tr><td>64</td><td>X</td><td>1</td><td>0</td><td>0</td><td>0</td><td>2048</td></tr> <tr><td>64</td><td>X</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1544</td></tr> <tr><td>128</td><td>X</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2048</td></tr> <tr><td>128</td><td>X</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1544</td></tr> <tr><td>256</td><td>X</td><td>1</td><td>1</td><td>1</td><td>0</td><td>2048</td></tr> <tr><td>256</td><td>X</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1544</td></tr> </tbody> </table> <p>In Hardware mode, the state of these signals are ignored and the master frequency PLL is controlled by the corresponding Hardware pins.</p> | MCLKE1 kHz | MCLKT1 kHz | CLKSEL2 | CLKSEL1 | CLKSEL0 | MCLKRATE | CLKOUT/ kHz | 2048 | 2048 | 0 | 0 | 0 | 0 | 2048 | 2048 | 2048 | 0 | 0 | 0 | 1 | 1544 | 2048 | 1544 | 0 | 0 | 0 | 0 | 2048 | 1544 | 1544 | 0 | 0 | 1 | 1 | 1544 | 1544 | 1544 | 0 | 0 | 1 | 0 | 2048 | 2048 | 1544 | 0 | 0 | 1 | 1 | 1544 | 8 | X | 0 | 1 | 0 | 0 | 2048 | 8 | X | 0 | 1 | 0 | 1 | 1544 | 16 | X | 0 | 1 | 1 | 0 | 2048 | 16 | X | 0 | 1 | 1 | 1 | 1544 | 56 | X | 0 | 0 | 0 | 0 | 2048 | 56 | X | 1 | 0 | 0 | 1 | 1544 | 64 | X | 1 | 0 | 0 | 0 | 2048 | 64 | X | 1 | 0 | 1 | 1 | 1544 | 128 | X | 1 | 1 | 0 | 0 | 2048 | 128 | X | 1 | 1 | 0 | 1 | 1544 | 256 | X | 1 | 1 | 1 | 0 | 2048 | 256 | X | 1 | 1 | 1 | 1 | 1544 | R/W | 0 |
| MCLKE1 kHz | MCLKT1 kHz | CLKSEL2 | CLKSEL1 | CLKSEL0 | MCLKRATE | CLKOUT/ kHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2048 | 2048 | 0 | 0 | 0 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2048 | 2048 | 0 | 0 | 0 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2048 | 1544 | 0 | 0 | 0 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1544 | 1544 | 0 | 0 | 1 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1544 | 1544 | 0 | 0 | 1 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2048 | 1544 | 0 | 0 | 1 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | X | 0 | 1 | 0 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | X | 0 | 1 | 0 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 16 | X | 0 | 1 | 1 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 16 | X | 0 | 1 | 1 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 56 | X | 0 | 0 | 0 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 56 | X | 1 | 0 | 0 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 64 | X | 1 | 0 | 0 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 64 | X | 1 | 0 | 1 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 128 | X | 1 | 1 | 0 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 128 | X | 1 | 1 | 0 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 256 | X | 1 | 1 | 1 | 0 | 2048 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 256 | X | 1 | 1 | 1 | 1 | 1544 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D5 | CLKSEL1 | <p>Clock Select inputs for Master Clock Synthesizer bit 1: See description of bit D6 for function of this bit.</p> | R/W | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D4 | CLKSEL0 | <p>Clock Select inputs for Master Clock Synthesizer bit 0: See description of bit D6 for function of this bit.</p> | R/W | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | MCLKRATE | <p>Master clock Rate Select: The state of this bit programs the Master Clock Synthesizer to generate the T1/J1 or E1 clock. The Master Clock Synthesizer will generate the E1 clock when MCLKRATE = "0", and the T1/J1 clock when MCLKRATE = "1".</p> | R/W | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D2 | RXMUTE | <p>Receive Output Mute: Writing a "1" to this bit, mutes receive outputs at RPOS/RDATA and RNEG/LCV pins to a "0" state for any channel that detects an RLOS condition. NOTE: RCLK is not muted.</p> | R/W | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

TABLE 39: MICROPROCESSOR REGISTER 0X81H, BIT DESCRIPTION

| | | | | |
|----|-------|---|-----|---|
| D1 | EXLOS | Extended LOS: Writing a “1” to this bit extends the number of zeros at the receive input of each channel before RLOS is declared to 4096 bits. Writing a “0” reverts to the normal mode (175+75 bits for T1 and 32 bits for E1). | R/W | 0 |
| D0 | ICT | In-Circuit-Testing: Writing a “1” to this bit configures all the output pins of the chip in high impedance mode for In-Circuit-Testing. Setting the ICT bit to “1” is equivalent to connecting the Hardware ICT pin 88 to ground. | R/W | 0 |

TABLE 40: MICROPROCESSOR REGISTER 0X82H BIT DESCRIPTION

| GLOBAL REGISTER (0X82H) | | | | |
|-------------------------|----------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | TxONCNTL | Transmit On Control 0 = Control of receive termination is set; if in Hardware mode, by RXTSEL Pins If in Host mode by the RXTsel bit 0 = Control of Transmitter is set ; if Hardware mode, by TxON pin if Host mode, by TxON bit 1 = Control of transmitter on, is determined by the individual channel TxOn bits | R/W | 0 |
| D6 | TERCNTL | Receive Termination Select Control This bit sets the LIU to control the RXTSEL function with either the individual channel register bit or the global hardware pin. 0 = Control of the receive termination is set by Hardware-Host bit or Hardware pin and individual software 1 = Control of the receive termination is set to the hardware pin | R/W | 0 |
| D[5:0] | Reserved | These Register Bits are Not Used | | |

TABLE 41: MICROPROCESSOR REGISTER 0x8Ch BIT DESCRIPTION

| GLOBAL REGISTER (0x8Ch) | | | | |
|-------------------------|----------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D[7:4] | Reserved | Tese Register Bits are Not Used | R/W | 0 |
| D3 | LCVCH3 | Line Code Violation Counter Select These bits are used to select which channel is to be addressed for reading the contents in register 0x8Eh. It is also used to address the counter for a given channel when performing an update or reset on a per channel basis. By default, Channel 0 is selected. 0000 = None 0001 = Channel 0 0010 = Channel 1 0011 = Channel 2 0100 = Channel 3 0101 = Channel 4 0110 = Channel 5 0111 = Channel 6 1000 = Channel 7 | R/W | 0 |
| D2 | LCVCH2 | | | 0 |
| D1 | LCVCH1 | | | 0 |
| D0 | LCVCH0 | | | 0 |
| | | | | |

TABLE 42: MICROPROCESSOR REGISTER 0x8Dh BIT DESCRIPTION

| GLOBAL REGISTER (0x8Dh) | | | | |
|-------------------------|-----------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Reserved | This Register Bit is Not Used | R/W | 0 |
| D6 | Reserved | This Register Bit is Not Used | R/W | 0 |
| D5 | Reserved | This Register Bit is Not Used | R/W | 0 |
| D4 | allRST | LCV Counter Reset for All Channels This bit is used to reset all internal LCV counters to their default state 0000h. This bit must be set to "1" for 1 μ S. 0 = Normal Operation 1 = Resets all Counters | R/W | 0 |
| D3 | allUPDATE | LCV Counter Update for All Channels This bit is used to latch the contents of all 8 counters into holding registers so that the value of each counter can be read. The channel is addressed by using bits D[3:0] in register 0x8Ch. 0 = Normal Operation 1 = Updates all Counters | R/W | 0 |

TABLE 42: MICROPROCESSOR REGISTER 0x8DH BIT DESCRIPTION

| GLOBAL REGISTER (0x8DH) | | | | |
|-------------------------|----------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D2 | BYTEsel | <p>LCV Counter Byte Select</p> <p>This bit is used to select the MSB or LSB for Reading the contents of the LCV counter for a given channel. The channel is addressed by using bits D[3:0] in register 0x8Ch. By default, the LSB byte is selected.</p> <p>0 = Low Byte 1 = High Byte</p> | R/W | 0 |
| D1 | chUPDATE | <p>LCV Counter Update Per Channel</p> <p>This bit is used to latch the contents of the counter for a given channel into a holding register so that the value of the counter can be read. The channel is addressed by using bits D[3:0] in register 0x8Ch.</p> <p>0 = Normal Operation 1 = Updates the Selected Channel</p> | R/W | 0 |
| D0 | chRESET | <p>LCV Counter Reset Per Channel</p> <p>This bit is used to reset the LCV counter of a given channel to its default state 0000h. The channel is addressed by using bits D[3:0] in register 0x8Ch. This bit must be set to "1" for 1µS.</p> <p>0 = Normal Operation 1 = Resets the Selected Channel</p> | R/W | 0 |

TABLE 43: MICROPROCESSOR REGISTER 0x8EH BIT DESCRIPTION

| GLOBAL REGISTER (0x8EH) | | | | |
|-------------------------|---------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | LCVCNT7 | <p>Line Code Violation Byte Contents</p> <p>These bits contain the LCV counter contents of the Byte selected by bit D2 in register 0x8Dh for a given channel. The channel is addressed by using bits D[3:0] in register 0x8Ch. By default, the contents contain the LSB, however no channel is selected..</p> | R/W | 0 |
| D6 | LCVCNT6 | | | 0 |
| D5 | LCVCNT5 | | | 0 |
| D4 | LCVCNT4 | | | 0 |
| D3 | LCVCNT3 | | | 0 |
| D2 | LCVCNT2 | | | 0 |
| D1 | LCVCNT1 | | | 0 |
| D0 | LCVCNT0 | | | 0 |

TABLE 44: MICROPROCESSOR REGISTER 0xC0H BIT DESCRIPTION

| GLOBAL REGISTER (0xC0H) | | | | |
|-------------------------|----------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D[7:1] | Reserved | These register bits are not used. | R/W | 0 |
| D0 | E1Arben | <p>E1 Arbitrary Pulse Enable</p> <p>This bit is used to enable the Arbitrary Pulse Generators for shaping the transmit pulse shape when E1 mode is selected. If this bit is set to "1", all 8 channels will be configured for the Arbitrary Mode. However, each channel is individually controlled by programming the channel registers 0xn8 through 0xnF, where n is the number of the channel.</p> <p>"0" = Disabled (Normal E1 Pulse Shape ITU G.703)</p> <p>"1" = Arbitrary Pulse Enabled</p> | R/W | 0 |

TABLE 45: MICROPROCESSOR REGISTER 0xFEH BIT DESCRIPTION

| DEVICE "ID" REGISTER (0xFEH) | | | | |
|------------------------------|-------------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Device "ID" | The device "ID" of the XRT83SH38 short haul LIU is 0xF5h. Along with the revision "ID", the device "ID" is used to enable software to identify the silicon adding flexibility for system control and debug. | RO | 1 |
| D6 | | | | 1 |
| D5 | | | | 1 |
| D4 | | | | 1 |
| D3 | | | | 0 |
| D2 | | | | 1 |
| D1 | | | | 0 |
| D0 | | | | 1 |

TABLE 46: MICROPROCESSOR REGISTER 0xFFH BIT DESCRIPTION

| REVISION "ID" REGISTER (0xFFH) | | | | |
|--------------------------------|---------------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Revision "ID" | The revision "ID" of the XRT83SH38 LIU is used to enable software to identify which revision of silicon is currently being tested. The revision "ID" for the first revision of silicon will be 0x01h. | RO | 0 |
| D6 | | | | 0 |
| D5 | | | | 0 |
| D4 | | | | 0 |
| D3 | | | | 0 |
| D2 | | | | 0 |
| D1 | | | | 0 |
| D0 | | | | 1 |

ELECTRICAL CHARACTERISTICS

TABLE 47: ABSOLUTE MAXIMUM RATINGS

| | |
|-----------------------|-----------------|
| Storage Temperature | -65°C to +150°C |
| Operating Temperature | -40°C to +85°C |
| Supply Voltage | -0.5V to +3.8V |
| V _{in} | -0.5V to +5.5V |

TABLE 48: DC DIGITAL INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

| VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED | | | | | |
|--|-----------------|------|-----|------|-------|
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
| Power Supply Voltage | VDD | 3.13 | 3.3 | 3.46 | V |
| Input High Voltage | V _{IH} | 2.0 | - | 5.0 | V |
| Input Low Voltage | V _{IL} | -0.5 | - | 0.8 | V |
| Output High Voltage I _{OH} =2.0mA | V _{OH} | 2.4 | - | | V |
| Output Low Voltage I _{OL} =2.0mA | V _{OL} | | - | 0.4 | V |
| Input Leakage Current | I _L | - | - | ±10 | µA |
| Input Capacitance | C _I | | 5.0 | | pF |
| Output Lead Capacitance | C _L | | - | 25 | pF |

NOTE: Input leakage current excludes pins that are internally pulled "Low" or "High"

TABLE 49: AC ELECTRICAL CHARACTERISTICS

| VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED | | | | | |
|--|--------|-----|-----|-----|-------|
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
| MCLKin Clock Duty Cycle | | 40 | - | 60 | % |
| MCLKin Clock Tolerance | | - | ±50 | - | ppm |

TABLE 50: POWER CONSUMPTION

| VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED | | | | | | | | |
|--|----------------|-----------|----------|-------------|-------|-----|------|----------------|
| MODE | SUPPLY VOLTAGE | IMPEDANCE | RECEIVER | TRANSMITTER | TYP | MAX | UNIT | TEST CONDITION |
| E1 | 3.3V | 75Ω | 1:1 | 1:2 | 1.059 | - | W | 50% ones |
| | | | | | 1.422 | | | 100% ones |
| E1 | 3.3V | 120Ω | 1:1 | 1:2 | 0.974 | - | W | 50% ones |
| | | | | | 1.264 | | | 100% ones |
| T1 | 3.3V | 100Ω | 1:1 | 1:2 | 1.465 | - | W | 50% ones |
| | | | | | 1.904 | | | 100% ones |

TABLE 51: E1 RECEIVER ELECTRICAL CHARACTERISTICS

| VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED | | | | | |
|--|------|-----|------|--------------------|---|
| PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITION |
| Receiver Loss of Signal | | | | | |
| Number of consecutive zeros before RLOS is declared | - | 32 | - | | |
| Input signal level at RLOS | 15 | 24 | - | dB | Cable attenuation @ 1024kHz |
| RLOS clear | 12.5 | - | - | % ones | ITU-G.775, ETSI 300 233 |
| Receiver Sensitivity (short haul with cable loss) | 11 | - | - | dB | With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω with -18dB interference signal added. |
| Input Impedance | - | 13 | - | kΩ | |
| Input Jitter Tolerance | | | | | |
| 1Hz | 37 | - | - | U _{I p-p} | ITU-G.823 |
| 10kHz - 100kHz | 0.2 | - | - | U _{I p-p} | |
| Recovered Clock Jitter | | | | | |
| Transfer Corner Frequency | - | 36 | - | kHz | ITU-G.736 |
| Peaking Amplitude | - | - | -0.5 | dB | |
| Jitter Attenuator Corner Frequency | | | | | |
| JABW = 0 | - | 10 | - | Hz | ITU-G.736 |
| JABW = 1 | - | 1.5 | - | Hz | |
| Return Loss | | | | | |
| 51kHz - 102kHz | 14 | - | - | dB | ITU-G.703 |
| 102kHz - 2048kHz | 20 | - | - | dB | |
| 2048kHz - 3072kHz | 16 | - | - | dB | |

TABLE 52: T1 RECEIVER ELECTRICAL CHARACTERISTICS

| VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED | | | | | |
|--|------|-----|-----|-------------------------------|--|
| PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITION |
| Receiver Loss of Signal | | | | | |
| Number of consecutive zeros before RLOS is declared | 160 | 175 | 190 | | |
| Input signal level at RLOS | 15 | 24 | - | dB | Cable attenuation @ 772kHz |
| RLOS clear | 12.5 | - | - | % ones | ITU-G.775, ETSI 300 233 |
| Receiver Sensitivity (short haul with cable loss) | 12 | - | - | dB | With nominal pulse amplitude of 3.0V for 100Ω termination. |
| Input Impedance | - | 13 | - | kΩ | |
| Input Jitter Tolerance | | | | | |
| 1Hz | 138 | - | - | U _I _{p-p} | AT&T Pub 62411 |
| 10kHz - 100kHz | 0.4 | - | - | U _I _{p-p} | |
| Recovered Clock Jitter | | | | | |
| Transfer Corner Frequency | - | 9.8 | - | kHz | TR-TSY-000499 |
| Peaking Amplitude | - | - | 0.1 | dB | |
| Jitter Attenuator Corner Frequency | - | 6 | - | Hz | AT&T Pub 62411 |
| Return Loss | | | | | |
| 51kHz - 102kHz | - | 20 | - | dB | |
| 102kHz - 2048kHz | - | 25 | - | dB | |
| 2048kHz - 3072kHz | - | 25 | - | dB | |

The Product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 53: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

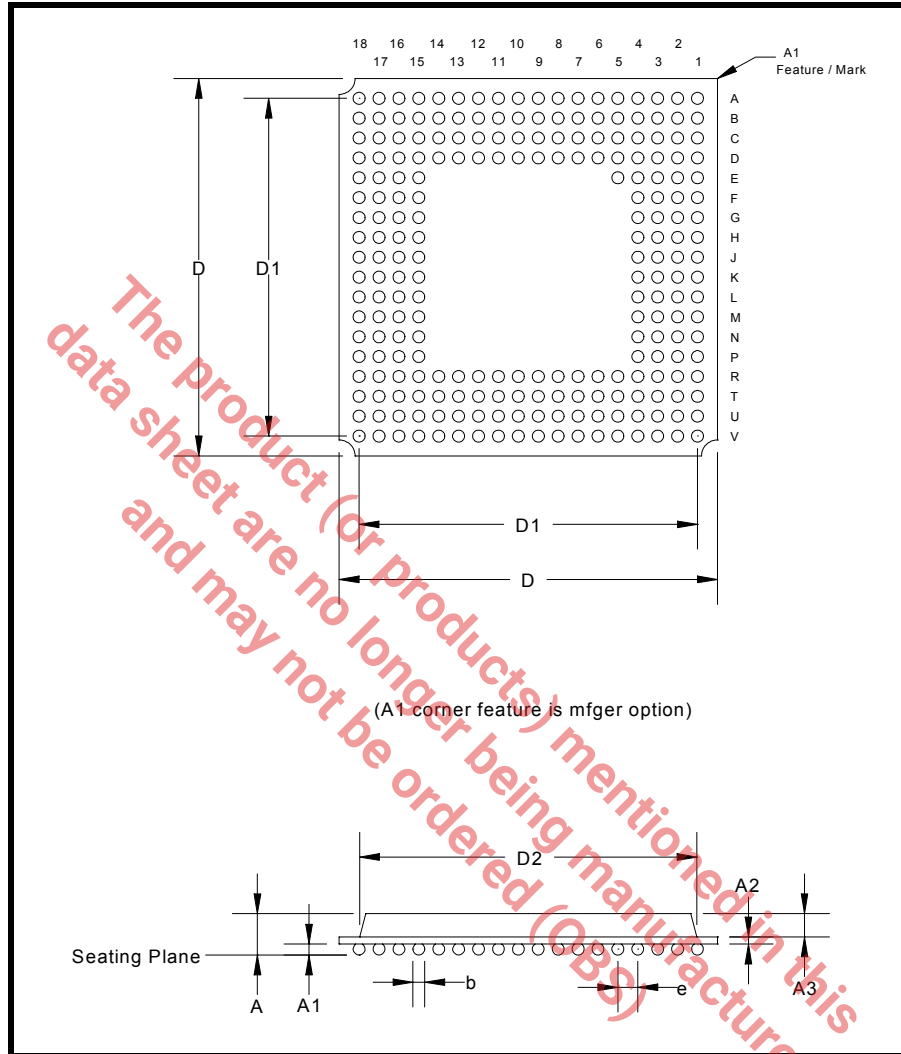
| VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED | | | | | |
|--|------|-------|------|--------------------|--|
| PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITION |
| AMI Output Pulse Amplitude | | | | | |
| 75Ω | 2.13 | 2.37 | 2.60 | V | 1:2 Transformer |
| 120Ω | 2.70 | 3.00 | 3.30 | V | |
| Output Pulse Width | 224 | 244 | 264 | ns | |
| Output Pulse Width Ratio | 0.95 | - | 1.05 | | ITU-G.703 |
| Output Pulse Amplitude Ratio | 0.95 | - | 1.05 | | ITU-G.703 |
| Jitter Added by the Transmitter Output | - | 0.025 | 0.05 | U _{I p-p} | Broad Band with jitter free TCLK applied to the input. |
| Output Return Loss | | | | | ETSI 300 166, CHPTT |
| 51kHz - 102kHz | 8 | - | - | dB | |
| 102kHz - 2048kHz | 14 | - | - | dB | |
| 2048kHz - 3072kHz | 10 | - | - | dB | |

TABLE 54: T1 TRANSMITTER ELECTRICAL CHARACTERISTICS

| VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED | | | | | |
|--|-----|-------|------|--------------------|--|
| PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITION |
| AMI Output Pulse Amplitude | 2.4 | 3.0 | 3.6 | V | 1:2 Transformer measured at DSX-1 |
| Output Pulse Width | 338 | 350 | 362 | ns | ANSI T1.102 |
| Output Pulse Width Imbalance | - | - | 20 | | ANSI T1.102 |
| Output Pulse Amplitude Imbalance | - | - | ±200 | mV | ANSI T1.102 |
| Jitter Added by the Transmitter Output | - | 0.025 | 0.05 | U _{I p-p} | Broad Band with jitter free TCLK applied to the input. |
| Output Return Loss | | | | | |
| 51kHz - 102kHz | - | 15 | - | dB | |
| 102kHz - 2048kHz | - | 15 | - | dB | |
| 2048kHz - 3072kHz | - | 15 | - | dB | |

PACKAGE DIMENSIONS

225 BALL PLASTIC BALL GRID ARRAY (BOTTOM VIEW)
(19.0 x 19.0 x 1.0mm)



Note: The control dimension is in millimeter.

| SYMBOL | INCHES | | MILLIMETERS | |
|--------|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.049 | 0.096 | 1.24 | 2.45 |
| A1 | 0.016 | 0.024 | 0.40 | 0.60 |
| A2 | 0.013 | 0.024 | 0.32 | 0.60 |
| A3 | 0.020 | 0.048 | 0.52 | 1.22 |
| D | 0.740 | 0.756 | 18.80 | 19.20 |
| D1 | 0.669 BSC | | 17.00 BSC | |
| D2 | 0.665 | 0.669 | 16.90 | 17.00 |
| b | 0.020 | 0.028 | 0.50 | 0.70 |
| e | 0.039 BSC | | 1.00 BSC | |

8-CHANNEL T1/E1/J1 SHORT-HAUL LINE INTERFACE UNIT

ORDERING INFORMATION

| PART NUMBER | PACKAGE | OPERATING TEMPERATURE RANGE |
|-------------|--------------|-----------------------------|
| XRT83SH38IB | 225 Ball BGA | -40°C to +85°C |

REVISIONS

| REVISION # | DATE | DESCRIPTION |
|------------|----------|---|
| 1.0.0 | 12/15/05 | Release to production |
| 1.0.1 | 01/04/05 | Removed TRATIO, Gain control section, text edits. |
| 1.0.2 | 4/19/06 | Corrected referenced hex bits in register 0x05 bit4, LCV/OF. (0xE5h to 0x81h & 0xE0h to 0x80h.) Changed logo format. |
| 1.0.3 | 5/30/06 | Replaced TBD in power consumption table with typical numbers. |
| 1.0.4 | 7/17/06 | Pin number correction, changed SDO pin number from A6 to R7 |
| 1.0.5 | 08/03/06 | Added note to figure 33, (For applications without a free running SCLK, a minimum of 1 SCLK pulse must be applied when CS is "High", before CS is pulled "Low". |
| 1.0.6 | 08/11/06 | Added timing diagram and specs for the uP serial interface. |
| 1.0.7 | 09/08/06 | Modified table 23, deleted 0x0Eh to 0x13h and 0x1Eh to 0x1Fh values for EQC[4:0]. |

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