MxL86110

Ethernet PHY

Single Port Gigabit Ethernet PHY

MxL86110C
MxL86110I

Data Sheet

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Legal Notice

MaxLinear, Inc.
5966 La Place Court, Suite 100
Carlsbad, CA 92008
Tel.: +1 (760) 692-0711
Fax: +1 (760) 444-8598
www.maxlinear.com

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14	**Chapter 2**, **External Signals**: Updated chapter.
24	**Chapter 3**, **Functional Description**: Updated chapter.
33	**Chapter 4**, **MDIO and MMD Register Interface Description**: Updated chapter.
37	**Chapter 5.1**, **Standard Management Registers**: Updated chapter.
59	**Chapter 5.2**, **PHY-specific Management Registers**: Updated chapter.
72	**Chapter 6.1**, **Standard PCS Registers for MMD=0003$_H$**: Updated chapter.
75	**Chapter 6.2**, **Standard Auto-Negotiation Registers for MMD=0007$_H$**: Updated chapter.
79	**Chapter 7.1**, **Common Extended Register**: Updated chapter.
105	**Chapter 7.2**, **UTP Extended Register**: Updated chapter.
128	**Chapter 8**, **Electrical Characteristics**: Updated chapter.
138	**Chapter 9**, **Package Outline**: Updated chapter.
144	**Terminology**: Updated chapter.

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Preface

This Data Sheet describes the features and system architecture of the single port Gigabit Ethernet PHYs MxL86110C and MxL86110I.

Note: The device address map is considered as a flat address map implementation. No Mailbox functionality behind MDIO IF.

This document uses this synonym to simplify matters:

MxL86110

Synonym used for the Ethernet PHYs MxL86110C and MxL86110I

Organization of this Document

- **Chapter 1**, **Product Overview**
  This chapter provides an overview.
- **Chapter 2**, **External Signals**
  This chapter provides the external signals.
- **Chapter 3**, **Functional Description**
  This chapter provides the function description.
- **Chapter 4**, **MDIO and MMD Register Interface Description**
  This chapter describes the MDIO and MMD register format.
- **Chapter 5**, **MDIO Registers Detailed Description**
  This chapter details the MDIO registers.
- **Chapter 6**, **MMD Registers Detailed Description**
  This chapter details the MDD registers.
- **Chapter 7**, **Extended Register Detailed Description**
  This chapter details the extended register.
- **Chapter 8**, **Electrical Characteristics**
  This chapter provides the electrical specifications.
- **Chapter 9**, **Package Outline**
  This chapter provides information about the package.
- **Standards References**
- **Terminology**

Attention: MaxLinear only guarantees the behavior of the device based on documented registers. The device does not offer any protection against access to other non-documented addresses over the MDIO interface.

1 Product Overview

The MxL86110 is a low power Ethernet PHY transceiver integrated circuit following the IEEE 802.3 [1] standard. It offers a cost-optimized solution that is well-suited for routers, switches, and home gateways. It performs data transmission on an Ethernet twisted pair copper cable of category CAT5e or higher. The MxL86110 supports 1000, 100, and 10 Mbit/s data rates.

On the Ethernet twisted pair interface, the MxL86110 is compliant with the 1000BASE-T (IEEE802.3 Clause 40), 100BASE-TX (IEEE 802.3 Clause 25), and 10BASE-Te (IEEE 802.3 Clause 14) standards defined by the IEEE 802.3 see [1] for more information. This interface supports the Energy-Efficient Ethernet (EEE) feature in accordance with IEEE802.3 [1] to reduce idle mode power consumption. Power saving at the system level is also possible with the Wake-on-LAN feature. A low-EMI line driver with integrated termination facilitates PCB design.

The MxL86110 supports a standard MDIO management interface as defined in IEEE 802.3 Clause 22 and Clause 45 [1]. The MDIO serial interface operates with a clock running up to 12.5 MHz. This allows a management entity (the external chip implementing the MAC) to access standard MDIO / MMD registers to control the MxL86110 behavior, or to read the link status. In addition, vendor specific register banks allow MxL86110-specific configuration of LED, and Wake-on-LAN features. The MDIO and MMD registers are documented in **Chapter 5** and **Chapter 6**, respectively. The MxL86110 is also configurable via pin strapping.

The MxL86110 can drive up to three LEDs. Each LED is independently programmable to indicate the link speed, and traffic activity. Several indication schemes are selectable.

A DC/DC converter is integrated within the MxL86110. A single external power supply of 3.3 V is sufficient to power the chip, with the internal DC/DC converter generating 1.1 V to supply the low voltage domains. External supply of both 3.3 V and 1.1 V is also an option.

The MxL86110 is available in a Quad Flat Non-leaded package (PG-QFN-40). It therefore provides an ideal solution for footprint-sensitive applications such as SFP copper modules or Ethernet Controllers. Furthermore, the MxL86110 design supports a reduced external bill of materials, for example through the integration of termination resistors at both the MDI and MII. The CLKOUT pin can optionally be used to provide a 25 MHz reference clock, allowing for multiple PHY devices to be cascaded while using only one crystal.

The MxL86110 uses a PG-QFN-40 package which is 5 x 5 mm in size.

The MxL86110 has a built-in switching regulator for 1.1 V core power.

The MxL86110 has a built-in LDO providing 2.5/1.8 V power for the RGMII I/O interface.

1.1 Features

This section provides an overview of the features supported by the MxL86110.

Communication Interfaces

- The multiple speed, single-port Ethernet PHY interface to the twisted pair cable supports:
  – Ethernet modes and standards: 1000BASE-T (IEEE 802.3), 100BASE-TX (IEEE 802.3) and 10BASE-Te (IEEE 802.3)
  – Ethernet twisted pair copper cable of category CAT5 or higher
  – Low EMI voltage mode line driver with integrated termination resistors
  – Transformerless Ethernet for backplane applications
  – Auto-Negotiation (ANEG) with extended next page support
  – Auto-MDIX and polarity correction
  – Auto-Downspeed (ADS)
  – Energy-Efficient Ethernet (EEE) and power down mode
  – Wake-on-LAN (WoL)
  – 10k byte jumbo frame support.
- RGMII Interface
- The management interface supports the communication between the Station Management Entity (STA) and the MxL86110 using:
  – An MDIO slave interface that provides access to the standard registers in the MMD as described in IEEE 802.3 Clause 22 and Clause 45 [1] and listed in **Chapter 5** and **Chapter 6**
  – An MDIO interface clock of up to 12.5 MHz
  – Three MDIO message frame types as described in IEEE 802.3: Clause 22, Clause 22 Extended, and Clause 45 [1]

LED Interface, which supports:

- Up to three LEDs
- Single color LEDs
- Connection of LED to ground or 3.3 V
- Several LED indication schemes (link/activity, link speed)
- Configuration of LED indication via Extended Registers

Supports one interrupt output to external controller.

Clocking and Timing Features

- 25 MHz crystal operation

Power Supply

- Single 3.3 V power supply, when using the integrated switching regulator to DC/DC converter to generate the 1.1 V power supply rail
- If the internal integrated DC/DC converter is not used, an additional 1.1 V supply must be provided externally
- Built-in LDO for RGMII IO power 2.5/1.8 V

1.2 Block Diagram

Figure 1 shows the block diagram of the MxL86110. The main interfaces are:

- Data interface to a MAC processor, using RGMII
- Slave control interface driven by a MAC processor, using MDIO slave
- Interrupt signal MDINT allowing the MxL86110 to notify the MAC processor about a change of status
- LED control
- Twisted Pair Interface (TPI)

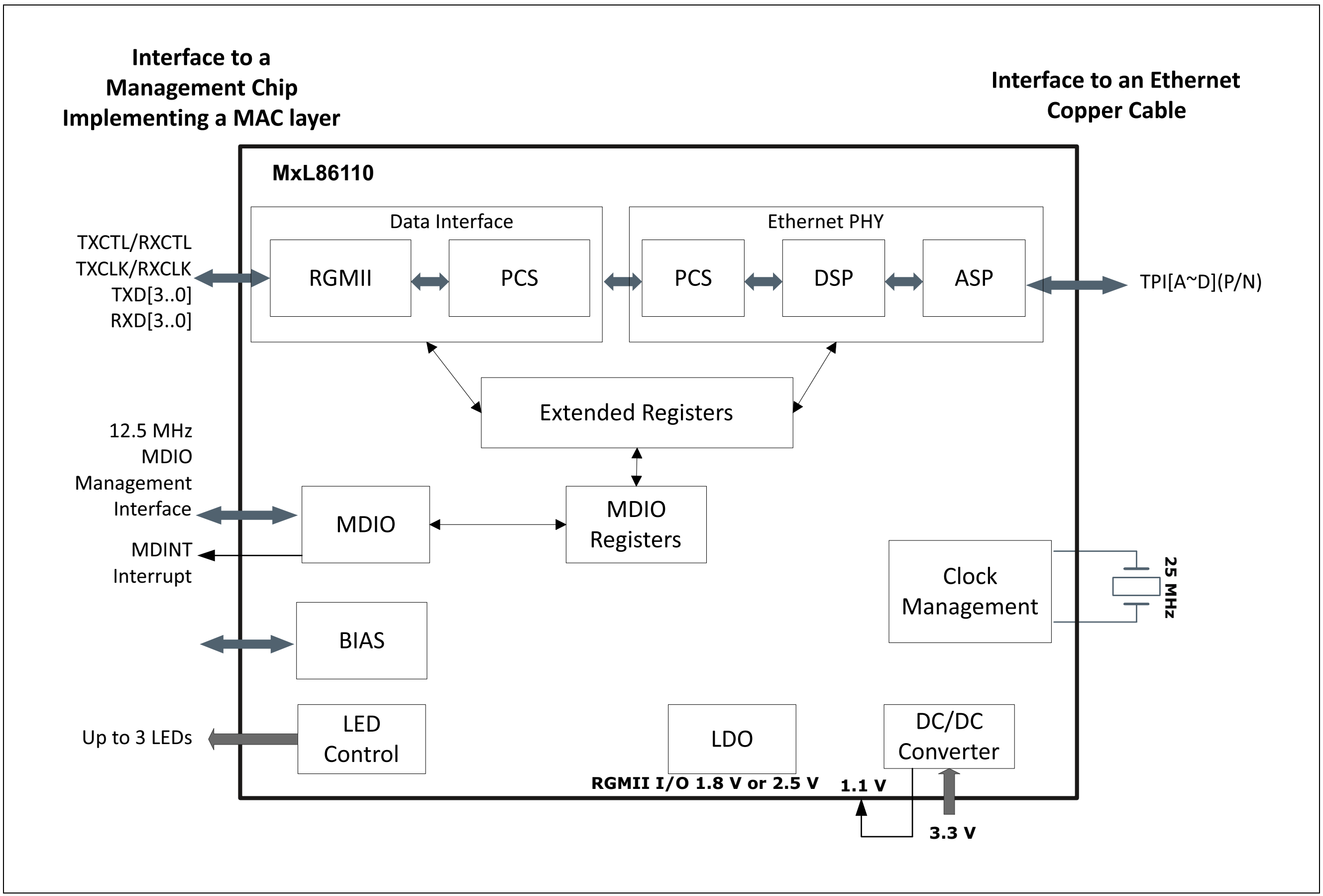

Figure 1 MxL86110 Block Diagram

1.3 Target Applications

- Gateways
- Routers
- Wi-Fi access points
- Set-top-boxes
- IP-phones
- Digital TVs
- Ethernet switches
- NAS
- DVD Players
- Game consoles
- Printers
- Office machines
- Industrial PCs
- IoT devices
- PoE applications

2 External Signals

This chapter describes the signal mapping to the package.

2.1 Overview

Figure 2 provides an overview of the external interfaces of the MxL86110.

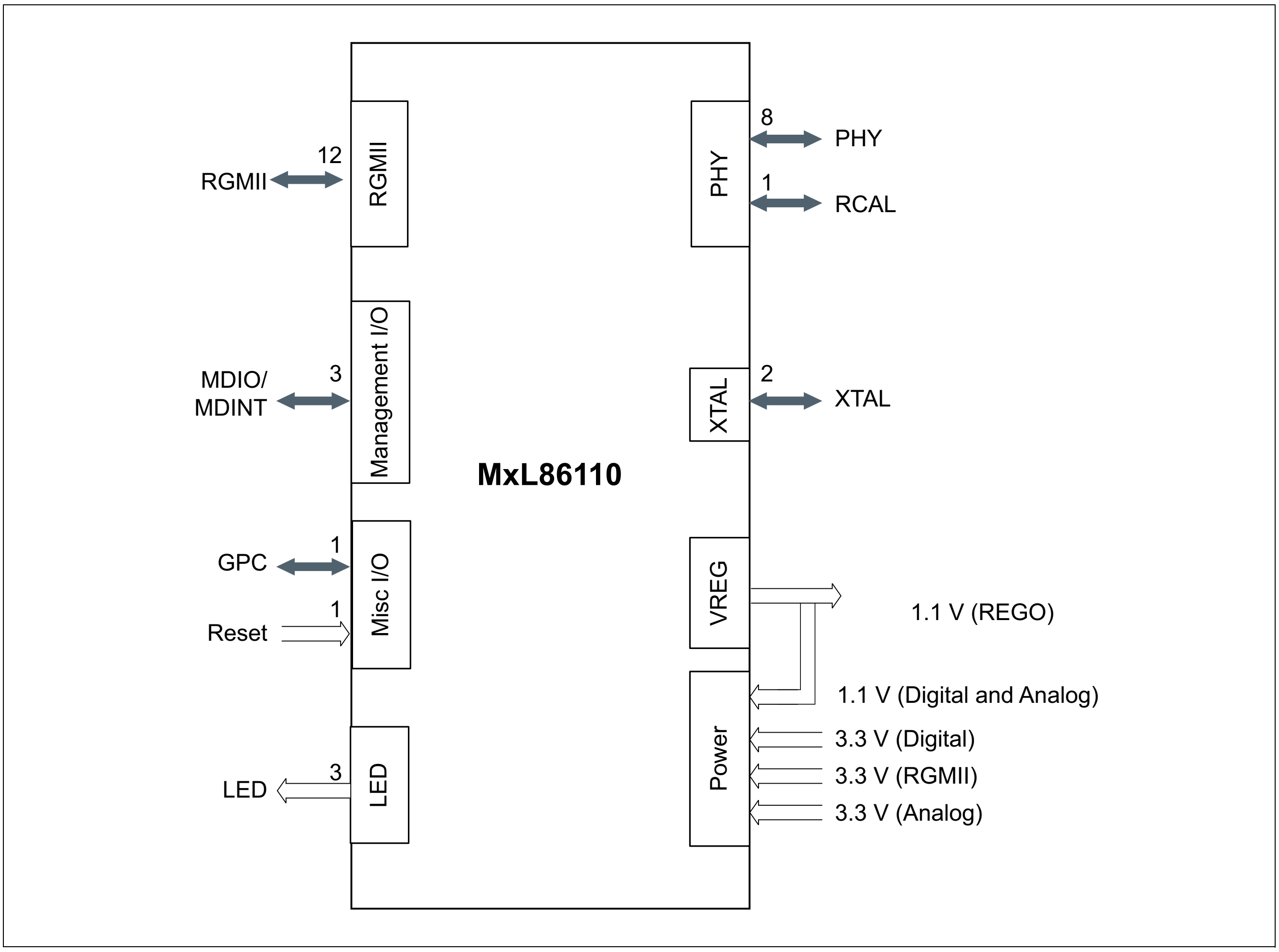

Figure 2 MxL86110 External Signals Overview

2.2 External Signal Description

This section provides the pin diagram, abbreviations for pin types and buffer types, as well as tables describing the input and output signals.

2.2.1 Pin Diagram

Figure 3 shows the pin layout for the MxL86110 package.

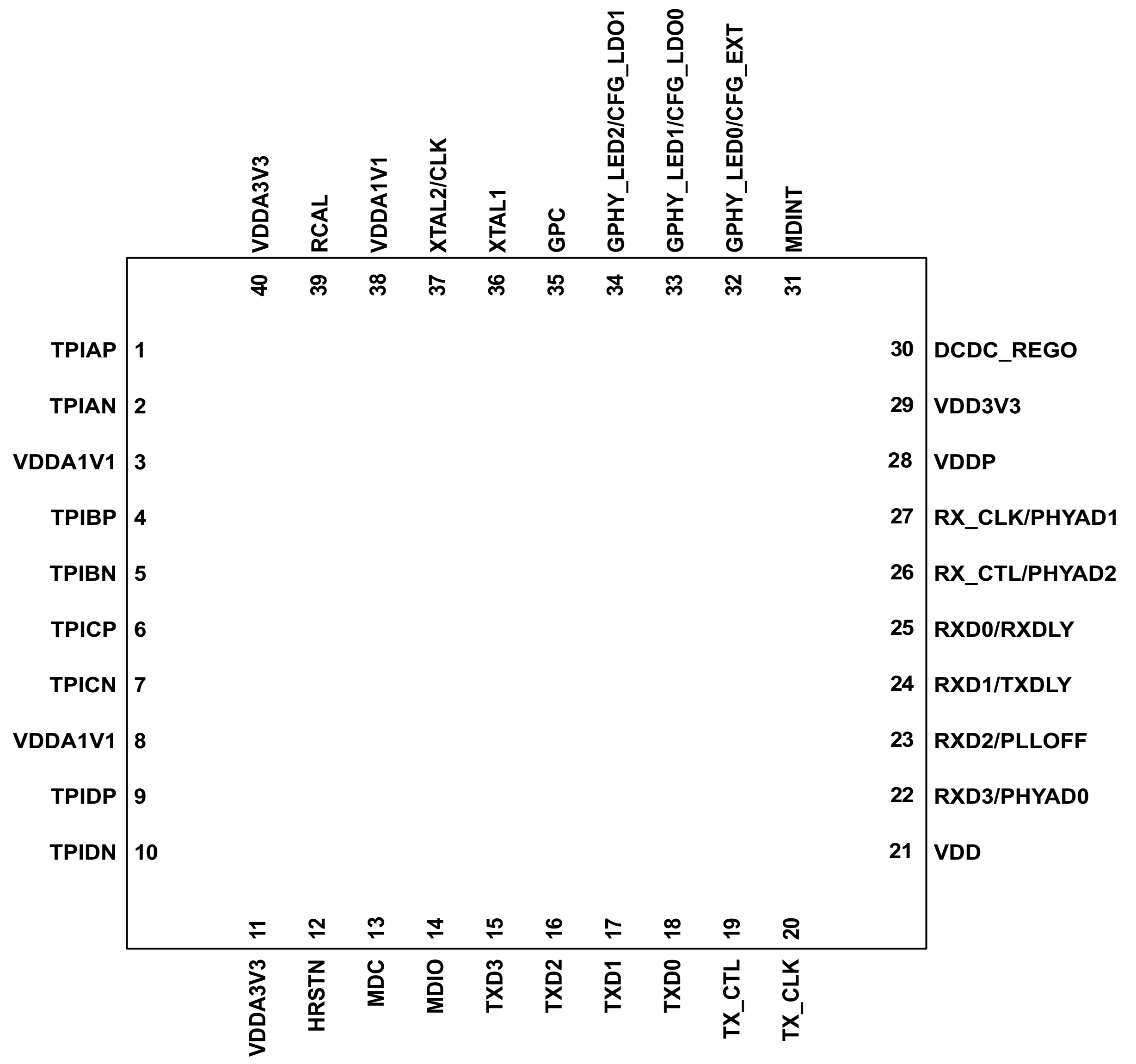

Figure 3 Pin Diagram for MxL86110

2.2.2 Abbreviations

Abbreviations that are used in the signal tables are summarized in **Table 1** and **Table 2**.

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Input only, digital levels
O	Output only, digital levels
I/O	Bidirectional input/output signal, digital levels
AI	Input only, analog levels
AO	Output only, analog levels
AI/O	Bidirectional, analog levels
PWR	Power
GND	Ground

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
A	Analog characteristics, see the AC/DC specification for more detail
GND	Ground
OD	Open Drain
PU	Internal pull-up resistor
PD	Internal pull-down resistor

2.2.3 Input/Output Signals

A detailed description of all the pins is given in **Table 3** to **Table 7**.

In **Table 3** to **Table 7**, the signal names highlighted in bold are the same as the pin name. Signal names are provided in bold. The primary function is listed first and then alternate functions.

2.2.3.1 Ethernet Media Interface

Table 3 describes the Ethernet Media Interface's TPI pins which uses pins 1-10.

Table 3 Ethernet Media Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
Ethernet Port Ethernet Media Interface				
1	**TPIAP**	AI/AO	A	**Twisted Pair Transmit/Receive Positive/Negative**
2	**TPIAN**	AI/AO	A	
4	**TPIBP**	AI/AO	A	
5	**TPIBN**	AI/AO	A	
6	**TPICP**	AI/AO	A	
7	**TPICN**	AI/AO	A	
9	**TPIDP**	AI/AO	A	
10	**TPIDN**	AI/AO	A	

2.2.3.2 RGMII

Table 4 describes the RGMII interface-related pins which uses pins 15-20 and 22-27.

Table 4 RGMII Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
RGMII Interface Signals				
15	**TXD3**	I	PD	**RGMII: Transmit Data Bit 3** This pin carries bit 3 of the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC.
16	**TXD2**	I	PD	**RGMII: Transmit Data Bit 2** This pin carries bit 2 of the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC.
17	**TXD1**	I	PD	**RGMII: Transmit Data Bit 1** This pin carries bit 1 of the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC.
18	**TXD0**	I	PD	**RGMII: Transmit Data Bit 0** This pin carries bit 0 of the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC.
19	**TX_CTL**	I	PD	**RGMII: Transmit Control** This pin is the transmit control signal for the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC.

Table 4 RGMII Interface Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
20	**TX_CLK**	I	PD	**RGMII: Transmit Clock** The TXC signal is a continuous clock signal and provides the timing reference for the transfer of TX_EN_CTL and TXD[3:0]. The nominal frequency of this clock is 125 MHz for 1000 Mbit/s, 25 MHz for 100 Mbit/s, and 2.5 MHz for 10 Mbit/s. Depending on the speed selection, this clock is assumed to be properly adjusted by the MAC. The frequency deviation is assumed to be smaller than +/- 50 ppm.
22	**RXD3 /PHYAD0**	I/O	PD	**RGMII: Receive Data Bit 3** This pin carries bit 3 of the RXD[3:0] RGMII receive data vector. It is synchronous with RXC. **PHYAD0:** This pin reads in soft pin-strapping information during reset.
23	**RXD2 /PLLOFF**	I/O	PD	**RGMII: Receive Data Bit 2** This pin carries bit 2 of the RXD[3:0] RGMII receive data vector. It is synchronous with RXC. **PLLOFF:** This pin reads in soft pin-strapping information during reset.
24	**RXD1 /TXDLY**	I/O	PD	**RGMII: Receive Data Bit 1** This pin carries bit 1 of the RXD[3:0] RGMII receive data vector. It is synchronous with RXC. **TXDLY:** This pin reads in soft pin-strapping information during reset.
25	**RXD0 /RXDLY**	I/O	PD	**RGMII: Receive Data Bit 0** This pin carries bit 0 of the RXD[3:0] RGMII receive data vector. It is synchronous with RXC. **RXDLY:** This pin reads in soft pin-strapping information during reset.
26	**RX_CTL /PHYAD2**	I/O	PD	**RGMII: Receive Control** This is the receive control signal driven by the PHY, and which is synchronous with RXC. The signal encodes the RX_DV and RX_ER signals of the GMII. **PHYAD2:** This pin reads in soft pin-strapping information during reset.
27	**RX_CLK /PHYAD1**	I/O	PD	**RGMII: Receive Clock** The RXC signal is a continuous clock signal and provides the timing reference for the transfer of RX_EN_CTL and RXD[3:0]. The nominal frequency of this clock is 125 MHz for 1000 Mbit/s, 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. The frequency deviation is smaller than +/-50 ppm. **PHYAD1:** This pin reads in soft pin-strapping information during reset.

2.2.3.3 LED Interface

Table 5 describes the LED interface-related pins which allow external LEDs to be connected to the MxL86110C/MxL86110I to indicate the status of the Ethernet PHY interfaces. The LED interface uses pins 32-34.

Table 5 LED Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
LED Signals				
32	**GPHY_LED0 /CFG_EXT**	I/O	PU	**GPHY LED0** The LED control output drives single color LEDs. **CFG_EXT:** This pin reads in soft pin-strapping information during reset.
33	**GPHY_LED1 /CFG_LDO0**	I/O	PU	**GPHY LED1** The LED control output drives single color LEDs. **CFG_LDO0:** This pin reads in soft pin-strapping information during reset.
34	**GPHY_LED2 /CFG_LDO1**	O	PD	**GPHY LED2** The LED control output drives single color LEDs. **CFG_LDO1:** This pin reads in soft pin-strapping information during reset.

2.2.3.4 Management Interfaces

Table 6 describes the MIDO slave interface pins which uses pins 13, 14, and 31

Table 6 Management Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
MDIO Slave Interface				
13	**MDC**	I	PD	**MDIO Slave Clock** The external controller host, also called STA by the IEEE, acts as clock master and provides the serial clock of up to 12.5 MHz on this input.
14	**MDIO**	I/O	PU	**MDIO Slave Data Input/Output** The external controller host uses this signal to address internal registers and to transfer data to and from the internal registers.
31	**MDINT**	O	OD	**MDIO Interrupt** The MDINT signal is used to send an interrupt to an external MAC SoC acting as station manager (STA).

2.2.3.5 Miscellaneous Signals

Table 7 lists miscellaneous signals required by the device.

Table 7 Miscellaneous Signals

Pin No.	Name	Pin Type	Buffer Type	Function
Reset and Clocking				
37	**XTAL2**	AO	A	**Crystal: Oscillator Output** A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must also tie both pins to GND.
	CLK	I		**Clock: Clock Input** The clock must have a frequency accuracy of ±50 ppm. When connecting an external 25 MHz oscillator or clock from another device to XTAL2 pin, XTAL1 must be tied to GND.
36	**XTAL1**	AI	A	**Crystal: Oscillator Input** A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must also tie both pins to GND.
35	**GPC**	O		**General Purpose Clock** 1. This is the reference clock generated from the internal PLL. This pin should be kept floating if the clock is not used by the MAC. 2. UTP recovery receive clock for Sync Ethernet. 3. 25 MHz reference clock.
12	**HRSTN**	I	PU	**Hardware Reset** Asynchronous active low device reset.

2.2.3.6 Power Supply

This section specifies the power supply pins. The device is supplied by to supply rails, V_{HIGH} (3.3 V) and V_{LOW} (1.1 V). The V_{LOW} domain can either be supplied externally, or self-generated by the internal DC/DC Selecting Voltage Regulator (SVR) converter, which converts the VDD3V3 supply into DCDC_REGO output. In the external supply configuration, the DCDC_REGO output pins are not connected (NC). In the internal DC/DC SVR converter configuration, the DCDC_REGO output pins are connected back to the V_{LOW} supply inputs.

Table 8 Power Supply Pins

Pin No.	Name	Pin Type	Buffer Type	Function
Power Supply Pins				
11, 40	**VDDA3V3**	PWR		**High Voltage Domain Supply V_{HIGH}** These are the input power pins for the analog front end in the high voltage domain. They must be supplied with a nominal voltage of V_{DDA3V3} = 3.3 V.
3, 8, 38	**VDDA1V1**	PWR		**Low Voltage Domain Supply V_{LOW}** These are the input power supply pins for the low voltage domain. These pins must be supplied with a nominal voltage of 1.1 V. When the internal DC/DC SVR converter is used, they must be connected to the output of the converter DCDC_REGO.
28	**VDDP**	PWR		**Configurable MDIO Pin Voltage Domain Supply** The voltage domains for the digital RGMII I/O and MDC/MDIO are controlled by the pins CFG_EXT, CFG_LDO0, and CFG_LDO1. Refer to **Section 3.16** for the settings. No matter whether the I/O pin power form external or internal, a bulk capacitor and a decoupling capacitor should be connected to this pin.
21	**VDD**	PWR		**Core Voltage Domain Supply V_{LOW}** This is the group of supply pins for the core digital voltage domain. This pin must be supplied with a nominal voltage of V_{DD} = 1.1 V. When the internal DC/DC SVR converter is used, these pins must be connected to the output of the converter DCDC_REGO.
29	**VDD3V3**	PWR		**Power Supply V_{HIGH}** This pin must be supplied with a nominal voltage of V_{DD3V3} = 3.3 V.
30	**DCDC_REGO**	PWR		**Internal DC/DC SVR Converter Output** The connection circuitry for the internal DCDC SVR V_{LOW} supply option and the external V_{LOW} supply option are described in **Figure 16**.
Ethernet Port Calibration				
39	**RCAL**	AI/AO	A	**Calibration of GPHY Ethernet Port** Connect a high precision resistor of 2.49 kΩ ±1% to GND

Table 9 Device Ground

Pin No.	Name	Pin Type	Buffer Type	Function
EPAD[1)]	VSS	GND		General device ground

1) The EPAD is the exposed pin on the bottom of the package. This pin must be properly connected to the ground plane of the PCB.

3 Functional Description

This chapter describes the functions available to the MxL86110.

3.1 Management Interface

The status and control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 12.5 MHz.

3.2 Auto-Negotiation (ANEG)

The MxL86110 negotiates its operation mode using the ANEG mechanism according to IEEE 802.3 Clause 28 over the copper media. ANEG supports choosing the mode of operation automatically by comparing its own abilities and received abilities from link partner. The advertised abilities include:

- Speed: 10/100/1000Mbps
- Duplex mode: full-duplex and/or half-duplex

ANEG is initialized when these scenarios occur:

- Power-up/Hardware/Software reset
- ANEG restart
- Transition from power down to normal operation of the port
- Link down

ANEG is enabled for MxL86110 by default, and can be disabled by software control.

3.3 Polarity Detection and Auto Correction

The MxL86110 can detect and correct two types of cable errors.

- Swapped pairs within the UTP cable:
  - Pair 0 and 1, and/or pair 2 and 3.
- Swapped wires within a pair.

3.4 Loopback Mode

The MxL86110 supports several test loops to support system integration.

3.4.1 Near-End Test Loops

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the MxL86110.

The near-end test loops are used to verify system integration of an MxL86110 device. They allow for closed loopback of data and signals at different Open Systems Interconnection (OSI) reference layers. **Section 3.4.2** and **Section 3.4.3** describe these loopback functions in descending order of OSI abstraction layer. Digital loopback is set via STD_CTRL.LB = 1_B. See **Section 5.1.1**.

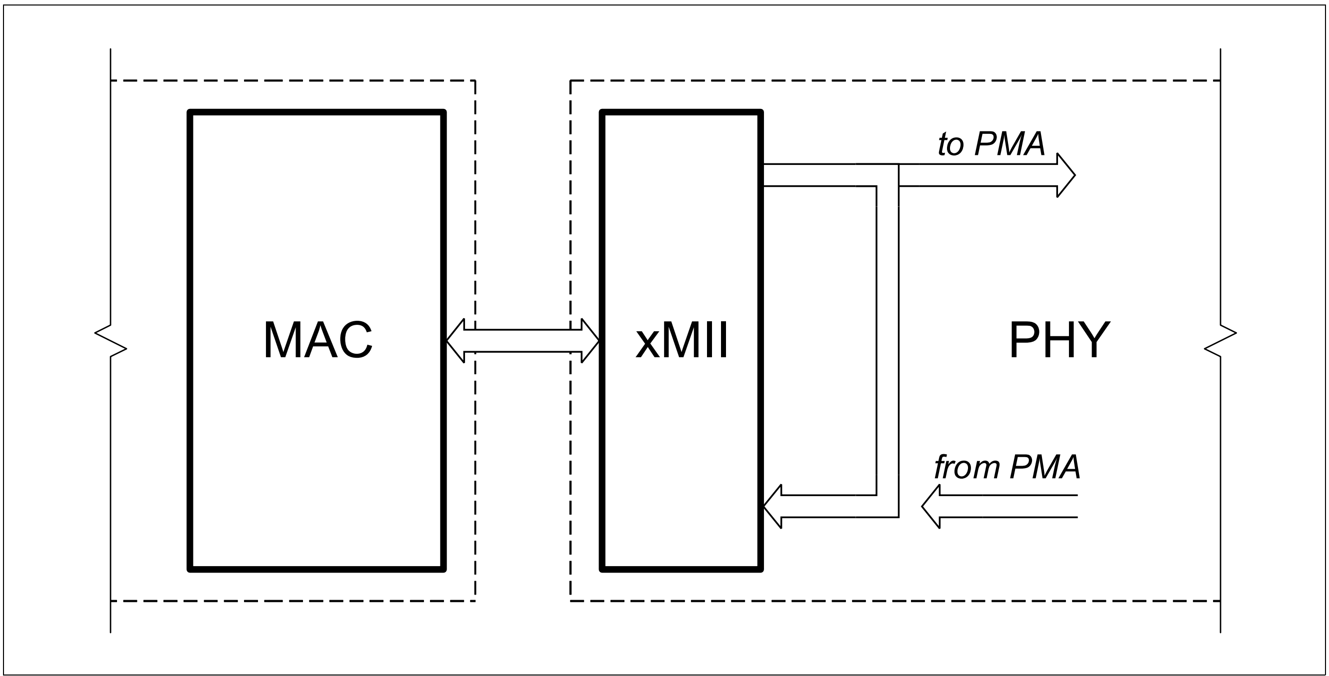

Figure 4 Near-End Loopback

3.4.2 External Loopback

The MxL86110 supports an external loopback with help of a physical connection at the RJ45 connector as shown in **Figure 5**. This allows a complete Tx -> Rx cable loopback.

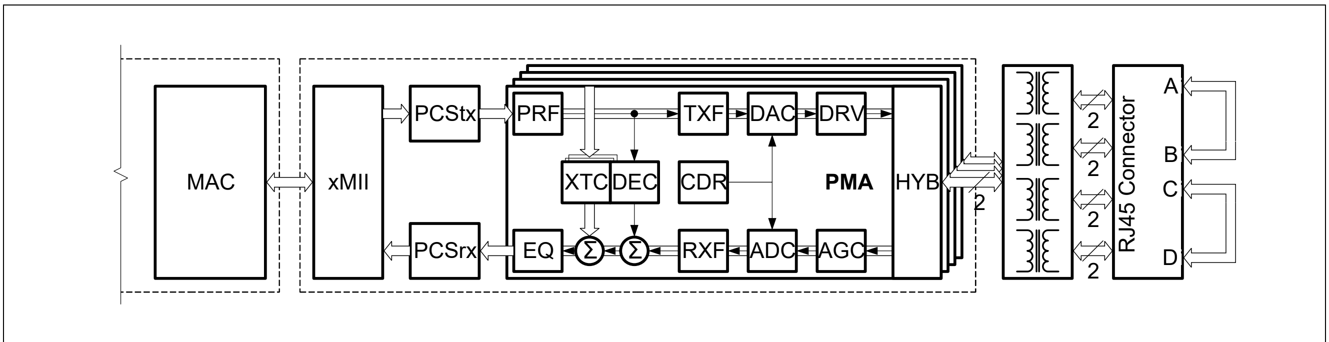

Figure 5 External Loopback

Note: External loopback is set via UTP_EXT_10BT_DBG.ELB. See ***Section 7.2****.*

3.4.3 Far-End PHY Loopback

The Far-End loopback mode connects the MDI Rx path to the MDI Tx path close to RGMII interface as shown in **Figure 6**. With this function the Far-End PHY can detect the proper connectivity.

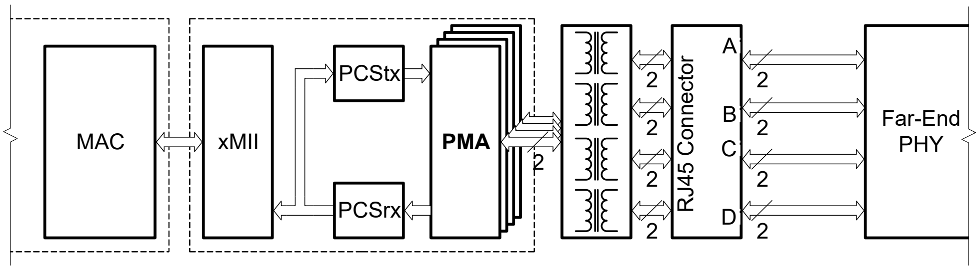

Figure 6 Far-End PHY Loopback

Note: Remote PHY loopback is set via COM_EXT_MISC_CFG.RLBP. See ***Section 7.2****.*

3.5 Energy Efficient Ethernet (EEE)

The IEEE 802.3 standard **[1]** describes the EEE operation that is supported by the MxL86110. EEE is supported in the various speeds of 100BASE-TX and 1000BASE-T. The general idea of EEE is to save power during periods of low link utilization. Instead of sending active idle data, the transmitters are switched off for a short period of time. This is called the quiet period in the standard. The link is kept active by means of a frequent refresh cycle initiated by the PHY itself while in the low power state. This sequence is repeated until a wake request is generated by one of the link partner MACs.

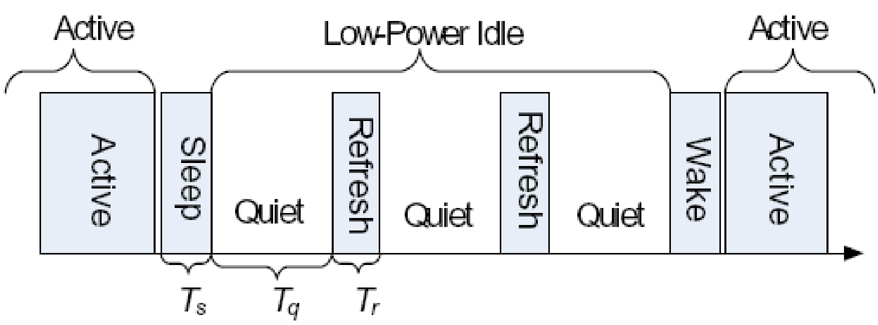

Figure 7 EEE Low Power Idle Sequence

3.6 Synchronous Ethernet (SyncE)

The MxL86110 provides Synchronous Ethernet (SyncE) support when the device is operating in 1000BASE-T and 100BASE-TX on the transmission media. The GPC pin can be assigned to output the recovered clock.

The MxL86110 allows a SyncE interface to support transportation of a source-referable clock from a clock master to clock clients. This is supported in 1000BASE-T and 100BASE-T mode on the TPI.

- In 1000BASE-T, the GPC outputs the recovered clock from PHY<->PHY.
- In slave mode, the GPC outputs the recovered clock from MDI.
- In master mode, the GPC outputs the clock from local free running PLL.

When the GPC pin is assigned to output the recovered clock from the PHY and the PHY is configured for 1000BASE-T mode, the function of the GPC varies depending upon the current PHY mode.

- When the PHY is in slave mode, the GPC outputs the recovered clock from the MDI.
- When the device is in master mode, the GPC outputs the clock based on the local free run PLL.

3.7 Wake-On-LAN (WoL)

The MxL86110 supports WoL. The MxL86110 generates an interrupt to an external controller when it detects special WoL Ethernet packets. This allows the controller to enter into sleep mode when there is no Ethernet traffic to process, and be woken up when traffic starts. WoL packets are detected at all link speeds. **Figure 8** shows this scenario. The specific frame contains a specific data sequence located anywhere inside the packet. The 48-bit address is set using the COM_EXT_MAC_ADDR_CFG1, COM_EXT_MAC_ADDR_CFG2, and COM_EXT_MAC_ADDR_CFG3 registers. See **Section 7.1**.

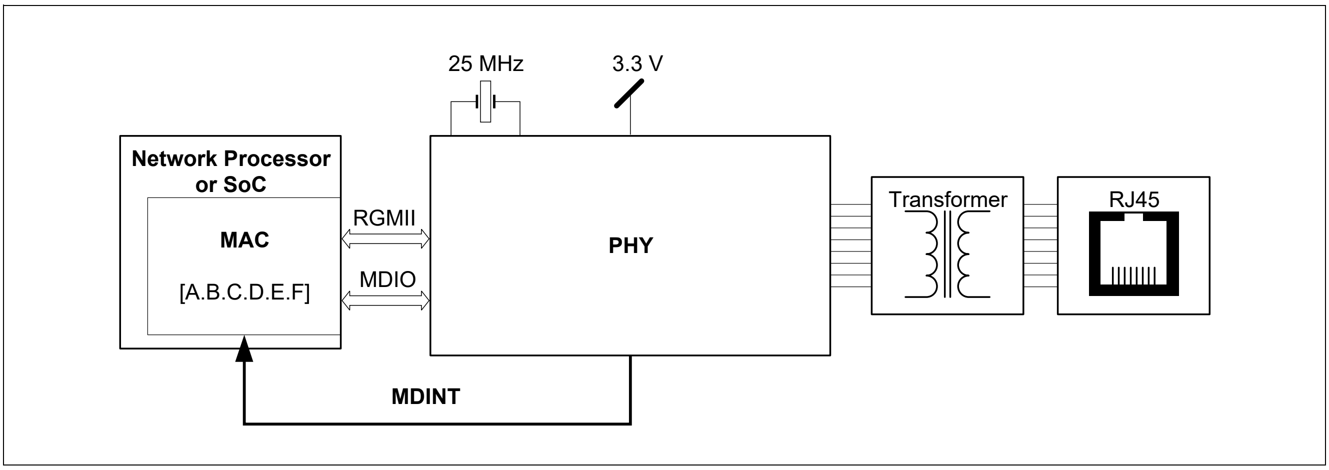

Figure 8 Block Diagram of WoL Application

The most commonly used WoL packet is called a magic packet. A magic packet contains the MAC address of the device to be woken up.

3.8 Link Down Power Saving (Sleep Mode)

The MxL86110 supports link down power saving, also called sleep mode. The MxL86110 enters sleep mode after around 40 seconds if no signals are received over the Ethernet cable.

In sleep mode, the MxL86110 disables almost all circuits, nevertheless access by MDC/MDIO interface remains available.

Once signals are detected on an Ethernet cable, the MxL86110 exits sleep mode automatically.

3.9 Interrupt

The MxL86110 provides an active low interrupt output signal (MDINT) based on change of the PHY status. Every interrupt condition is mapped to the read-only general interrupt status register by the read-only general interrupt status register. See **Section 5.2** for more information.

The interrupts can be individually enabled or disabled by setting or clearing bits in the interrupt enable register **Section 5.2**. See PHY_IMASK **Section 5.2.3**.

The MDINT signal is used to send an interrupt to an external MAC SoC acting as station manager (STA). The STA can program its sensitivity to specific events using the PHY_IMASK register. The MDINT event is then raised when the event occurs. The STA can read which type of event occurred in the PHY_ISTAT register. Upon reading of PHY_ISTAT by the STA, the MDINT is deasserted by the MxL86110.

Note: The interrupt of the MxL86110 is a level-triggered mechanism.

3.10 Reset

The MxL86110 has a hardware reset (HRSTN) pin. The HRSTN signal must be active for at least 10 ms after power-up. After the HRTSN is released, the MxL86110 latches the input values on the strapping pins to configure the device settings. This is useful for configuring the device in applications where MDIO access is unavailable. After a hardware reset, there is a 100 ms MDIO access delay to complete MxL86110 internal initialization.

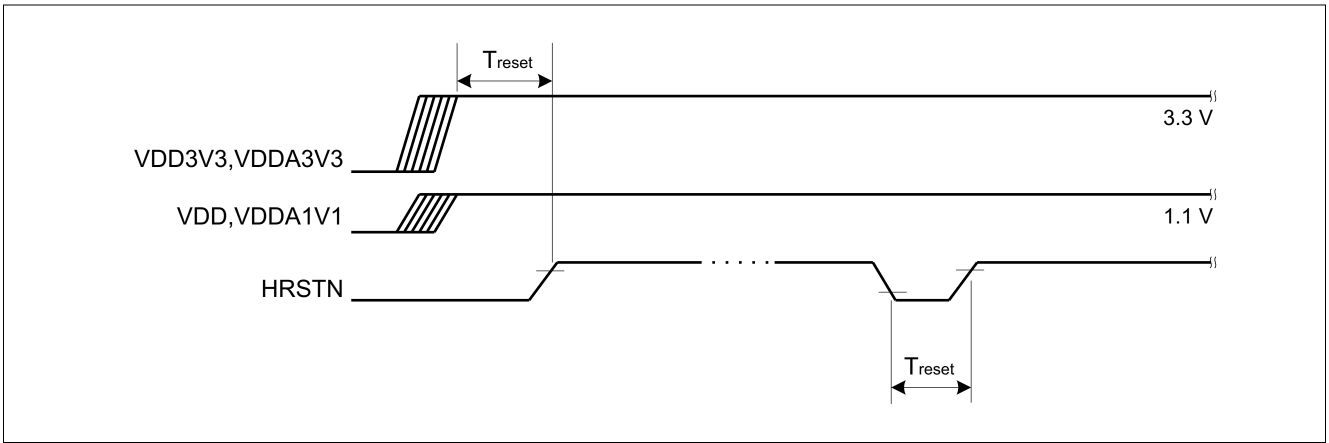

Figure 9 Reset Timing Diagram

Table 10 Reset Timing Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
T_{reset}	The amount of time to allow all power rails to stabilize before releasing HRSTN to high.	10	-	-	ms
T_{reset}	The minimum amount of time for a reset signal to be recognized.	10	-	-	ms

3.11 PHY Address

The MxL86110 offers the ability to configure the PHY address from the pins PHYAD1/PHYAD2. In addition, MxL86110 supports broadcast address 0 on the MDIO bus. This feature enables PHY to always respond to MDIO access. It is controlled via the COM_EXT_RGMII_MDIO_CFG register. See **Section 7.1** for more information.

The MxL86110 supports the option to configure a dedicated broadcast PHY address.

3.12 RGMII Interface

The RGMII interface implements a MAC interface which is usable for all supported speeds (10/100/1000 Mbit/s).

The transfer of data between the MAC and PHY devices is handled via a clock signal, a control signal, and a four bit data vector in both the transmit and receive directions. The clock signal is always driven by the signal source, which is the MAC in the transmit direction and PHY in the receive direction. The control and data signals change with both the rising and falling edges of the driving clock.

The nominal driving clock frequency at 1000 Mbit/s data speeds is 125 MHz. Lower speeds of 100 Mbit/s and 10 Mbit/s use a clock frequency of 25 MHz and 2.5 MHz respectively. At these lower speeds, the higher half of the data octet is empty and the signals on TXD[3:0] and RXD[3:0] are duplicated.

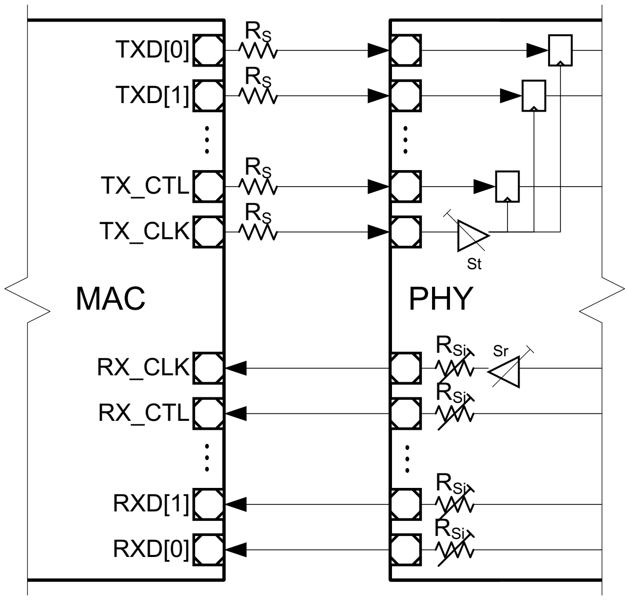

Figure 10 Connection Diagram of RGMII

3.13 LED Interface

The LED interface is controllable by two methods: by the PHY or manually controlled. The LED interface provides up to three LEDs to provide visual indication of the link speed, duplex, and link status. The LEDs are programmable by the MDIO interface via direct register access. Figure 11 shows the LED circuit design.

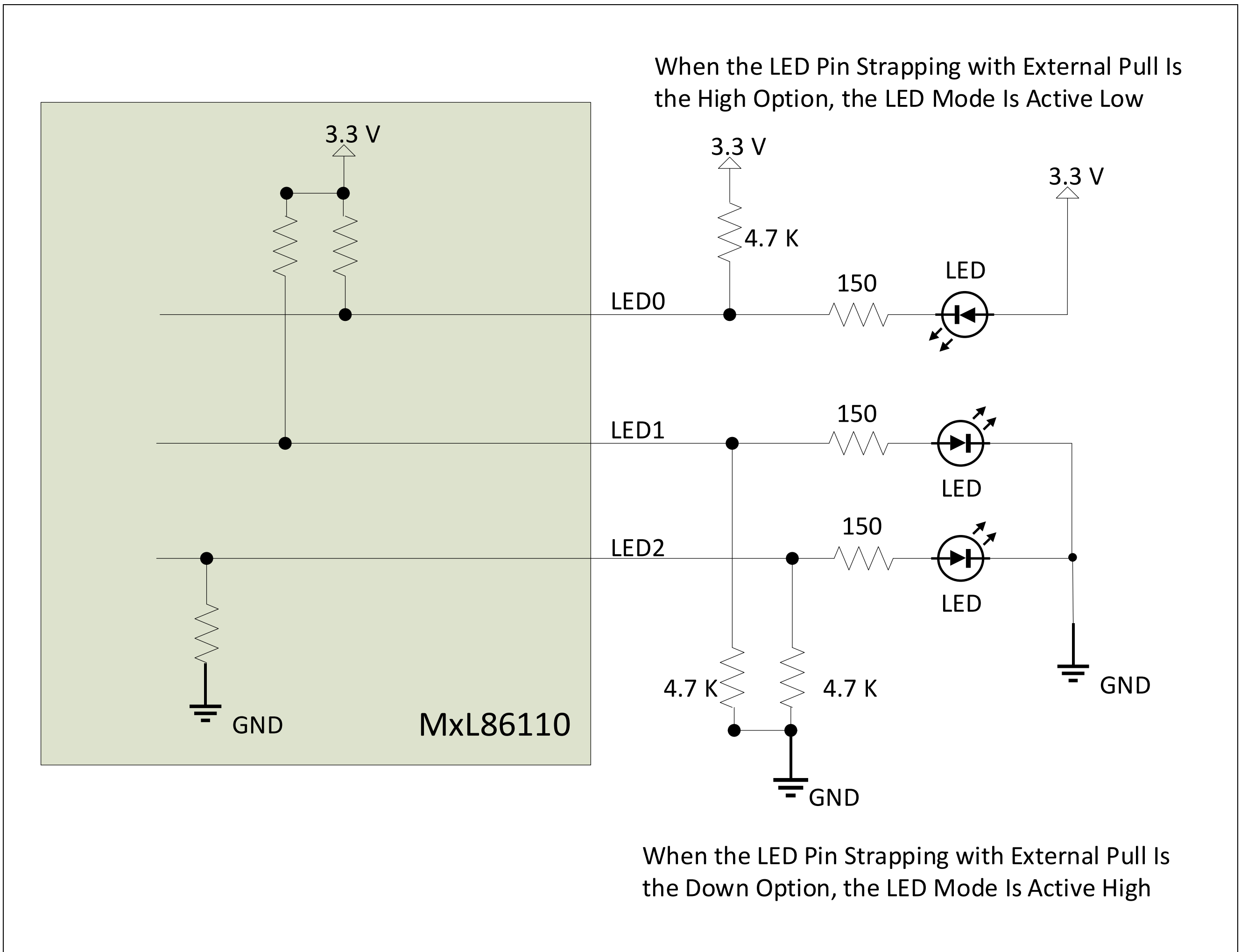

Figure 11 LED Circuit Design

3.14 MDINT Pin Usage

The MDINT pin is used to notify the network processor, or SoC, of both interrupt and WoL events. For general use, indication of a WoL event is also integrated into one of the interrupt events which is triggered when any specified WoL event occurs.

3.15 Power Supply Rails

The MxL86110 requires only one external supply rail of 3.3 V. The device has an integrated SVR which generates the 1.1 V rail, as well as an LDO to adapt to different RGMII levels (either 2.5 / 1.8 V).

The RGMII I/O voltage level is set via external strapping.

When the integrated SVR is not used, the MxL86110 can be powered by a 3.3 V and 1.1 V dual power supply. See **Section 8.2** for more information on the electrical characteristics of the power supply. In external supply mode, the DCDC_REGO output pins are left unconnected. The integrated SVR converter is able to be switched off after power up.

3.16 Configuration by Pin Strapping

The MxL86110 device can be configured by means of pin strapping several pins. The pin strapping configurations are captured during the chip power-on sequence, until the reset initialization is complete. The pin strap values can be set to logical high or low by connecting the corresponding pin via an external 1 kΩ resistor to either ground or the VDD domain supply for the pin strapping pins. For example, GPHY_LED0/1/2 connects to either ground or 3.3 V and RXD3/2/1/0/RX_CLK/RXCTL connects to either ground or the VDDP domain.

The pin strap mapping is described in **Table 11** and **Table 12**.

Table 11 Pin Names Used for Pin Strapping

Pin Name	Pin Number	Configuration Item Description
RXD3	22	PS_PHY_MADDR(0)
RXD2	23	PLLOFF
RXD1	24	TXDLY
RXD0	25	RXDLY
RX_CTL	26	PS_PHY_MADDR(2)
RX_CLK	27	PS_PHY_MADDR(1)
GPHY_LED0	32	CFG_EXT
GPHY_LED1	33	CFG_LDO0
GPHY_LED2	34	CFG_LDO1

Table 12 Pin Strapping Configuration Description

Pin Strapping Signals	Description
PS_PHY_MADDR(2:0)	**MDIO PHY Address** A high level means a logical 1 and low level means a logical 0.
PLLOFF	**PLL off Configuration During Sleep Mode** 0_B PLL is on during sleep mode. 1_B PLL is off during sleep mode.
TXDLY	**RGMII Transmit Clock Timing Control** 0_B No additional delay on TX_CLK. 1_B Enable 2 ns delay on TX_CLK when TX_CLK is 125 MHz or 8 ns delay on TX_CLK when TX_CLK is 25 MHz/2.5 MHz.
RXDLY	**RGMII Receiver Clock Timing Control** 0_B No additional delay on RX_CLK. 1_B Enable 2 ns delay on RX_CLK when RX_CLK is 125 MHz or 8 ns delay on RX_CLK when RX_CLK is 25 MHz/2.5 MHz.

Table 12 Pin Strapping Configuration Description

Pin Strapping Signals	Description
CFG_EXT	**External Power Source Mode Configuration** 0_B Use the integrated LDO to supply the RGMII/MDIO I/O pin. 1_B Use an external power source on VDDP for the RGMII/MDIO I/O pin.
CFG_LDO(1:0)	**Configuration of Integrated LDO voltage** This is the voltage level configuration for supplying the RGMII/MDIO I/O pin. 00_B Reserved 01_B **2.5 V** 10_B **1.8 V** $1x_B$ **1.8 V**

4 MDIO and MMD Register Interface Description

This chapter describes the MDIO and MMD registers, which are standardized by IEEE 802.3 [1], and available to support the MxL86110 feature set. After power-on, the MxL86110 resets the MDIO and MMD registers to default values that are sufficient to operate without specific programing.

All the register definitions, behaviors, and fields are strictly compliant with the IEEE 802.3 [1]. There are PHY specific registers which are not referenced in IEEE 802.3, which can be found in Section 5.2. These allow custom functions related to the MxL86110.

4.1 Definitions

These acronyms are used in the IEEE 802.3 standard and commonly used in the Ethernet technical domain:

- **STA**: Station Management. A host connected to the MDIO interface. STAs are generally Media Access Controllers (MACs). The STA drives the MDIO bus as a clock master and the MxL86110 is MDIO slave.
- **Host**: Used as a synonym of STA in this document.
- **PHY**: Physical Layer. In the MxL86110 this encompasses Analog Signal Processing, Digital Signal Processing, and Physical Coding Sublayer (PCS). The PHY contains several sub-layers that are individually manageable entities known as MDIO manageable devices (MMDs).
- **MMD**: MDIO Manageable Device. The list of MMDs available in the MxL86110 is in Section 4.3.
- **Device**: In the context of MDIO/MMD registers, a device is a register bank grouped by logical sub-layers of the PHY layer.
- **Clause**: Refers to a particular section of the IEEE 802.3 standard [1]. In particular Clause 22 describes MDIO device 0, and Clause 45 describes the other MMDs.
- **MII**: Media Independent Interface. This encompasses the MDIO as well as the (G)MII as described in Clause 22. STD registers in device 0 are also called MII registers.

4.2 Register Naming and Numbering

The register numbering convention in this document is similar to that of IEEE 802.3:

The numbering syntax uses 3 numbers “a.b.c” as specified in IEEE 802.3 paragraph 45.1, and the notation is generalized to Clause 22 registers in device 0 “STD”. The alphanumeric syntax also uses the same structure and uses the names of the MMD devices, registers and register fields separated by underscore and dot as described below.

4.2.1 Register Numbering

The syntax is as follows, with a, b, c written as decimal numbers:

a.b.c = <DEVICE_NUMBER>.<REGISTER_NUMBER>.<FIELD_NUMBER>

When the last indicator (c) is omitted, the register numbering refers to the full register.

When a field is more than a single bit, the bit range is indicated using a semicolon (e.g. 1:3 is the field of bits 1 to 3). In an MDIO register, the least significant bit is bit 0 and most significant bit is bit 15. All MDIO registers are 16 bit wide.

4.2.2 Register Naming

The syntax is as follows, with AA, BB, CC written as alphanumeric strings:

AA.BB.CC = <DEVICE_NAME>_<REGISTER_NAME>.<FIELD_NAME>

When the last indicator (CC) is omitted, the register naming refers to the full register.

The fields named RES, refer to reserved fields as per IEEE 802.3 documents.

4.2.3 Examples

STD_STAT.ANOK is the name of the field 0.1.5, which indicates auto-negotiation complete.

ANEG_CTRL.ANEG_RESTART is the name of the field 7.0.9, which allows the STA to restart the Ethernet ANEG procedure.

ANEG_PHYID1 is the complete 16-bit register number 7.2, for the PHY identifier 1 number.

4.3 MMD Devices Present in MxL86110

Table 13 lists the devices present in the MxL86110.

Table 13 MMD Devices Present in MxL86110

MDIO / MMD Name	Device Number (decimal)	Description
PCS	3	Control and status registers related to PCS encoding/decoding device.
ANEG	7	Control and status registers related to auto-negotiation device.

4.4 Responsibilities of the STA

The MMD devices implement groups of standardized registers under the management of the STA. They are defined in IEEE 802.3.

As per IEEE 802.3 guidelines, it is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs of the MxL86110.

4.5 MDIO Access Protocols to Read / Write Registers

All the MDIO/MMD registers can be accessed from an external chip connected to the MDIO bus on the MDIO and MDC pins. The MxL86110 supports several MDIO frame protocols:

- Clause 22: To access Device 0
- Clause 22 Extended: To access other devices (Dev 3: PCS, Dev 7: ANEG,) using the indirection scheme specified by IEEE 802.3.
- Clause 45: to access device as Table 13.

Both Clause 22 Extended and Clause 45 can be used to access MMD devices. However, the mechanism implemented in the MxL86110 provides faster speeds using Clause 45, so there are some differences in latencies in the MDIO reply:

- Protocol “Clause 22 Extended" involves the MxL86110 an indirection mechanism.
- Protocol “Clause 45" provides faster replies.

The Clause 22 registers can be accessed using the Clause 45 electrical interface and the Clause 22 management frame structure (IEEE 802.3 section 45.2).

5 MDIO Registers Detailed Description

Table 14 MDIO Register Access Type

Mode	Symbol
Status Register (Status, or Ability Register)	RO
Read-Write Register (e.g. MDIO Register)	RW
Read-Write, Self-Clearing Register. The bit is cleared after being read from the MDIO interface.	RWSC

Attention: Since the MxL86110 is a 1000 Mbit/s product, the maximum speed capability availabe in the registers is 1000 Mbit/s. Any speed higher than 1000 Mbit/s, such as 2.5 Gbit/s, 5 Gbit/s, or 10 Gbit/s, defaults to 1000 Mbit/s.

5.1 Standard Management Registers

This section describes the IEEE 802.3 standard management registers corresponding to Clause 22.

Table 15 Registers Overview - Standard Management

Register Short Name	Register Long Name	Reset Value
STD_CTRL	STD Control (Register 0)	1140_H
STD_STAT	Status Register (Register 1)	7949_H
STD_PHYID1	PHY Identifier 1 (Register 2)	$C133_H$
STD_PHYID2	PHY Identifier 2 (Register 3)	5580_H 1)
STD_AN_ADV	Auto-Negotiation Advertisement (Register 4)	$11E1_H$
STD_AN_LPA	Auto-Negotiation Link Partner Ability (Register 5)	0000_H
STD_AN_EXP	Auto-Negotiation Expansion (Register 6)	0004_H
STD_AN_NPTX	Auto-Negotiation Next Page Transmit Register (Register 7)	2001_H
STD_AN_NPRX	Auto-Negotiation Link Partner Received Next Page Register (Register 8)	0000_H
STD_GCTRL	Gigabit Control Register (Register 9)	0200_H
STD_GSTAT	Gigabit Status Register (Register 10)	0000_H
STD_MMDCTRL	MMD Access Control Register (Register 13)	0000_H
STD_MMDDATA	MMD Access Data Register (Register 14)	0000_H
STD_XSTAT	Extended Status Register (Register 15)	2000_H

1) For the device specific reset value, refer to the Product Naming table in the **Package Outline** chapter.

5.1.1 Standard Management Registers

This chapter describes all registers of STD in detail.

STD Control (Register 0)

This register controls the main functions of the PHY.

IEEE Standard Register=0

STD_CTRL **Reset Value**
STD Control (Register 0) **1140_H**

15	14	13	12	11	10	9	8	7	6	5 … 0
RST	LB	SSL	ANEN	PD	ISOL	ANRS	DPLX	COL	SSM	RES
rwsc	rw	rw	rw	rw	rw	rwsc	rw	rw	rw	ro

Field	Bits	Type	Description
RST	15	RWSC	**Reset** Resets the PHY to its default state. Active links are terminated. Note that this is a self-clearing bit which is set to zero by the hardware after reset has been done. 0_B **NORMAL** Normal operational mode 1_B **RESET** Resets the device
LB	14	RW	**Loopback on GMII** This mode enables looping back of MII data from the transmit to the receive direction. No data is transmitted to the Ethernet PHY. The device operates at the selected speed. The collision signal remains de-asserted unless otherwise forced by the collision test. 0_B **NORMAL** Normal operational mode 1_B **ENABLE** Closes the loopback from Tx to Rx at xMII
SSL	13	RW	**Forced Speed Selection LSB** This bit only takes effect with the auto-negotiation process is disabled (STD_CTRL.ANEN bit is set to 0_B). This is the lower bit (LSB) of the forced speed selection. In conjunction with the higher bit (MSB), this encoding is valid: The standard procedure to force 2500 Mbit/s operation (when ANEG is disabled) is to program PMA_CTRL with 1.0.6 = 1.0.13 = 1 and 1.0.5:2 = [0 1 1 0] PHY mirrors 1.0.6, 1.0.13 and 0.0.6, 0.0.13 MSB LSB bit values: 00_B **10 Mbit/s** 01_B **100 Mbit/s** 10_B **1000 Mbit/s** 11_B **Reserved**

Field	Bits	Type	Description (cont'd)
ANEN	12	RW	**Auto-Negotiation Enable** Allows enabling and disabling of the auto-negotiation process capability of the PHY. If enabled, the force bits for duplex mode (STD_CTRL.DPLX) and the speed selection (STD_CTRL.SSM, STD_CTRL.SSL) become inactive. Otherwise, the force bits define the PHY operation. 0_B **DISABLE** Disable the auto-negotiation protocol 1_B **ENABLE** Enable the auto-negotiation protocol
PD	11	RW	**Power Down** Forces the device into a power down state (SLEEP) in which power consumption is the minimum required to still maintain the MII management interface communication. When activating the power down functionality, the PHY terminates active data links. The MII interface is also stopped in power down mode. 0_B **NORMAL** Normal operational mode 1_B **POWERDOWN** Forces the device into power down mode
ISOL	10	RW	**Isolate** The isolation mode isolates the PHY from the MAC. MAC interface inputs are ignored, whereas MAC interface outputs are set to tristate (high-impedance). 0_B **NORMAL** Normal operational mode 1_B **ISOLATE** Isolates the PHY from the MAC
ANRS	9	RWSC	**Restart Auto-Negotiation** Restarts the auto-negotiation process on the MDI. This bit does not take any effect when auto-negotiation is disabled using (STD_CTRL.ANEN). Note that this bit is self-clearing after the auto-negotiation process is initiated. 0_B **NORMAL** Stay in current mode 1_B **RESTART** Restart auto-negotiation
DPLX	8	RW	**Forced Duplex Mode** This bit controls forced duplex mode. It forces the PHY into full or half-duplex mode for 10BASE-T and 100BASE-T modes. This field is ignored for higher speeds. Note(s): - This bit only takes effect when the auto-negotiation process (STD_CTRL.ANEN) is set to 0_B. - This bit does not take effect in loopback mode, when STD_CTRL.LB is set to 1_B. 0_B **HD** Half-duplex 1_B **FD** Full-duplex
COL	7	RW	**Collision Test** Allows testing of the COL signal at the xMII interface. When the collision test is enabled, the state of the TX_EN signal is looped back to the COL signal within a minimum latency. 0_B **DISABLE** Normal operational mode 1_B **ENABLE** Activates the collision test

Field	**Bits**	**Type**	**Description** (cont'd)
SSM	6	RW	**Forced Speed Selection MSB** This bit only takes effect when the auto-negotiation process is disabled, that is, bit ANEN is set to zero. This is the most significant bit (MSB) of the forced speed selection. In conjunction with the lower bit, (LSB), the following encoding is valid: PHY mirrors 1.06, 1.0.13 and 0.0.6, 0.0.13 MSB LSB: 00_B **10 Mbit/s** 01_B **100 Mbit/s** 10_B **1000 Mbit/s** 11_B **Reserved**
RES	5:0	RO	**Reserved** Write as zero, ignore on read.

Status Register (Register 1)

This register contains status and capability information about the device. All bits are read-only. A write access by the MAC does not have any effect.

IEEE Standard Register=1

STD_STAT **Reset Value**

Status Register (Register 1) **7949_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CBT4	**CBTXF**	**CBTXH**	**XBTF**	**XBTH**	**CBT2F**	**CBT2H**	**EXT**	**RES**	**MFPS**	**ANOK**	**RF**	**ANAB**	**LS**	**JD**	**XCAP**
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	rolh	ro	roll	rolh	ro

Field	Bits	Type	Description
CBT4	15	RO	**IEEE 100BASE-T4** Specifies the 100BASE-T4 ability. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBTXF	14	RO	**IEEE 100BASE-TX Full-Duplex** Specifies the 100BASE-TX full-duplex ability. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBTXH	13	RO	**IEEE 100BASE-TX Half-Duplex** Specifies the 100BASE-TX half-duplex ability. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
XBTF	12	RO	**IEEE 10BASE-T Full-Duplex** Specifies the 10BASE-T full-duplex ability. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
XBTH	11	RO	**IEEE 10BASE-T Half-Duplex** Specifies the 10BASE-T half-duplex ability. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBT2F	10	RO	**IEEE 100BASE-T2 Full-Duplex** Specifies the 100BASE-T2 full-duplex ability. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBT2H	9	RO	**IEEE 100BASE-T2 Half-Duplex** Specifies the 100BASE-T2 half-duplex ability. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode

Field	Bits	Type	Description (cont'd)
EXT	8	RO	**Extended Status** The extended status registers are used to specify 1000 Mbit/s speed capabilities in the register STD_XSTAT register. 0_B **DISABLED** No extended status information available in register 15 1_B **ENABLED** Extended status information available in register 15
RES	7	RO	**Reserved** Ignore when read.
MFPS	6	RO	**Management Preamble Suppression** Specifies the MF preamble suppression ability. 0_B **DISABLED** PHY requires management frames with preamble 1_B **ENABLED** PHY accepts management frames without preamble
ANOK	5	RO	**Auto-Negotiation Completed** Indicates whether the auto-negotiation process is completed or in progress. 0_B **RUNNING** Auto-Negotiation process is in progress 1_B **COMPLETED** Auto-Negotiation process is completed
RF	4	ROLH	**Remote Fault** Indicates the detection of a remote fault event. 0_B **INACTIVE** No remote fault condition detected 1_B **ACTIVE** Remote fault condition detected
ANAB	3	RO	**Auto-Negotiation Ability** Specifies the auto-negotiation ability. 0_B **DISABLED** PHY is not able to perform auto-negotiation 1_B **ENABLED** PHY is able to perform auto-negotiation
LS	2	ROLL	**Link Status** Indicates the link status of the PHY to the link partner. 0_B **INACTIVE** The link is down. No communication with link partner possible. 1_B **ACTIVE** The link is up. Data communication with link partner is possible.
JD	1	ROLH	**Jabber Detect** Indicates that a jabber event has been detected. 0_B **NONE** No jabber condition detected 1_B **DETECTED** Jabber condition detected
XCAP	0	RO	**Extended Capability** Indicates the availability and support of extended capability registers. 0_B **DISABLED** Only base registers are supported 1_B **ENABLED** Extended capability registers are supported

PHY Identifier 1 (Register 2)

This code specifies the Organizationally Unique Identifier (OUI), the vendor's model number, and the model's revision number.

IEEE Standard Register=2

STD_PHYID1	**Reset Value**
PHY Identifier 1 (Register 2)	**$C133_H$**

15 … 0
OUI
ro

Field	Bits	Type	Description
OUI	15:0	RO	**Organizationally Unique Identifier Bits 3:18**

PHY Identifier 2 (Register 3)

IEEE Standard Register=3

STD_PHYID2 **Reset Value**

PHY Identifier 2 (Register 3) **5580_H**

15 ... 10	9 ... 4	3 ... 0
OUI	**LDN**	**LDRN**
ro	ro	ro

Field	Bits	Type	Description
OUI	15:10	RO	**Organizationally Unique Identifier Bits 19:24**
LDN	9:4	RO	**Device Number** Specifies the device number[1)] to distinguish between several products.
LDRN	3:0	RO	**Device Number** Specifies the device revision number[1)] to distinguish between several versions of this device.

1) For the device specific reset value, refer to Product Naming table in the **Package Outline** chapter.

Auto-Negotiation Advertisement (Register 4)

This register contains the advertised abilities of the PHY during auto-negotiation.

IEEE Standard Register=4

STD_AN_ADV **Reset Value**
Auto-Negotiation Advertisement (Register 4) **$11E1_H$**

15	14	13	12	11 … 5	4 … 0
NP	**RES**	**RF**	**XNP**	**TAF**	**SF**
rw	ro	rw	rw	rw	rw

Field	Bits	Type	Description
NP	15	RW	**Next Page** Next page indication is encoded in bit NP regardless of the selector field value or link code word encoding. The PHY always advertises NP if a 1000BASE-T mode is advertised during auto-negotiation. 0_B **INACTIVE** No next page(s) will follow 1_B **ACTIVE** Additional next page(s) will follow
RES	14	RO	**Reserved** Write as zero, ignore on read.
RF	13	RW	**Remote Fault** The remote fault bit allows indication of a fault to the link partner. 0_B **NONE** No remote fault is indicated 1_B **FAULT** A remote fault is indicated
XNP	12	RW	**Extended Next Page** Indicates that the PHY supports transmission of extended next pages (XNP). 0_B **UNABLE** PHY is XNP unable 1_B **ABLE** PHY is XNP able
TAF	11:5	RW	**Technology Ability Field** The technology ability field is an 8-bit wide field containing information indicating supported technologies. This field indicates PHY support for 10BASE-T (half- and full-duplex), 100BASE-T (half- and full-duplex), and PAUSE (asymmetric and symmetric). 40_H **PS_ASYM** Advertise asymmetric pause 20_H **PS_SYM** Advertise symmetric pause 10_H **DBT4** Advertise 100BASE-T4 08_H **DBT_FDX** Advertise 100BASE-TX full-duplex 04_H **DBT_HDX** Advertise 100BASE-TX half-duplex 02_H **XBT_FDX** Advertise 10BASE-T full-duplex 01_H **XBT_HDX** Advertise 10BASE-T half-duplex
SF	4:0	RW	**Selector Field** The selector field is a 5-bit wide field for encoding 32 possible messages. Combinations not specified are reserved for future use. Reserved combinations of the selector field are not to be transmitted. 00001_B**IEEE802DOT3** Select the IEEE 802.3 technology

Auto-Negotiation Link Partner Ability (Register 5)

IEEE Standard Register=5

When the auto-negotiation is complete, this register contains the advertised ability of the link partner. The bit definitions are a direct representation of the received link code word.

STD_AN_LPA — **Reset Value**
Auto-Negotiation Link Partner Ability (Register 5) — **0000_H**

15	14	13	12	11:5	4:0
NP	ACK	RF	XNP	TAF	SF
ro	ro	ro	rw	rw	ro

Field	Bits	Type	Description
NP	15	RO	**Next Page** Next page request indication from the link partner. 0_B **INACTIVE** No next page(s) will follow 1_B **ACTIVE** Additional next pages will follow
ACK	14	RO	**Acknowledge** Acknowledgment indication from the link partner's link code word. 0_B **INACTIVE** The device did not successfully receive its link partner's link code word 1_B **ACTIVE** The device has successfully received its link partner's link code word
RF	13	RO	**Remote Fault** Remote fault indication from the link partner. 0_B **NONE** Remote fault is not indicated by the link partner 1_B **FAULT** Remote fault is indicated by the link partner
XNP	12	RW	**Extended Next Page** Indicates that PHY supports transmission of extended next pages (XNP). 0_B **UNABLE** Link partner is XNP unable 1_B **ABLE** Link partner is XNP able
TAF	11:5	RW	**Technology Ability Field** 40_H **PS_ASYM** Advertise asymmetric pause 20_H **PS_SYM** Advertise symmetric pause 10_H **DBT4** Advertise 100BASE-T4 08_H **DBT_FDX** Advertise 100BASE-TX full-duplex 04_H **DBT_HDX** Advertise 100BASE-TX half-duplex 02_H **XBT_FDX** Advertise 10BASE-T full-duplex 01_H **XBT_HDX** Advertise 10BASE-T half-duplex
SF	4:0	RO	**Selector Field** 00001_B**IEEE802DOT3** Select the IEEE 802.3 technology

Auto-Negotiation Expansion (Register 6)

This is the auto-negotiation expansion register indicating the status of the link partner's auto-negotiation. This register is valid only after the auto-negotiation is completed.

IEEE Standard Register=6

STD_AN_EXP **Reset Value**
Auto-Negotiation Expansion (Register 6) **0004_H**

15–5	4	3	2	1	0
RES	PDF	LPNPC	NPC	PR	LPANC
ro	rolh	ro	ro	rolh	ro

Field	Bits	Type	Description
RES	15:5	RO	**Reserved** Write as zero, ignore on read.
PDF	4	ROLH	**Parallel Detection Fault** 0_B **NONE** A fault has not been detected via the parallel detection function 1_B **FAULT** A fault has been detected via the parallel detection function
LPNPC	3	RO	**Link Partner Next Page Capable** 0_B **UNABLE** Link partner is unable to exchange next pages 1_B **CAPABLE** Link partner is capable of exchanging next pages
NPC	2	RO	**Next Page Capable** 0_B **UNABLE** PHY is unable to exchange next pages 1_B **CAPABLE** PHY is capable of exchanging next pages
PR	1	ROLH	**Page Received** 0_B **NONE** A new page has not been received 1_B **RECEIVED** A new page has been received
LPANC	0	RO	**Link Partner Auto-Negotiation Capable** 0_B **UNABLE** Link partner is unable to auto-negotiate 1_B **CAPABLE** Link partner is auto-negotiation capable

Auto-Negotiation Next Page Transmit Register (Register 7)

The auto-negotiation next page transmit register contains the next page link code word to be transmitted when next page ability is supported.

IEEE Standard Register=7

STD_AN_NPTX **Reset Value**
Auto-Negotiation Next Page Transmit Register (Register 7) **2001_H**

15	14	13	12	11	10 … 0
NP	RES	MP	ACK2	TOGG	MCF
rw	ro	rw	rw	ro	rw

Field	Bits	Type	Description
NP	15	RW	**Next Page** 0_B **INACTIVE** Last page 1_B **ACTIVE** Additional next page(s) will follow
RES	14	RO	**Reserved** Write as zeros, ignore on read.
MP	13	RW	**Message Page** Indicates that the content of **STD_AN_NPTX.MCF** is either an unformatted page or a formatted message. 0_B **UNFOR** Unformatted page 1_B **MESSG** Message page
ACK2	12	RW	**Acknowledge 2** 0_B **INACTIVE** Device cannot comply with message 1_B **ACTIVE** Device will comply with message
TOGG	11	RO	**Toggle** This bit always takes the opposite value of the **STD_AN_NPTX.TOGG** bit in the previously exchanged link code word. 0_B **ZERO** Previous value of the transmitted link code word was 1_B 1_B **ONE** Previous value of the transmitted link code word was 0_B

Field	Bits	Type	**Description** (cont'd)
MCF	10:0	RW	**Message or Unformatted Code Field** When Message Page **STD_AN_NPTX.MP** bit is set to 1_B (0.7.13), this field is the Message Code Field of a message page used in next page exchange. The message codes are described in IEEE802.3 Appendix 28C. It is used to indicate the type of message in UCF1 and UCF2. 00_H Reserved 01_H Null message 02_H One Unformatted Page (UP) with TAF follows 03_H Two UPs with TAF follows 04_H Remote fault details message 05_H OUI message 06_H PHY ID message 07_H 100BASE-T2 message 08_H 1000BASE-T message 09_H MULTIGBASE-T message $0A_H$ EEE technology capability follows in next UP $0B_H$ OUI XNP

Auto-Negotiation Link Partner Received Next Page Register (Register 8)

The auto-negotiation link partner received next page register contains the next page link code word received from the link partner.

IEEE Standard Register=8

STD_AN_NPRX **Reset Value**
Auto-Negotiation Link Partner Received Next Page Register (Register 8) **0000_H**

15	14	13	12	11	10 ... 0
NP	ACK	MP	ACK2	TOGG	MCF
ro	ro	ro	ro	ro	rw

Field	Bits	Type	Description
NP	15	RO	**Next Page** 0_B **INACTIVE** No next pages to follow 1_B **ACTIVE** Additional next page(s) will follow
ACK	14	RO	**Acknowledge** 0_B **INACTIVE** The device did not successfully receive its link partner's link code word 1_B **ACTIVE** The device has successfully received its link partner's link code word
MP	13	RO	**Message Page** Indicates that the content of **STD_AN_NPTX.MCF** is either an unformatted page or a formatted message. 0_B **UNFOR** Unformatted page 1_B **MESSG** Message page
ACK2	12	RO	**Acknowledge 2** 0_B **INACTIVE** Device cannot comply with message 1_B **ACTIVE** Device will comply with message
TOGG	11	RO	**Toggle** This bit always takes the opposite value of the **TOGG** bit in the previously exchanged link code word. 0_B **ZERO** Previous value of the transmitted link code word was equal to ONE 1_B **ONE** Previous value of the transmitted link code word was equal to ZERO

Field	Bits	Type	Description (cont'd)
MCF	10:0	RW	**Message or Unformatted Code Field** This field is the Message Code Field of a message page used in next page exchange. The message codes are described in IEEE802.3 Appendix 28C. It is used to indicate the type of message in UCF1 and UCF2. 00_H Reserved 01_H Null message 02_H One Unformatted Page (UP) with TAF follows 03_H Two UPs with TAF follows 04_H Remote fault details message 05_H OUI message 06_H PHY ID message 07_H 100BASE-T2 message 08_H 1000BASE-T message 09_H MULTIGBASE-T message $0A_H$ EEE technology capability follows in next UP $0B_H$ OUI XNP

Gigabit Control Register (Register 9)

This is the control register used to configure the Gigabit Ethernet behavior of the PHY.

IEEE Standard Register=9

STD_GCTRL **Reset Value**
Gigabit Control Register (Register 9) **0200_H**

15–13	12	11	10	9	8	7–0
TM	**MSEN**	**MS**	**MSPT**	**MBTFD**	**MBTHD**	**RES**
rw	rw	rw	rw	rw	rw	ro

Field	Bits	Type	Description
TM	15:13	RW	**Transmitter Test Mode** This register field allows enabling of the standard transmitter test modes. 000_B **NOP** Normal operation 001_B **WAV** Test mode 1 transmit waveform test 010_B **JITM** Test mode 2 transmit jitter test in master mode 011_B **JITS** Test mode 3 transmit jitter test in slave mode 100_B **DIST** Test mode 4 transmitter distortion test
MSEN	12	RW	**Master/Slave Manual Configuration Enable** 0_B **DISABLED** Disable master/slave manual configuration value 1_B **ENABLED** Enable master/slave manual configuration value
MS	11	RW	**Master/Slave Config Value** Allows forcing of master or slave mode manually when **STD_GCTRL.MSEN** is set to logical one. 0_B **SLAVE** Configure PHY as slave during master/slave negotiation 1_B **MASTER** Configure PHY as master during master/slave negotiation
MSPT	10	RW	**Master/Slave Port Type** Defines whether the PHY advertises itself as a multi- or single-port device, which in turn impacts the master/slave resolution function. 0_B **SPD** Single-port device 1_B **MPD** Multi-port device
MBTFD	9	RW	**1000BASE-T Full-Duplex** Advertises the 1000BASE-T full-duplex capability; always forced to 1_B in converter mode. 0_B **DISABLED** Advertise PHY as not 1000BASE-T full-duplex capable 1_B **ENABLED** Advertise PHY as 1000BASE-T full-duplex capable
MBTHD	8	RW	**1000BASE-T Half-Duplex** Always advertises the 1000BASE-T half-duplex capability as disabled; PHY does not support 1000BASE-T Half-Duplex capability 0_B **DISABLED** Advertise PHY as not 1000BASE-T half-duplex capable 1_B **ENABLED** Advertise PHY as 1000BASE-T half-duplex capable

Field	Bits	Type	Description (cont'd)
RES	7:0	RO	**Reserved** Write as zero, ignore on read.

Gigabit Status Register (Register 10)

This is the status register used to reflect the Gigabit Ethernet status of the PHY.

IEEE Standard Register=10

STD_GSTAT — **Reset Value**

Gigabit Status Register (Register 10) — **0000_H**

15	14	13	12	11	10	9–8	7–0
MSFAULT	**MSRES**	**LRXSTAT**	**RRXSTAT**	**MBTFD**	**MBTHD**	**RES**	**IEC**
rwsc	ro	ro	ro	ro	ro	ro	rwsc

Field	Bits	Type	Description
MSFAULT	15	RWSC	**Master/Slave Manual Configuration Fault** This bit is set if the number of attempts to set the master/slave configuration reaches 7. It is cleared upon each read of the **STD_GSTAT** register. This bit self clears on auto-negotiation enable or auto-negotiation complete. 0_B **OK** Master/slave manual configuration resolved successfully 1_B **NOK** Master/slave manual configuration resolved with a fault
MSRES	14	RO	**Master/Slave Configuration Resolution** 0_B **SLAVE** Local PHY configuration resolved to slave 1_B **MASTER** Local PHY configuration resolved to master
LRXSTAT	13	RO	**Local Receiver Status** Indicates the status of the local receiver. 0_B **NOK** Local receiver not OK 1_B **OK** Local receiver OK
RRXSTAT	12	RO	**Remote Receiver Status** Indicates the status of the remote receiver. 0_B **NOK** Remote receiver not OK 1_B **OK** Remote receiver OK
MBTFD	11	RO	**Link Partner Capable of Operating 1000BASE-T Full-Duplex** 0_B **DISABLED** Link partner is not capable of operating 1000BASE-T full-duplex 1_B **ENABLED** Link partner is capable of operating 1000BASE-T full-duplex
MBTHD	10	RO	**Link Partner Capable of Operating 1000BASE-T Half-Duplex** 0_B **DISABLED** Link partner is not capable of operating 1000BASE-T half-duplex 1_B **ENABLED** Link partner is capable of operating 1000BASE-T half-duplex
RES	9:8	RO	**Reserved** Write as zero, ignore on read.

Field	Bits	Type	Description (cont'd)
IEC	7:0	RWSC	**Idle Error Count** Indicates the idle error count. This field contains a cumulative count of the errors detected when the receiver is receiving idles.

MMD Access Control Register (Register 13)

The MMD access control register is used in conjunction with the MMDDATA register to access the MMD register space. This uses address directing as specified in IEEE802.3 Clause 22 Extended.

IEEE Standard Register=13

STD_MMDCTRL — **Reset Value**

MMD Access Control Register (Register 13) — **0000_H**

15–14	13–8	7–5	4–0
ACTYPE	RES	RES	DEVAD
rw	ro	ro	rw

Field	Bits	Type	Description
ACTYPE	15:14	RW	**Access Type Function** If the access of the **MMDDATA** register is an address access (**ACTYPE** = 00_B) then it is directed to the address register within the MMD associated with the value in the DEVAD field. Otherwise, both the DEVAD field and the MMD's address register direct the register MMDDATA data accesses to the appropriate registers within that MMD. 00_B **ADDRESS** Accesses to register MMDDATA access the MMD individual address register 01_B **DATA** Accesses to register MMDDATA access the register within the MMD selected 10_B **DATA_PI** Accesses to register MMDDATA access the register within the MMD selected 11_B **DATA_PIWR** Accesses to register MMDDATA access the register within the MMD selected
RES	13:8	RO	**Reserved** Write as zero, ignored on read.
RES	7:5	RO	**Reserved** Write as zero, ignored on read.
DEVAD	4:0	RW	**Device Address** The field directs any accesses of register MMDDATA to the appropriate MMD.

MMD Access Data Register (Register 14)

The MMD access data register is used in conjunction with the MMD access control (MMDCTRL) register to access the MMD register space.

IEEE Standard Register=14

STD_MMDDATA	Reset Value
MMD Access Data Register (Register 14)	0000_H

15 … 0
ADDR_DATA
rw

Field	Bits	Type	Description
ADDR_DATA	15:0	RW	**Address or Data Register** This register accesses either a specific MMD address register or the data content of the MMD register to which this address register points. Which of the functions is currently valid is defined by the MMDCTRL register.

Extended Status Register (Register 15)

This register contains extended status and capability information about the PHY. All bits are read-only. A write access does not have any effect.

IEEE Standard Register=15

STD_XSTAT **Reset Value**

Extended Status Register (Register 15) **2000_H**

15	14	13	12	11–8	7–0
MBXF	MBXH	MBTF	MBTH	RES	RES
ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
MBXF	15	RO	**1000BASE-X Full-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-X full-duplex. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
MBXH	14	RO	**1000BASE-X Half-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-X half-duplex. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
MBTF	13	RO	**1000BASE-T Full-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-T full-duplex. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
MBTH	12	RO	**1000BASE-T Half-Duplex Capability** PHY does not support 1000BASE-T Half-Duplex capability. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
RES	11:8	RO	**Reserved** Ignore when read.
RES	7:0	RO	**Reserved** Ignore when read.

5.2 PHY-specific Management Registers

This section describes the PHY specific management registers.

Table 16 Registers Overview - PHY-specific Management Registers

Register Short Name	Register Long Name	Reset Value
PHY_CTL	PHY Specific Function Control Register (Register 16)	0062_H
PHY_STAT	PHY Specific Status (Register 17)	0000_H
PHY_IMASK	Interrupt Mask Register (Register 18)	0000_H
PHY_ISTAT	Interrupt Status Register (Register 19)	0000_H
PHY_ADS_CTL	Speed Auto Downgrade Control Register (Register 20)	$0082c_H$
PHY_EXT_ADR	Extended Register's Address Offset Register (Register 30)	0000_H
PHY_EXT_DATA	Extended Register's Data Register (Register 31)	$1C8D_H$

5.2.1 PHY Specific Function Control Register (Register 16)

This section describes the PHY Specific Function Control Register in detail.

PHY Specific Function Control Register (Register 16)

The register controls PHY specific functions.

PHY_CTL	**Offset**	**Reset Value**
PHY Specific Function Control Register (Register 16)	**0010_H**	**0062_H**

15 ... 7	6 ... 5	4	3	2	1	0
RES	**MDIX**	**RES**	**CRS**	**SQE**	**POL**	**JAB**
ro	rw	rw	rw	rw	rw	rw

Field	**Bits**	**Type**	**Description**
RES	15:7	RO	**Reserved**
MDIX	6:5	RW	**MDI Crossover** Changes made to these bits disrupt normal operation, thus a software reset is mandatory after the change. The configuration does not take effect until software reset. 00_B Manual MDI configuration 01_B Manual MDIX configuration 10_B Reserved 11_B Enable automatic crossover for all modes
RES	4	RW	**Reserved**
CRS	3	RW	**Carrier Sense on Transmitting** This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode: 0_B Never assert Carrier Sense (CRS) on transmitting, only assert it on receiving 1_B Assert CRS on transmitting or receiving
SQE	2	RW	**Enable SQE Testing** Note: The Signal Quality Errors (SQE) test is automatically disabled in full-duplex mode regardless the setting in this bit. 0_B SQE test disabled 1_B SQE test enabled
POL	1	RW	**Enable Polarity Reversal** If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te. 0_B Polarity reversal disabled 1_B Polarity reversal enabled
JAB	0	RW	**Disable Jabber** Jabber takes effect only in 10BASE-Te half-duplex mode. 0_B Enable the jabber function 1_B Disable the jabber function

5.2.2 PHY Specific Status Register (Register 17)

This section describes the PHY Specific Status register in detail.

PHY Specific Status Register (Register 17)

The register reports PHY link, MDI crossover, polarity, ADS, and PAUSE status.

PHY_STAT	**Offset**	**Reset Value**
PHY Specific Status Register (Register 17)	**0011_H**	**0000_H**

15–14	13	12	11	10	9–7	6	5	4	3	2	1	0
SPEED	**DPX**	**PAGE**	**SDR**	**LSRT**	**RES**	**MDIXS**	**ADS**	**RES**	**TPS**	**RPS**	**POLRT**	**JABRT**
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
SPEED	15:14	RO	**Speed Mode** This register contains the speed mode status. These status bits are only valid when **PHY_STAT.SDR** is 1_B. **PHY_STAT.SDR** is set when auto-negotiation is completed or auto-negotiation is disabled. 00_B 10 Mbit/s 01_B 100 Mbit/s 10_B 1000 Mbit/s 11_B Reserved
DPX	13	RO	**Duplex** This register contains the duplex mode status. These status bits are only valid when **PHY_STAT.SDR** is 1_B. **PHY_STAT.SDR** is set when auto-negotiation is completed or auto-negotiation is disabled. 0_B Half-duplex 1_B Full-duplex
PAGE	12	RO	**Page Received Real-Time** 0_B Page not received 1_B Page received
SDR	11	RO	**Speed and Duplex Resolved** This field contains the status of whether the speed and duplex has been resolved. This bit is set when auto-negotiation is completed or disabled. When auto-negotiation is disabled (force-speed mode), this bit is set to 1_B. 0_B Not resolved 1_B Resolved
LSRT	10	RO	**Link Status Real-Time** 0_B Link down 1_B Link up
RES	9:7	RO	**Reserved**

Field	Bits	Type	Description (cont'd)
MDIXS	6	RO	**MDI Crossover Status** This field contains the MDI Crossover status. This bit value depends upon the **PHY_CTL.MDIX** (bits [6:5]) configuration. This status bit is only valid when the **PHY_STAT.SPEED** is 1_B. 0_B MDI 1_B MDIX
ADS	5	RO	**Wirespeed Downgrade** 0_B No Downgrade 1_B Downgrade
RES	4	RO	**Reserved**
TPS	3	RO	**Transmit Pause** This field contains the MAC pause resolution status. This bit is for information purposes only. When in forced mode, this bit is set to 0_B.This status bit is only valid when the **PHY_STAT.SPEED** is 1_B. 0_B Transmit pause disabled 1_B Transmit pause enabled
RPS	2	RO	**Receive Pause** This field contains the MAC pause resolution status. This bit is for information purposes only. When in forced mode, this bit is set to 0_B.This status bit is only valid when the **PHY_STAT.SPEED** is 1_B. 0_B Receive pause disabled 1_B Receive pause enabled
POLRT	1	RO	**Polarity Real Time** 0_B Normal polarity 1_B Reverted polarity
JABRT	0	RO	**Jabber Real Time** 0_B No jabber 1_B Jabber

5.2.3 Interrupt Mask Register (Register 18)

This section describes the Interrupt Mask Register in detail.

Interrupt Mask Register (Register 18)

This register defines the mask for the Interrupt Status Register, which contains the event source for INT_N sent from the PHY to an external device.

PHY_IMASK	**Offset**	**Reset Value**
Interrupt Mask Register (Register 18)	**0012_H**	**0000_H**

15	14	13	12	11	10	9:7	6	5	4	3	2	1	0
ANE	**LSPC**	**DXMC**	**NPRX**	**LFST**	**LSTC**	**RES**	**WOL**	**ADSC**	**RES**	**RES**	**RES**	**MDIPC**	**JAB**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ANE	15	RW	**Auto-Negotiation Error INT Mask** 0_B Interrupt disable 1_B Interrupt enable
LSPC	14	RW	**Speed Changed INT Mask** 0_B Interrupt disable 1_B Interrupt enable
DXMC	13	RW	**Duplex Changed INT Mask** 0_B Interrupt disable 1_B Interrupt enable
NPRX	12	RW	**Page Received INT Mask** 0_B Interrupt disable 1_B Interrupt enable
LFST	11	RW	**Link Failed INT Mask** 0_B Interrupt disable 1_B Interrupt enable
LSTC	10	RW	**Link Succeed INT Mask** 0_B Interrupt disable 1_B Interrupt enable
RES	9:7	RW	**Reserved** Not used.
WOL	6	RW	**WOL INT Mask** 0_B Interrupt disable 1_B Interrupt enable
ADSC	5	RW	**Link Speed Auto-Downspeed Detect Mask** 0_B Interrupt disable 1_B Interrupt enable
RES	4	RW	**Reserved** Not used.
RES	3	RW	**Reserved**

Field	Bits	Type	Description (cont'd)
RES	2	RW	**Reserved**
MDIPC	1	RW	**Polarity Changed INT Mask** 0_B Interrupt disable 1_B Interrupt enable
JAB	0	RW	**Jabber Occurred INT Mask** 0_B Interrupt disable 1_B Interrupt enable

5.2.4 Interrupt Status Register (Register 19)

This section describes the Interrupt Status Register in detail.

Interrupt Status Register (Register 19)

This register defines the event source for the MDINT interrupt sent from the PHY to an external device. The register is a cleared on read by the STA.

PHY_ISTAT	Offset	Reset Value
Interrupt Status Register (Register 19)	**0013_H**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANE	**LSPC**	**DXMC**	**NPRX**	**LFST**	**LSTC**	**RES**	**RES**	**RES**	**WOL**	**ADSC**	**RES**	**RES**	**RES**	**MDIPC**	**JAB**
ro rc	ro rc	ro rc	ro rc	ro rc	ro rc	ro rc	ro rc	ro rc	ro rc	ro rc	ro rc	ro rc	ro rc	ro rc	ro rc

Field	Bits	Type	Description
ANE	15	RO RC	**Auto-Negotiation Error INT** This field indicates errors occurring during ANEG. 0_B No auto-negotiation error takes place 1_B Auto-Negotiation error takes place
LSPC	14	RO RC	**Speed Changed INT** 0_B Speed not changed 1_B Speed changed
DXMC	13	RO RC	**Duplex Changed INT** 0_B Duplex not changed 1_B Duplex changed
NPRX	12	RO RC	**Page Received INT** 0_B Page not received 1_B Page received
LFST	11	RO RC	**Link Failed INT** 0_B No link down takes place 1_B PHY link down takes place
LSTC	10	RO RC	**Link Succeed INT** 0_B No link up takes place 1_B PHY link up takes place
RES	9	RO RC	**Reserved**
RES	8	RO RC	**Reserved**
RES	7	RO RC	**Reserved**
WOL	6	RO RC	**WOL INT** 0_B PHY did not receive WOL magic frame 1_B PHY received WOL magic frame.
ADSC	5	RO RC	**Link Speed Auto-Downspeed Detect Interrupt Status** 0_B Speed did not downgrade 1_B Speed downgraded
RES	4	RO RC	**Reserved**

Field	Bits	Type	Description (cont'd)
RES	3	RO RC	**Reserved**
RES	2	RO RC	**Reserved**
MDIPC	1	RO RC	**Polarity Changed INT** 0_B PHY did not revert MDI polarity 1_B PHY revered MDI polarity
JAB	0	RO RC	**Jabber Occurred INT** Refer to STD_STAT.JD. 0_B 10BaseT Tx jabber did not occur 1_B 10BaseT Tx jabber occurred

5.2.5 Speed Auto Downgrade Control Register (Register 20)

This section describes the Speed Auto Downgrade Control Register in detail.

Speed Auto Downgrade Control Register (Register 20)

The register is used for speed downshift control.

PHY_ADS_CTL	Offset	Reset Value
Speed Auto Downgrade Control Register (Register 20)	**0014_H**	**$0082c_H$**

15–12	11	10	9	8	7–6	5	4–2	1	0
RES	EML	REANEG	RANEG	DGA	RES	EADS	ADSRT	BAT	RES
ro	rw	rwsc	rw	rw	ro	rw	rw	rw	ro

Field	Bits	Type	Description
RES	15:12	RO	**Reserved**
EML	11	RW	**MDIO Latch Enable** 0_B Do not latch the MII/MMD register's read out value during MDIO read 1_B Latch the MII/MMD register's read out value during MDIO read
REANEG	10	RWSC	**Restart Auto-Negotiation** This field controls whether to force the PHY to restart the auto-negotiation process. 0_B Normal state 1_B Trigger restarting ANEG that automatically resets to 0 when auto-negotiation is complete.
RANEG	9	RW	**Reverse Auto-Negotiation** 0_B Normal autoneg direction 1_B Reverse the autoneg direction, 10 Mbit/s has 1st priority, then 100 Mbit/s and at last 1000 Mbit/s.
DGA	8	RW	**Gigabit Capability Disable** 0_B Do not disable so that the PHY advertises Gigabit capability based on the STD_GCTRL. 1_B Disable advertisement of Gigabit ability in AUTONEG.
RES	7:6	RO	**Reserved**
EADS	5	RW	**Auto Down Speed Enable** Link speed auto-downspeed is a functionality which allows an Ethernet link to be established even in non-standard harsh cable environments. This field only takes effect after a software reset. 0_B Disabled 1_B Enabled

Field	Bits	Type	**Description** (cont'd)
ADSRT	4:2	RW	**Autoneg Retry Limit Pre-downgrade** This field sets the number of link-up attempts before performing an Automatic-Downspeed (ADS) of the link. For example, with a 000_B setting, the PHY makes two attempts to link-up before trying a lower speed. (N+2). 000_B ADS after 2 consecutive link-up failures. 001_B ADS after 3 consecutive link-up failures. 010_B ADS after 4 consecutive link-up failures. 011_B ADS after 5 consecutive link-up failures. 100_B ADS after 6 consecutive link-up failures. 101_B ADS after 7 consecutive link-up failures. 110_B ADS after 8 consecutive link-up failures. 111_B ADS after 9 consecutive link-up failures.
BAT	1	RW	**Bypass Autospeed Timer** A link up that does not hold for 2.5 seconds is counted as a link fail, and the Auto-Downspeed retry counter increases by 1. The field only takes effect after a software reset. 0_B Do not bypass the timer 1_B Bypass the timer
RES	0	RO	**Reserved**

5.2.6 Extended Register's Address Offset Register (Register 30)

This section describes the Extended Register's Address Offset Register in detail.

Extended Register's Address Offset Register (Register 30)

The register is used in conjunction with the MDIO access to the extended register address field. This uses address directing as specified in the extended register chapter. See **Section 7.1** for more information.

PHY_EXT_ADR	**Offset**	**Reset Value**
Extended Register's Address Offset Register (Register 30)	**$001E_H$**	**0000_H**

15 … 0
EXTA
rw

Field	**Bits**	**Type**	**Description**
EXTA	15:0	RW	**Extended Register Address Offset** This is the address offset of the extended register that is read or written.

5.2.7 Extended Register's Data Register (Register 31)

This section describes the Extended Register's Data Register in detail.

Extended Register's Data Register (Register 31)

The register is used in conjunction with the MDIO access to the extended data field. The data format is defined as specified in the extended register chapter. This register holds the data to be written or read to the extended register (indicated in **Section 5.2.6**). See **Section 7.1** for more information.

PHY_EXT_DATA	Offset	Reset Value
Extended Register's Data Register (Register 31)	**$001F_H$**	**$1C8D_H$**

15 ... 0
EXTD
rw

Field	Bits	Type	Description
EXTD	15:0	RW	**Extended Register Data** This field contains the data to be written to, or read from, the extended register indicated by **Extended Register Address Offset** $001E_H$.

6 MMD Registers Detailed Description

Table 17 MMD Register Access Type

Mode	Symbol
Status Register (Status, or Ability Register)	RO
Read-Write Register (e.g. MDIO Register)	RW
Read-Write, Self-Clearing Register. The bit is cleared after being read from the MDIO interface.	RWSC

6.1 Standard PCS Registers for MMD=0003$_H$

This section describes the PCS registers for MMD device 0003$_H$.

Table 18 Registers Overview - Standard PCS Registers

Register Short Name	Register Long Name	Reset Value
PCS_STAT1	PCS status 1 (Register 3.1)	0000$_H$
PCS_EEE_CAP	PCS EEE capability (Register 3.20)	0006$_H$

6.1.1 Standard PCS Registers for MMD=0003_H

This chapter describes all registers of PCS in detail.

PCS status 1 (Register 3.1)

IEEE Standard Register=3.1

PCS_STAT1 **Reset Value**

PCS status 1 (Register 3.1) **0000_H**

15–12	11	10	9	8	7	6	5–3	2	1	0
RES	**TX_LPI_***	**RX_LPI_***	**TX_LPI_***	**RX_LPI_***	**FAULT**	**TXCKST**	**RES**	**PCS_RX_***	**LOW_POW***	**RES**
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
RES	15:12	RO	**Reserved**
TX_LPI_RXD	11	RO	**Tx Low Power Idle (LPI) Received** 0_B LPI not received 1_B Tx PCS has received LPI
RX_LPI_RXD	10	RO	**Rx LPI received** 0_B LPI not received Rx 1_B PCS has received LPI
TX_LPI_INDICATION	9	RO	**Tx LPI Indication** 0_B PCS is not currently receiving LPI 1_B Tx PCS is currently receiving LPI
RX_LPI_INDICATION	8	RO	**Rx LPI Indication** 0_B PCS is not currently receiving LPI 1_B Rx PCS is currently receiving LPI
FAULT	7	RO	**Fault** 0_B No fault condition detected 1_B Fault condition detected
TXCKST	6	RO	**Clock Stop Capable** 0_B Clock not stoppable 1_B The MAC has the ability to stop the clock during LPI
RES	5:3	RO	**Reserved**
PCS_RX_LINK_STATUS	2	RO	**PCS Receive Link Status** 0_B PCS receive link down 1_B PCS receive link up
LOW_POWER_ABILITY	1	RO	**Low-Power Ability** 0_B PCS does not support low-power mode 1_B PCS supports low-power mode
RES	0	RO	**Reserved**

PCS EEE Capability (Register 3.20)

IEEE Standard Register=3.20

PCS_EEE_CAP | **Reset Value**
PCS EEE Capability (Register 3.20) | **0006_H**

15–7	6	5	4	3	2	1	0
RES	R10GBAS*	R10GBAS*	R1000BA*	R10GBAS*	R1000BA*	R100BAS*	RES
ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
RES	15:7	RO	**Reserved**
R10GBASE_KR_EEE	6	RO	**10GBASE-KR EEE** 0_B EEE is not supported for 10GBASE-KR 1_B EEE is supported for 10GBASE-KR
R10GBASE_KX4_EEE	5	RO	**10GBASE-KX4 EEE** 0_B EEE is not supported for 10GBASE-KX4 1_B EEE is supported for 10GBASE-KX4
R1000BASE_KX_EEE	4	RO	**1000BASE-KX EEE** 0_B EEE is not supported for 1000BASE-KX 1_B EEE is supported for 1000BASE-KX
R10GBASE_T_EEE	3	RO	**10GBASE-T EEE** 0_B EEE is not supported for 10GBASE-T 1_B EEE is supported for 10GBASE-T
R1000BASE_T_EEE	2	RO	**1000BASE-T EEE** 0_B EEE is not supported for 1000BASE-T 1_B EEE is supported for 1000BASE-T
R100BASE_TX_EEE	1	RO	**100BASE-TX EEE** 0_B EEE is not supported for 100BASE-TX 1_B EEE is supported for 100BASE-TX
RES	0	RO	**Reserved**

6.2 Standard Auto-Negotiation Registers for MMD=0007_H

This register file contains the auto-negotiation registers for MMD device 0007_H.

Table 19 Registers Overview - Standard Auto-Negotiation Registers

Register Short Name	Register Long Name	Reset Value
ANEG_EEE_AN_ADV1	EEE Advertisement 1 (Register 7.60)	0000_H
ANEG_EEE_AN_LPAB1	EEE Link Partner Ability 1 (Register 7.61)	0000_H

6.2.1 Standard Auto-Negotiation Registers for MMD=0007$_H$

This section describes all registers of ANEG in detail.

EEE Advertisement 1 (Register 7.60)

IEEE Standard Register=7.60

ANEG_EEE_AN_ADV1 **Reset Value**

EEE Advertisement 1 (Register 7.60) **0000$_H$**

15–7	6	5	4	3	2	1	0
RES	**EEE_10G***	**EEE_10G***	**EEE_100***	**EEE_10G***	**EEE_100***	**EEE_100***	**RES**
ro	ro	ro	ro	ro	rw	rw	ro

Field	Bits	Type	Description
RES	15:7	RO	**Reserved**
EEE_10GBKR	6	RO	**Support of 10GBASE-KR EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBKX4	5	RO	**Support of 10GBASE-KX4 EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BKX	4	RO	**Support of 1000BASE-KX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBT	3	RO	**Support of 10GBASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BT	2	RW	**Support of 1000BASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_100BTX	1	RW	**Support of 100BASE-TX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
RES	0	RO	**Reserved**

EEE Link Partner Ability 1 (Register 7.61)

After the ANEG process is completed, this register reflects the contents of the link partner's EEE advertisement register. The definitions are thee same as the **ANEG_EEE_AN_ADV1** register.

IEEE Standard Register=7.61

All of the bits in the EEE LP ability 1 register are read-only. A write operation to the EEE LP advertisement register has no effect.

ANEG_EEE_AN_LPAB1 **Reset Value**
EEE Link Partner Ability 1 (Register 7.61) **0000_H**

15–7	6	5	4	3	2	1	0
RES	**EEE_10G***	**EEE_10G***	**EEE_100***	**EEE_10G***	**EEE_100***	**EEE_100***	**RES**
ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
RES	15:7	RO	**Reserved**
EEE_10GBKR	6	RO	**Support of 10GBASE-KR EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBKX4	5	RO	**Support of 10GBASE-KX4 EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BKX	4	RO	**Support of 1000BASE-KX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBT	3	RO	**Support of 10GBASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BT	2	RO	**Support of 1000BASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_100BTX	1	RO	**Support of 100BASE-TX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
RES	0	RO	**Reserved**

7 Extended Register Detailed Description

Table 20 Extended Register Access Type

Mode	Symbol
Status Register (Status, or Ability Register)	RO
Read-Write Register (e.g. MDIO Register)	RW
Read-Write, Self-Clearing Register. The bit is cleared after being read from the MDIO interface.	RWSC

7.1 Common Extended Register

This section describes the common extended registers.

Table 21 Registers Overview - Common Extended Register

Register Short Name	Register Long Name	Reset Value
COM_EXT_CHIP_CFG	Chip Configuration Register (Register A001H)	8140_H
COM_EXT_RGMII_CFG1	RGMII Configuration Register 1 (Register A003H)	$00F1_H$
COM_EXT_RGMII_CFG2	RGMII Configuration Register 2 (Register A004H)	0000_H
COM_EXT_RGMII_MDIO_CFG	RGMII In-Band Status and MDIO Configuration Register (Register A005H)	$00C0_H$
COM_EXT_MISC_CFG	Miscellaneous Control Register (Register A006H)	$000D_H$
COM_EXT_MAC_ADDR_CFG1	Wake on LAN Address Byte 5 and 6 (Register A007H)	0000_H
COM_EXT_MAC_ADDR_CFG2	Wake on LAN Address Byte 3 and 2 (Register A008H)	0000_H
COM_EXT_MAC_ADDR_CFG3	Wake on LAN Address Byte 1 and 0 (Register A009H)	0000_H
COM_EXT_WOL_CFG	Wake on LAN Control Register (Register A00AH)	0002_H
COM_EXT_LED_GEN_CFG	LED General Configuration Register (Register A00BH)	$E000_H$
COM_EXT_LED0_CFG	LED0 Configuration Register (Register A00CH)	0610_H
COM_EXT_LED1_CFG	LED1 Configuration Register (Register A00DH)	0620_H
COM_EXT_LED2_CFG	LED2 Configuration Register (Register A00EH)	0640_H
COM_EXT_LED BLINK_CFG	LED Blinking Configuration Register (Register A00FH)	0006_H
COM_EXT_PAD_STR_CFG	Pin Driving Strength Configuration Register (Register A010H)	$6BFF_H$
COM_EXT_SYNCE_CFG	SyncE Configuration Register (Register A012H)	$00C8_H$

7.1.1 Chip Configuration Register (Register A001$_H$)

This section describes the Chip Configuration Register in detail.

Chip Configuration Register (Register A001$_H$)

This register controls the chip mode and configuration.

COM_EXT_CHIP_CFG	Offset	Reset Value
Chip Configuration Register (Register A001H)	A001$_H$	8140$_H$

15	14–10	9	8	7	6	5–4	3	2–0
MCR	RES	GERXC	RXDLY	RES	ELDO	CLDO	RES	RES
rwsc	rw	rw	rw	ro	rw	rw	ro	rw

Field	Bits	Type	Description
MCR	15	RWSC	**Software Reset Mode** This MCR field resets the chip to change the mode. The bit is active low and self clearing. 0_B Reset 1_B No Reset (Default)
RES	14:10	RW	**Reserved**
GERXC	9	RW	**RGMII Rx Clock Enable** This GERXC field enables or disables the RGMII Rx clock no matter the link status of the TPI. 0_B Disable the RGMII Rx clock when the link is down. (Default) 1_B Enable the RGMII Rx clock when the link is down.
RXDLY	8	RW	**RGMII TX Clock Delay** This RXDLY field enables or disables the RGMII Rx clock delay. When enabled the delay is 2 ns for 125 MHz or 8 ns for 25 MHz and 2.5 MHz. The initial setting is defined by pin strapping. 0_B Disable the RGMII Rx clock delay. 1_B Enable the RGMII Rx clock delay. (Default)
RES	7	RO	**Reserved**
ELDO	6	RW	**LDO Enable** This ELDO field controls the RGMII LDO. Default is 0 and is set to 1 after power-on pin strapping is completed. 0_B Disable the LDO. 1_B Enable the LDO. (Default)
CLDO	5:4	RW	**LDO Configuration** This CLDO field sets the RGMII LDO voltage and RGMII/MDC/MDIO pin's level shifter control. The initial setting is defined by pin strapping. 00_B 3.3 V - Not regulated from 3.3 V. (Default) 01_B 2.5 V 10_B 1.8 V 11_B 1.8 V

Field	Bits	Type	Description (cont'd)
RES	3	RO	**Reserved**
RES	2:0	RW	**Reserved**

7.1.2 RGMII Configuration Register 1 (Register $A003_H$)

This section describes the RGMII Configuration Register 1 in detail.

RGMII Configuration Register 1 (Register $A003_H$)

This register controls the setting of RGMII interface.

COM_EXT_RGMII_CFG1	Offset	Reset Value
RGMII Configuration Register 1 (Register A003H)	**$A003_H$**	**$00F1_H$**

15–14	13–10	9	8	7–4	3–0
RES	**RDLYS**	**ERFC**	**ERC**	**TDSF**	**TDS**
rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RES	15:14	RW	**Reserved**
RDLYS	13:10	RW	**RGMII Rx Delay Select** This register controls the RGMII Rx clock delay training configuration. Each step adds approximately 150 ps of delay. 0000_B Disabled (Default) 0001_B 150 ps 0010_B 300 ps 0011_B 450 ps 0100_B 600 ps 0101_B 750 ps 0110_B 900 ps 0111_B 1050 ps 1000_B 1200 ps 1001_B 1350 ps 1010_B 1500 ps 1011_B 1650 ps 1100_B 1800 ps 1101_B 1950 ps 1110_B 2100 ps 1111_B 2250 ps
ERFC	9	RW	**Enable RGMII In-Band Full Duplex with CRS** This ERFC field in conjunction with the ERC field controls encoding of the GMII/MII CRS into RGMII In-band status. 0_B Encoding of GMII/MII CRS into RGMII In-band status is controlled by the ERC field. (Default) 1_B Encode GMII/MII CRS into RGMII In-band status if the field ERC is set to 1.

Field	Bits	Type	Description (cont'd)
ERC	8	RW	**Enable RGMII In-Band with CRS** This ERC field controls encoding of GMII/MII CRS into RGMII In-band status. 0_B Do not encode GMII/MII CRS into RGMII In-band status. (Default) 1_B Encode GMII/MII CRS into RGMII In-band status on half-duplex mode or if field ERFC is also set to 1.
TDSF	7:4	RW	**Fast Ethernet RGMII Tx Clock Delay Selection** This TDSF field configures the RGMII TX_CLK delay train for 100 Mbps or 10 Mbps link speed. Each step delays by about 150 ps. 0000_B Disabled 0001_B 150 ps 0010_B 300 ps 0011_B 450 ps 0100_B 600 ps 0101_B 750 ps 0110_B 900 ps 0111_B 1050 ps 1000_B 1200 ps 1001_B 1350 ps 1010_B 1500 ps 1011_B 1650 ps 1100_B 1800 ps 1101_B 1950 ps 1110_B 2100 ps 1111_B 2250 ps (Default)
TDS	3:0	RW	**Gigabit Ethernet RGMII Tx Clock Delay Selection** This TDS field configures the RGMII TX_CLK delay train for 1000 Mbps link speed. Each step delays by about 150 ps. 0000_B Disabled 0001_B 150 ps (Default) 0010_B 300 ps 0011_B 450 ps 0100_B 600 ps 0101_B 750 ps 0110_B 900 ps 0111_B 1050 ps 1000_B 1200 ps 1001_B 1350 ps 1010_B 1500 ps 1011_B 1650 ps 1100_B 1800 ps 1101_B 1950 ps 1110_B 2100 ps 1111_B 2250 ps

7.1.3 RGMII Configuration Register 2 (Register $A004_H$)

This section describes the RGMII Configuration Register 2 in detail.

RGMII Configuration Register 2 (Register $A004_H$)

This register is used for RGMII in-band status.

COM_EXT_RGMII_CFG2	Offset	Reset Value
RGMII Configuration Register 2 (Register A004H)	$A004_H$	0000_H

15–14	13	12	11–10	9	8	7–0
SPDP	DUPP	LNKP	PAUP	EEECP	EEECCP	RES
ro	ro	ro	ro	ro	ro	rw

Field	Bits	Type	Description
SPDP	15:14	RO	**RGMII PHY Speed Status** This SPDP field reports the RGMII interface speed information when configured as an RGMII PHY. This is also the source of RGMII In-band status communication. 00_B 10 Mbps (Default) 01_B 100 Mbps 10_B 1000 Mbps 11_B Reserved
DUPP	13	RO	**RGMII PHY Duplex Status** This DUPP field reports the RGMII interface duplex information when configured as an RGMII PHY. This is also the source of RGMII In-band status. 0_B Half-duplex (Default) 1_B Full-duplex
LNKP	12	RO	**RGMII PHY Link-up Status** This LNKP field reports the RGMII interface linkup information when configured as an RGMII PHY. This is also the source of RGMII In-band status. 0_B Link down (Default) 1_B Link up
PAUP	11:10	RO	**RGMII PHY Pause Information** This PAUP field reports the RGMII interface pause information when configured as an RGMII PHY. 00_B No asymmetric pause (Default) 10_B Asymmetric pause 10_B No Pause symmetric pause 11_B Symmetric pause

Field	Bits	Type	Description (cont'd)
EEECP	9	RO	**RGMII PHY EEE Capability** This EEECP field reports the capability of the RGMII interface for EEE when configured as RGMII PHY. 0_B This RGMII interface is not capable of EEE. (Default) 1_B This RGMII interface is capable of EEE.
EEECCP	8	RO	**RGMII PHY EEE Clock Stopping** This EEECCP field reports the capability of the RGMII interface for EEE clock stopping when configured as RGMII PHY. 0_B This RGMII interface is not capable of EEE clock stopping. (Default) 1_B This RGMII interface is capable of EEE clock stopping.
RES	7:0	RW	**Reserved**

7.1.4 RGMII In-Band Status and MDIO Configuration Register (Register $A005_H$)

This section describes the RGMII In-Band Status and MDIO Configuration Register in detail.

RGMII In-Band Status and MDIO Configuration Register (Register $A005_H$)

This register shows the RGMII in-band status and MDIO setting.

COM_EXT_RGMII_MDIO_CFG	Offset	Reset Value
RGMII In-Band Status and MDIO Configuration Register (Register A005H)	$A005_H$	$00C0_H$

15:12	11:7	6	5	4:0
RES	RES	EPA0	EBA	BA
rw	ro	rw	rw	rw

Field	Bits	Type	Description
RES	15:12	RW	**Reserved**
RES	11:7	RO	**Reserved** Reserved The default is 0_B.
EPA0	6	RW	**Enable PHY Address 0 Broadcast Responses** This field controls whether the PHY responds to the MDIO interface's broadcasts access from PHY address 0. 0_B Disabled 1_B Enabled (Default)
EBA	5	RW	**Enable PHY BA Broadcast Responses** This field controls whether the PHY responds to broadcasts from a PHY address defined in **COM_ETX_RGMII_MIDO_CFG.BA**. 0_B Disabled 1_B Enabled (Default)
BA	4:0	RW	**Broadcast Address** This BA field defines the address for accepting broadcast access response. The default is 0_B.

7.1.5 Miscellaneous Control Register (Register $A006_H$)

This section describes the Miscellaneous Control Register in detail.

Miscellaneous Control Register (Register $A006_H$)

This register controls miscellaneous PHY settings.

COM_EXT_MISC_CFG	Offset	Reset Value
Miscellaneous Control Register (Register A006H)	$A006_H$	$000D_H$

15:8	7	6	5	4	3	2:0
RES	JE	RES	RLBP	RES	BGFR	RES
rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RES	15:8	RW	**Reserved**
JE	7	RW	**Jumbo Frame Enable** This JE field controls the use of jumbo frames. 0_B Jumbo frames are disabled. (Default) 1_B Jumbo frames are enabled.
RES	6	RW	**Reserved**
RLBP	5	RW	**PHY Remote Loopback** This RLBP field controls setting of remote loopback for PHY. 0_B Disabled (Default) 1_B Enabled
RES	4	RW	**Reserved**
BGFR	3	RW	**Bypass GMII Overflow and Reset** This BGFR field controls whether to bypass the GMII FIFO overflow and underflow RST. 0_B Enable to reset GMII FIFO automatic when overflow or underflow happens. 1_B Disable to reset GMII FIFO when overflow or underflow happen. (Default)
RES	2:0	RW	**Reserved**

7.1.6 Wake on LAN Address Byte 5 and 6 (Register $A007_H$)

This section describes the Wake on LAN Address Byte 5 and 6 registers in detail.

Wake on LAN Address Byte 5 and 6 (Register $A007_H$)

This register holds the WoL MAC address's bytes 4 and 5.

COM_EXT_MAC_ADDR_CFG1	Offset	Reset Value
Wake on LAN Address Byte 5 and 6 (Register A007H)	**$A007_H$**	**0000_H**

15 … 0
MALH
rw

Field	Bits	Type	Description
MALH	15:0	RW	**MAC Address Location 47-32** This MALH field holds the first two octets of the MAC address used for WOL. The default is 0_B.

7.1.7 Wake on LAN Address Byte 3 and 2 (Register $A008_H$)

This section describes the Wake on LAN Address Byte 3 and 2 registers in detail.

Wake on LAN Address Byte 5 and 6 (Register $A008_H$)

This register holds the WoL MAC address's bytes 3 and 2.

COM_EXT_MAC_ADDR_CFG2	Offset	Reset Value
Wake on LAN Address Byte 3 and 2 (Register A008H)	**$A008_H$**	**0000_H**

15 ... 0
MALM
rw

Field	Bits	Type	Description
MALM	15:0	RW	**MAC Address Location 31-16** This MALM field holds the middle two octets of the MAC address used for WOL. The default is 0_B.

7.1.8 Wake on LAN Address Byte 1 and 0 (Register $A009_H$)

This section describes the Wake on LAN Address Byte 1 and 0 registers in detail.

Wake on LAN Address Byte 1 and 0 (Register $A009_H$)

This register holds the WoL MAC address's bytes 1 and 0.

COM_EXT_MAC_ADDR_CFG3	Offset	Reset Value
Wake on LAN Address Byte 1 and 0 (Register A009H)	**$A009_H$**	**0000_H**

15 … 0

MALL

rw

Field	Bits	Type	Description
MALL	15:0	RW	**MAC Address Location 15-0** This MALL field holds the last two octets of the MAC address used for WOL. The default is 0_B.

7.1.9 Wake on LAN Control Register (Register $A00A_H$)

This section describes the Wake on LAN Control Register in detail.

Wake on LAN Address Byte 1 and 0 (Register $A00A_H$)

This register configures the WoL function.

COM_EXT_WOL_CFG	Offset	Reset Value
Wake on LAN Control Register (Register A00AH)	**$A00A_H$**	**0002_H**

15–8	7	6–4	3	2–0
RES	SCR	RES	WOLE	RES
ro	rw	rw	rw	rw

Field	Bits	Type	Description
RES	15:8	RO	**Reserved** Reserved The default is 0_B.
SCR	7	RW	**RGMII Enable** This SCR field enables or disables the RGMII interface. 0_B Enable the RGMII interface. (Default) 1_B Disable the RGMII interface.
RES	6:4	RW	**Reserved**
WOLE	3	RW	**WOL Enable** This WOLE field controls the operation mode of the Wake-on-LAN feature. 0_B WOL is disabled. (Default) 1_B WOL is enabled.
RES	2:0	RW	**Reserved**

7.1.10 LED General Configuration Register (Register A00B$_H$)

This section describes the LED General Configuration Register in detail.

LED General Configuration Register (Register A00B$_H$)

This register controls the LED general configuration.

COM_EXT_LED_GEN_CFG	Offset	Reset Value
LED General Configuration Register (Register A00BH)	A00B$_H$	E000$_H$

15	14	13	12	11:9	8	7:6	5	4:3	2	1:0
COLBS	JABLD	LPLD	DLDT	RES	L2FE	L2FM	L1FE	L1FM	L0FE	L0FM
rw	rw	rw	rw	ro	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
COLBS	15	RW	**LED Collision Blink Frequency** This COLBS field controls the collision LED blinking frequency. The blink function is only value if **COM_EXT_LED0_CFG.LCBE0**, **COM_EXT_LED1_CFG.LCBE0**, or **COM_EXT_LED0_CFG.LCBE0** is set to 1$_B$. 0$_B$ When a collision occurs, blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ1. 1$_B$ When a collision occurs, blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ2. (Default)
JABLD	14	RW	**LED Jabber Blink** This JABLD field controls LED blinking on a jabber condition. 0$_B$ Blinking under jabber conditions. 1$_B$ No blinking under jabber conditions. (Default)
LPLD	13	RW	**LED Loopback Display** This LPLD field controls whether the LED should indicate an internal loopback condition. 0$_B$ Blinking under loopback conditions. 1$_B$ No blinking under loopback conditions. (Default)
DLDT	12	RW	**Auto-Negotiation Display** This DLDT field controls whether the LED should indicate the auto-negotiation state. 0$_B$ Blinking when auto-negotiation is at LINK_GOOD_CHECK condition. It means the link is not yet ready. (Default) 1$_B$ No blinking to indicate auto-negotiation state.
RES	11:9	RO	**Reserved** Reserved The default is 0$_B$.

Field	Bits	Type	Description (cont'd)
L2FE	8	RW	**LED2 Force Enable** This L2FE field controls the enable of LED2 force mode defined in the L2FM field. 0_B Disable LED2 force mode. (Default) 1_B Enable LED2 force mode.
L2FM	7:6	RW	**LED2 Force Mode** This L2FM field controls the LED2 blink pattern in force mode. Force mode is enabled with the L2FE bit. 00_B Force the LED off. (Default) 01_B Force the LED on. 10_B Force the LED to blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ1. 11_B Force the LED to blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ2.
L1FE	5	RW	**LED1 Force Enable** This L1FE field controls the enable of LED1 force mode defined in the L1FM field. 0_B Disable LED1 force mode. (Default) 1_B Enable LED1 force mode.
L1FM	4:3	RW	**LED1 Force Mode** This L1FM field controls the LED1 blink pattern in force mode. Force mode is enabled with the L1FE bit. 00_B Force the LED off. (Default) 01_B Force the LED on. 10_B Force the LED to blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ1. 11_B Force the LED to blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ2.
L0FE	2	RW	**LED0 Force Enable** This L0FE field controls the enable of LED0 force mode defined in the L0FM field. 0_B Disable LED0 force mode. (Default) 1_B Enable LED0 force mode.
L0FM	1:0	RW	**LED0 Force Mode** This L0FM field controls the LED0 blink pattern in force mode. Force mode is enabled with the L0FE bit. 00_B Force the LED off. (Default) 01_B Force the LED on. 10_B Force the LED to blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ1. 11_B Force the LED to blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ2.

7.1.11 LED0 Configuration Register (Register A00C$_H$)

This section describes the LED0 Configuration Register in detail.

LED0 Configuration Register (Register A00C$_H$)

This register configures LED0.

COM_EXT_LED0_CFG	Offset	Reset Value
LED0 Configuration Register (Register A00CH)	A00C$_H$	0610$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		LAB0	LFDE0	LHDE 0	LTAB E0	LRAB E0	LTAE0	LRAE 0	LGE0	LFE0	LBE0	LCBE 0	LGBE 0	LFBE0	LBBE 0
rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RES	15:14	RW	**Reserved**
LAB0	13	RW	**LED0 Activity Blink Indicator** This field configures LED blinking when there is traffic activity no matter LED under constant on or off state. 0$_B$ LED0 only blinks at Link LED0 under ON state. (Default) 1$_B$ LED0 blinks no matter LED0 is under ON or OFF state.
LFDE0	12	RW	**LED0 Full-Duplex Status** This field control LED to show full-duplex status. 0$_B$ No full-duplex status support. (Default) 1$_B$ When the PHY link is up and the duplex mode is full-duplex, LED0 is ON. If the LED also has blink setting, the Blink setting has a higher priority.
LHDE0	11	RW	**LED0 Half-Duplex Status** This LHDE0 field controls how LED0 indicates half-duplex status. 0$_B$ Half-duplex mode is not indicated. (Default) 1$_B$ When the PHY link is up and the duplex mode is half-duplex, LED0 is ON. If the LED also has blink setting, the Blink setting has a higher priority.
LTABE0	10	RW	**LED0 Tx Activity Blink** This LTABE0 field controls how LED0 indicates Tx activity status. 0$_B$ Tx activity is not indicated. 1$_B$ When the PHY link is up and Tx activity occurs, LED0 blinks at the frequency defined in field COM_EXT_LED_BLINK_CFG.LFEQ2 in the COM_EXT_LED_BLINK_CFG register. (Default)
LRABE0	9	RW	**LED0 Rx Activity Blink** This LRABE0 field controls how LED0 indicates Rx activity status. 0$_B$ Rx activity is not indicated. 1$_B$ When the PHY link is up and Rx activity occurs LED0 blinks at the frequency defined in field COM_EXT_LED_BLINK_CFG.LFEQ2 in the COM_EXT_LED_BLINK_CFG register. (Default)

Field	Bits	Type	Description (cont'd)
LTAE0	8	RW	**LED0 Tx Activity Minimum On Time** This LTAE0 field controls a minimum ON time for LED0 when Tx is active. 0_B No minimum ON time for LED0 when Tx is active. (Default) 1_B When the PHY link is up and Tx is active, LED0 is ON for at least 10 ms. If the LED also has a blink setting for Tx activity the blink setting has a higher priority.
LRAE0	7	RW	**LED0 Rx Activity Minimum On Time** This LRAE0 field controls a minimum ON time for LED0 when Rx is active. 0_B No minimum ON time for LED0 when Rx is active. (Default) 1_B When the PHY link is up and Rx is active, LED0 is ON for at least 10 ms. If the LED also has a blink setting for Rx activity the blink setting has a higher priority.
LGE0	6	RW	**LED0 1000Base-T Ethernet Link Behavior** This LGE0 field controls how LED0 indicates 1000 Mbps link speed. 0_B No change to LED0 behavior. (Default) 1_B When the PHY link up is and the speed mode is 1000 Mbps, LED0 is ON. If the LED also has a blink setting the blink setting has a higher priority.
LFE0	5	RW	**LED0 100Base-T Ethernet Link Behavior** This LFE0 field controls how LED0 indicates 100 Mbps link speed. 0_B No change to LED0 behavior. (Default) 1_B When the PHY link is up and the speed mode is 100 Mbps, LED0 is ON. If the LED also has blink setting the blink setting has a higher priority.
LBE0	4	RW	**LED0 10Base-T Ethernet Link Behavior** This LBE0 field controls how LED0 indicates 10 Mbps link speed. 0_B No change to LED0 behavior. 1_B When the PHY link up and the speed mode is 10 Mbps, LED0 is ON. If the LED also has blink setting the blink setting has a higher priority. (Default)
LCBE0	3	RW	**LED0 Collision Behavior** This LCBE0 field controls how LED0 indicates collisions. 0_B No change to LED0 behavior. (Default) 1_B When the PHY link is up and a collision occurs, blink LED0.
LGBE0	2	RW	**LED0 1000Base-T Ethernet Link Blink** This LGBE0 field controls how LED0 indicates 1000 Mbps link speed. 0_B No change to LED0 behavior. (Default) 1_B When the PHY link is up and the speed mode is 1000 Mbps, blink LED0.
LFBE0	1	RW	**LED0 100Base-T Ethernet Link Blink** This LFBE0 field controls how LED0 indicates 100 Mbps link speed. 0_B No change to LED0 behavior. (Default) 1_B When the PHY link is up and the speed mode is 100 Mbps, blink LED0.

Field	Bits	Type	Description (cont'd)
LBBE0	0	RW	**LED0 10Base-T Ethernet Link Blink** This LBBE0 field controls how LED0 indicates 10 Mbps link speed. 0_B No change to LED0 behavior. (Default) 1_B When the PHY link up and the speed mode is 10 Mbps, LED0 blink.

7.1.12 LED1 Configuration Register (Register $A00D_H$)

This section describes the LED1 Configuration Register in detail.

LED1 Configuration Register (Register $A00D_H$)

This register configures LED1.

COM_EXT_LED1_CFG	Offset	Reset Value
LED1 Configuration Register (Register A00DH)	$A00D_H$	0620_H

15:14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES	**LAB1**	**LFDE1**	**LHDE1**	**LTABE1**	**LRABE1**	**LTAE1**	**LRAE1**	**LGE1**	**LFE1**	**LBE1**	**LCBE1**	**LGBE1**	**LFBE1**	**LBBE1**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RES	15:14	RW	**Reserved**
LAB1	13	RW	**LED1 Activity Blink Indicator** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LFDE1	12	RW	**LED1 Full-Duplex Status** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LHDE1	11	RW	**LED1 Half-Duplex Status** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LTABE1	10	RW	**LED1 Tx Activity Blink** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 1_B.
LRABE1	9	RW	**LED1 Rx Activity Blink** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 1_B.
LTAE1	8	RW	**LED0 Tx Activity Minimum On Time** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LRAE1	7	RW	**LED1 Rx Activity Minimum On Time** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LGE1	6	RW	**LED1 1000Base-T Ethernet Link Behavior** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LFE1	5	RW	**LED1 100Base-T Ethernet Link Behavior** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 1_B.

Field	Bits	Type	Description (cont'd)
LBE1	4	RW	**LED1 10Base-T Ethernet Link Behavior** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LCBE1	3	RW	**LED1 Collision Behavior** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LGBE1	2	RW	**LED1 1000Base-T Ethernet Link Blink** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LFBE1	1	RW	**LED1 100Base-T Ethernet Link Blink** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LBBE1	0	RW	**LED1 10Base-T Ethernet Link Blink** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.

7.1.13 LED2 Configuration Register (Register $A00E_H$)

This section describes the LED2 Configuration Register in detail.

LED2 Configuration Register (Register $A00E_H$)

This register configures LED2.

COM_EXT_LED2_CFG	Offset	Reset Value
LED2 Configuration Register (Register A00EH)	$A00E_H$	0640_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		LAB2	LFDE2	LHDE2	LTABE2	LRABE2	LTAE2	LRAE2	LGE2	LFE2	LBE2	LCBE2	LGBE2	LFBE2	LBBE2
rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RES	15:14	RW	**Reserved**
LAB2	13	RW	**LED2 Activity Blink Indicator** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LFDE2	12	RW	**LED2 Full-Duplex Status** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LHDE2	11	RW	**LED2 Half-Duplex Status** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LTABE2	10	RW	**LED2 Tx Activity Blink** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 1_B.
LRABE2	9	RW	**LED2 Rx Activity Blink** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 1_B.
LTAE2	8	RW	**LED2 Tx Activity Minimum On Time** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LRAE2	7	RW	**LED2 Rx Activity Minimum On Time** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LGE2	6	RW	**LED2 1000Base-T Ethernet Link Behavior** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 1_B.
LFE2	5	RW	**LED2 100Base-T Ethernet Link Behavior** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.

Field	Bits	Type	Description (cont'd)
LBE2	4	RW	**LED2 10Base-T Ethernet Link Behavior** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LCBE2	3	RW	**LED2 Collision Behavior** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LGBE2	2	RW	**LED2 1000Base-T Ethernet Link Blink** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LFBE2	1	RW	**LED2 100Base-T Ethernet Link Blink** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.
LBBE2	0	RW	**LED2 10Base-T Ethernet Link Blink** Same as LED0. See the COM_EXT_LED0_CFG description. The default is 0_B.

7.1.14 LED Blinking Configuration Register (Register A00F$_H$)

This section describes the LED Blinking Configuration Register in detail.

LED Blinking Configuration Register (Register A00F$_H$)

This register configures the LED blink frequency.

COM_EXT_LED BLINK_CFG	Offset	Reset Value
LED Blinking Configuration Register (Register A00FH)	A00F$_H$	0006$_H$

15–7	6–4	3–2	1–0
RES	LDTY	LFEQ2	LFEQ1
ro	rw	rw	rw

Field	Bits	Type	Description
RES	15:7	RO	**Reserved** Reserved The default is 0$_B$.
LDTY	6:4	RW	**LED Duty Cycle** This LDTY field configures the blink duty cycle. 000$_B$ 50% on and 50% off. (Default) 001$_B$ 67% on and 33% off. 010$_B$ 75% on and 25% off. 011$_B$ 83% on and 17% off. 100$_B$ 50% on and 50% off. 101$_B$ 33% on and 67% off. 110$_B$ 25% on and 75% off. 111$_B$ 17% on and 83% off.
LFEQ2	3:2	RW	**LED Blink Mode 2 Frequency** This LFEQ2 field configures the blink frequency for blink mode 2. 00$_B$ 2 Hz 01$_B$ 4 Hz (Default) 10$_B$ 8 Hz 11$_B$ 16 Hz
LFEQ1	1:0	RW	**LED Blink Mode 1Frequency** This LFEQ1 field configures the blink frequency for blink mode 1. 00$_B$ 2 Hz 01$_B$ 4 Hz 10$_B$ 8 Hz (Default) 11$_B$ 16 Hz

7.1.15 Pin Driving Strength Configuration Register (Register $A010_H$)

This section describes the Pin Driving Strength Configuration Register in detail.

LED Blinking Configuration Register (Register $A010_H$)

This register sets the pin interface's I/O drive strength.

COM_EXT_PAD_STR_CFG	Offset	Reset Value
Pin Driving Strength Configuration Register (Register A010H)	**$A010_H$**	**$6BFF_H$**

15:13	12	11	10	9:8	7:6	5:4	3:2	1:0
RSDR	RSD2	IODE	IAHL	DSE	DM	RSD10	DII	DL
rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RSDR	15:13	RW	**RGMII Rx Clock Pin Drive Strength** Sets the drive strength of the RX_CLK pin. 000_B Weakest 111_B Strongest
RSD2	12	RW	**Drive Strength of RGMII Data and Control** This RGMII_SW_DR2 field holds bit 2 of the drive strength of the RXD/RX_CTL pin. See **COM_EXT_PAD_STR_CFG.RGMII_SW_DR10**. 000_B Weakest 111_B Strongest
IODE	11	RW	**Interrupt Output Open Drain Enable** This IODE field controls the interrupt pin output mode. 0_B This interrupt pin acts as a push-pull output. 1_B This interrupt pin acts as open drain.
IAHL	10	RW	**Interrupt Polarity Active High** This IAHL field configures the interrupt line polarity sensitivity. 0_B The interrupt line is low-active. 1_B The interrupt line is high-active.
DSE	9:8	RW	**SyncE Pin Drive Strength** Sets the drive strength of the SyncE pin. 00_B Weakest 11_B Strongest (Default)
DM	7:6	RW	**MDIO Pin Drive Strength** Sets the drive strength of the MDIO pin. 00_B Weakest 11_B Strongest

Field	Bits	Type	Description (cont'd)
RSD10	5:4	RW	**Drive Strength of RGMII Data and Control** This RGMII_SW_DR10 field sets the drive strength of the RXD/RX_CTL pin. This field holds bit 1 and bit 0. Bit 2 is held in **COM_EXT_PAD_STR_CFG.RGMII_SW_DR2**. 000_B Weakest 111_B Strongest
DII	3:2	RW	**Interrupt Pin Drive Strength** Sets the drive strength of the interrupt pin. 00_B Weakest 11_B Strongest
DL	1:0	RW	**LED Pin Drive Strength** Sets the drive strength of GPHY_LED0, GPHY_LED1, and GPHY_LED2. 00_B Weakest 11_B Strongest

7.1.16 Pin Driving Strength Configuration Register (Register $A012_H$)

This section describes the Pin Driving Strength Configuration Register in detail.

Pin Driving Strength Configuration Register (Register $A012_H$)

This register sets the pin interface's I/O drive strength.

COM_EXT_SYNCE_CFG	Offset	Reset Value
SyncE Configuration Register (Register A012H)	$A012_H$	$00C8_H$

15–8	7	6	5	4	3–1	0
RES	PF	ESE	ESEDN	CFS	CSS	RES
ro	rw	rw	rw	rw	rw	ro

Field	Bits	Type	Description
RES	15:8	RO	**Reserved**
PF	7	RW	**PHY to Fiber** This PF field controls UTP activation. 0_B Always enable UTP. 1_B In UTP to FIBER mode, do not enable UTP until the fiber link is up. (Default)
ESE	6	RW	**SyncE Output Control** This ESE field controls the SyncE clock output. 0_B Disable SyncE clock output. 1_B Enable SyncE clock output. (Default)
ESEDN	5	RW	**Enable SyncE Clock Output under No Link** This ESEDN field controls SyncE clock output behavior in link down state. 0_B No SyncE clock output when the link is down. (Default) 1_B Force SyncE clock output when the link is down.
CFS	4	RW	**SyncE Clock Frequency Select** This CFS field selects the clock frequency. 0_B 25 MHz. (Default) 1_B 125 MHz.
CSS	3:1	RW	**SyncE Clock Source Select** This CSS field select the clock source for generating SyncE clock output. 000_B Use the internal 125 MHz PLL as the output clock. 001_B Use the TPI recovered clock. 010_B Reserved 011_B Use the RGMII Tx clock. 100_B Use the reference 25 MHz clock. (Default) 101_B Use 25 MHz with SSC.
RES	0	RO	**Reserved**

7.2 UTP Extended Register

This section describes the UTP extended register.

Table 22 Registers Overview - UTP Extended Register

Register Short Name	Register Long Name	Reset Value
UTP_EXT_10BT_DBG	10 M Base-Te Debug Mode Register (Register 000AH)	1000_H
UTP_EXT_SLEEP_CTRL	Sleep Mode Control Register (Register 0027H)	$E812_H$
UTP_EXT_PKG_RX_VALID_0	Packet Rx Valid High Register (Register 00A3H)	0000_H
UTP_EXT_PKG_RX_VALID_1	Packet Rx Valid Low Register (Register 00A4H)	0000_H
UTP_EXT_PKG_RX_OS_0	Packet Rx Oversize High Register (Register 00A5H)	0000_H
UTP_EXT_PKG_RX_OS_1	Packet Rx Oversize Low Register (Register 00A6H)	0000_H
UTP_EXT_PKG_RX_US_0	Packet Rx Undersize High Register (Register 00A7H)	0000_H
UTP_EXT_PKG_RX_US_1	Packet Rx Undersize Low Register (Register 00A8H)	0000_H
UTP_EXT_PKG_RX_ERR	Packet Rx CRC Register (Register 00A9H)	0000_H
UTP_EXT_PKG_RX_OS_BAD	Packet Rx CRC Oversize Register (Register 00AAH)	0000_H
UTP_EXT_PKG_RX_FRAGMENT	Packet Rx Fragment Register (Register 00ABH)	0000_H
UTP_EXT_PKG_RX_NOSFD	Packet Rx No SFD Register (Register 00ACH)	0000_H
UTP_EXT_PKG_TX_VALID_0	Packet Tx High Register (Register 00ADH)	0000_H
UTP_EXT_PKG_TX_VALID_1	Packet Tx Low Register (Register 00AEH)	0000_H
UTP_EXT_PKG_TX_OS_0	Packet Tx Oversize High Register (Register 00AFH)	0000_H
UTP_EXT_PKG_TX_OS_1	Packet Tx Oversize Low Register (Register 00B0H)	0000_H
UTP_EXT_PKG_TX_US_0	Packet Tx Undersize High Register (Register 00B1H)	0000_H
UTP_EXT_PKG_TX_US_1	Packet Tx Undersize Low Register (Register 00B2H)	0000_H
UTP_EXT_PKG_TX_ERR	Packet Tx CRC Register (Register 00B3H)	0000_H
UTP_EXT_PKG_TX_OS_BAD	Packet Tx CRC Oversize Register (Register 00B4H)	0000_H
UTP_EXT_PKG_TX_FRAGMENT	Packet Tx Fragment Register (Register 00B5H)	0000_H
UTP_EXT_PKG_TX_NOSFD	Packet Tx No SFD Register (Register 00B6H)	0000_H

7.2.1 10 M Base-Te Debug Mode Register (Register $000A_H$)

This section describes the 10 M Base-Te Debug Mode Register in detail.

10 M Base-Te Debug Mode Register (Register $000A_H$)

This register is used for 10 Base-T mode IEEE compliance and external loopback testing.

UTP_EXT_10BT_DBG	Offset	Reset Value
10 M Base-Te Debug Mode Register (Register 000AH)	$000A_H$	1000_H

15–14	13–5	4	3	2–0
RES	RES	ELB	RES	TM10
ro	rw	rw	rw	rw swc

Field	Bits	Type	Description
RES	15:14	RO	**Reserved** Reserved The default is 0_B.
RES	13:5	RW	**Reserved**
ELB	4	RW	**External Loopback Control** This field enables/disables the external loopback. 1_B Enable the external loopback. 0_B Disable the external loopback. (Default)
RES	3	RW	**Reserved**
TM10	2:0	RW SWC	**10Base-T Ethernet Test Mode** This field configures the 10Base-Te test modes. 000_B Normal operation (Default) 101_B Normal operation 110_B Normal operation 111_B Normal operation 001_B Used for IEEE harmonic test with 10 MHz sine wave and packets with "all ones". 010_B Enables a pseudo random packet for TP_IDLE/Jitter/Differential Voltage testing. 011_B Enables a "normal" link pulse 110_B Used to generate a 5 MHz sine wave

7.2.2 Sleep Mode Control Register (Register 0027_H)

This section describes the Sleep Mode Control Register in detail.

Sleep Mode Control Register (Register 0027_H)

This register configures the power saving mode.

UTP_EXT_SLEEP_CTRL	Offset	Reset Value
Sleep Mode Control Register (Register 0027H)	**0027_H**	**$E812_H$**

15	14	13	12 11	10 6	5	4 0
ESS	PLIS	SPS	RES	RES	SLP	RES
rw	rw	rw	rw	ro	ro	ro

Field	Bits	Type	Description
ESS	15	RW	**Sleep Mode Control** This field enables/disables the sleep mode feature of the PHY. In sleep mode, the PHY automatically disables AFE when the TPI has no link after a amount of certain time. 0_B Disables the sleep mode feature. 1_B Enables the sleep mode feature. (Default)
PLIS	14	RW	**Sleep Mode PLL Control** This field configures the PLL in the sleep mode of the PHY. 0_B PLL stops in sleep mode. (Default) 1_B PLL remains active in sleep mode.
SPS	13	RW	**Sleep Mode Periodic Pulse Control** This field configures the PHY sending periodic pulse signal in sleep mode. 0_B Disables sending periodic pulses. 1_B Enables sending periodic pulses. (Default)
RES	12:11	RW	**Reserved**
RES	10:6	RO	**Reserved** Reserved The default is 0_B.
SLP	5	RO	**Sleep Status** This SLP field reports the status of the PHY. 0_B PHY is enabled. (Default) 1_B PHY is in sleep mode.
RES	4:0	RO	**Reserved**

7.2.3 Packet Rx Valid High Register (Register $00A3_H$)

This section describes the Packet Rx Valid High Register in detail.

Packet Rx Valid High Register (Register $00A3_H$)

This register is used for debugging Rx packets.

UTP_EXT_PKG_RX_VALID_0	Offset	Reset Value
Packet Rx Valid High Register (Register 00A3H)	**$00A3_H$**	**0000_H**

15		0
	PIVH	
	ro rc	

Field	Bits	Type	Description
PIVH	15:0	RO RC	**Rx Packet Valid Count High** This PIVH field reports the number of Rx packets from line to PHY side with correct CRC and a packet length >= 64 bytes and <= 1518 bytes. These are the upper 16-bits of a 32-bit value. The lower 16-bits are in **UTP_EXT_PKG_RX_OS_1.PIVL**. The default is 0_B.

7.2.4 Packet Rx Valid Low Register (Register $00A4_H$)

This section describes the Packet Rx Valid Low Register in detail.

Packet Rx Valid Low Register (Register $00A4_H$)

This register is used for debugging Rx packets.

UTP_EXT_PKG_RX_VALID_1	Offset	Reset Value
Packet Rx Valid Low Register (Register 00A4H)	**$00A4_H$**	**0000_H**

15 … 0
PIVL
ro rc

Field	Bits	Type	Description
PIVL	15:0	RO RC	**Rx Packet Valid Count Low** This PIVL field reports the number of Rx packets from line to PHY side with correct CRC and a packet length >= 64 bytes and <= 1518 bytes. These are the lower 16-bits of a 32-bit value. The upper 16-bits are in **UTP_EXT_PKG_RX_VALID_0.PIVH**. The default is 0_B.

7.2.5 Packet Rx Oversize High Register (Register $00A5_H$)

This section describes the Packet Rx Oversize High Register in detail.

Packet Rx Valid Low Register (Register $00A5_H$)

This register is used for debugging Rx packets.

UTP_EXT_PKG_RX_OS_0	Offset	Reset Value
Packet Rx Oversize High Register (Register 00A5H)	**$00A5_H$**	**0000_H**

15 ... 0
PIOGH
ro rc

Field	Bits	Type	Description
PIOGH	15:0	RO RC	**Oversize Rx Packet Count High** This PIOGH field represents the number of Rx packets from line to PHY side with correct CRC and a packet length > 1518 bytes. These are the upper 16-bits of a 32-bit value. The lower 16-bits are in **UTP_EXT_PKG_RX_OS_1.PIOGL**. The default is 0_B.

7.2.6 Packet Rx Oversize Low Register (Register $00A6_H$)

This section describes the Packet Rx Oversize Low Register in detail.

Packet Rx Valid Low Register (Register $00A6_H$)

This register is used for debugging Rx packets.

UTP_EXT_PKG_RX_OS_1	Offset	Reset Value
Packet Rx Oversize Low Register (Register 00A6H)	**$00A6_H$**	**0000_H**

15 … 0
PIOGL
ro rc

Field	Bits	Type	Description
PIOGL	15:0	RO RC	**Oversize Rx Packet Count Low** This PIOGL field represents the number of Rx packets from line to PHY side with correct CRC and a packet length > 1518 bytes. These are the lower 16-bits of a 32-bit value. The upper 16-bits are in **UTP_EXT_PKG_RX_OS_0.PIOGH**. The default is 0_B.

7.2.7 Packet Rx Undersize High Register (Register 00A7$_H$)

This section describes the Packet Rx Undersize High Register in detail.

Packet Rx Undersize High Register (Register 00A7$_H$)

This register is used for debugging Rx packets.

UTP_EXT_PKG_RX_US_0	Offset	Reset Value
Packet Rx Undersize High Register (Register 00A7H)	**00A7$_H$**	**0000$_H$**

15		0
	PIUGH	
	ro rc	

Field	Bits	Type	Description
PIUGH	15:0	RO RC	**Good Rx Packet Count High** This PIUGH field represents the number of Rx packets from line to PHY side with correct CRC and a packet length < 64 bytes.These are the upper 16-bits of a 32-bit value. The lower 16-bits are in **UTP_EXT_PKG_RX_US_1.PIUGL**. The default is 0_B.

7.2.8 Packet Rx Undersize Low Register (Register $00A8_H$)

This section describes the Packet Rx Undersize Low Register in detail.

Packet Rx Undersize Low Register (Register $00A8_H$)

This register is used for debugging Rx packets.

UTP_EXT_PKG_RX_US_1	Offset	Reset Value
Packet Rx Undersize Low Register (Register 00A8H)	**$00A8_H$**	**0000_H**

15 ... 0
PIUGL
ro rc

Field	Bits	Type	Description
PIUGL	15:0	RO RC	**Good Rx Packet Count Low** This PIUGL field represents the number of Rx packets from line to PHY side with correct CRC and a packet length < 64 bytes.These are the lower 16-bits of a 32-bit value. The upper 16-bits are in **UTP_EXT_PKG_RX_US_0.PIUGH**. The default is 0_B.

7.2.9 Packet Rx CRC Register (Register $00A9_H$)

This section describes the Packet Rx CRC Register in detail.

Packet Rx CRC Register (Register $00A9_H$)

This register is used for debugging Rx packets.

UTP_EXT_PKG_RX_ERR	**Offset**	**Reset Value**
Packet Rx CRC Register (Register 00A9H)	**$00A9_H$**	**0000_H**

15		0
	PIE	
	ro rc	

Field	Bits	Type	Description
PIE	15:0	RO RC	**Rx Packet Error Count** This PIE field represents the number of Rx packets from line to PHY side with corrupted CRC and a packet length >= 64 bytes and <= 1518 bytes. The default is 0_B.

7.2.10 Packet Rx CRC Oversize Register (Register $00AA_H$)

This section describes the Packet Rx CRC Oversize Register in detail.

Packet Rx CRC Oversize Register (Register $00AA_H$)

This register is used for debugging Rx packets.

UTP_EXT_PKG_RX_OS_BAD	Offset	Reset Value
Packet Rx CRC Oversize Register (Register 00AAH)	**$00AA_H$**	**0000_H**

15 ... 0
PIOB
ro rc

Field	Bits	Type	Description
PIOB	15:0	RO RC	**Rx Oversize Packet CRC Error Count** This field represents the number of Rx packets from line to PHY side with corrupted CRC and a packet length >= 1518 bytes. The default is 0_B.

7.2.11 Packet Rx Fragment Register (Register $00AB_H$)

This section describes the Packet Rx Fragment Register in detail.

Packet Rx CRC Oversize Register (Register $00AB_H$)

This register is used for debugging Rx packets.

UTP_EXT_PKG_RX_FRAGMENT	Offset	Reset Value
Packet Rx Fragment Register (Register 00ABH)	**$00AB_H$**	**0000_H**

15 … 0
PIF
ro rc

Field	Bits	Type	Description
PIF	15:0	RO RC	**Rx Fragment Packet Error Count** This field represents the number of Rx packets from line to PHY side with corrupted CRC and a packet length <=64 bytes. The default is 0_B.

7.2.12 Packet Rx No SFD Register (Register $00AC_H$)

This section describes the Packet Rx No SFD Register in detail.

Packet Rx CRC Oversize Register (Register $00AC_H$)

This register is used for debugging Rx packets.

UTP_EXT_PKG_RX_NOSFD	Offset	Reset Value
Packet Rx No SFD Register (Register 00ACH)	**$00AC_H$**	**0000_H**

15		0
	PINF	
	ro rc	

Field	Bits	Type	Description
PINF	15:0	RO RC	**Rx Packet Missing Start Frame Delimiter Count** This PINF field represents the number of Rx packets from line to PHY side, with missing Start Frame Delimiter (SFD). The default is 0_B.

7.2.13 Packet Tx High Register (Register $00AD_H$)

This section describes the Packet Tx High Register in detail.

Packet Rx CRC Oversize Register (Register $00AD_H$)

This register is used for debugging Tx packets.

UTP_EXT_PKG_TX_VALID_0	Offset	Reset Value
Packet Tx High Register (Register 00ADH)	**$00AD_H$**	**0000_H**

15		0
	POVH	
	ro rc	

Field	Bits	Type	Description
POVH	15:0	RO RC	**Tx Packet Valid Count High** This POVH field represents the number of Tx packets sending from PHY GMII interface with correct CRC and a packet length >= 64 bytes and <=1518 bytes. These are the upper 16-bits of a 32-bit value. The lower 16-bits are in **UTP_EXT_PKG_TX_VALID_1.POVL**. The default is 0_B.

7.2.14 Packet Tx Low Register (Register $00AE_H$)

This section describes the Packet Tx Low Register in detail.

Packet Tx Low Register (Register $00AE_H$)

This register is used for debugging Tx packets.

UTP_EXT_PKG_TX_VALID_1	Offset	Reset Value
Packet Tx Low Register (Register 00AEH)	$00AE_H$	0000_H

15 … 0
POVL
ro rc

Field	Bits	Type	Description
POVL	15:0	RO RC	**Tx Packet Valid Count Low** This POVL field represents the number of Tx packets from PHY GMII interface with correct CRC and a packet length >= 64 bytes and <=1518 bytes. These are the lower 16-bit of a 32-bit value. The higher 16-bit are in the field **UTP_EXT_PKG_TX_VALID_0.POVH**. The default is 0_B.

7.2.15 Packet Tx Oversize High Register (Register 00AF$_H$)

This section describes the Packet Tx Oversize High Register in detail.

Packet Tx Oversize High Register (Register 00AF$_H$)

This register is used for debugging Tx packets.

UTP_EXT_PKG_TX_OS_0	Offset	Reset Value
Packet Tx Oversize High Register (Register 00AFH)	**00AF$_H$**	**0000$_H$**

15 … 0
POOGH
ro rc

Field	Bits	Type	Description
POOGH	15:0	RO RC	**Oversize Tx Packet Count High** This POOGH field represents the number of Tx packets from PHY GMII interface with correct CRC and a packet length > 1518 bytes. These are the upper 16-bits of a 32-bit value. The lower 16-bits are **UTP_EXT_PKG_TX_OS_1.POOGL**. The default is 0_B.

7.2.16 Packet Tx Oversize Low Register (Register $00B0_H$)

This section describes the Packet Tx Oversize Low Register in detail.

Packet Tx Oversize Low Register (Register $00B0_H$)

This register is used for debugging Tx packets.

UTP_EXT_PKG_TX_OS_1	Offset	Reset Value
Packet Tx Oversize Low Register (Register 00B0H)	**$00B0_H$**	**0000_H**

15 ... 0
POOGL
ro rc

Field	Bits	Type	Description
POOGL	15:0	RO RC	**Oversize Tx Packet Count Low** This POOGL field represents the number of Tx packets from PHY GMII interface with correct CRC and a packet length > 1518 bytes. These are the lower 16-bits of a 32-bit value. The upper 16-bits are **UTP_EXT_PKG_TX_OS_0.POOGH**. The default is 0_B.

7.2.17 Packet Tx Undersize High Register (Register 00B1$_H$)

This section describes the Packet Tx Undersize High Register in detail.

Packet Tx Oversize Low Register (Register 00B1$_H$)

This register is used for debugging Tx packets.

UTP_EXT_PKG_TX_US_0	**Offset**	**Reset Value**
Packet Tx Undersize High Register (Register 00B1H)	**00B1$_H$**	**0000$_H$**

15 … 0
POUGH
ro rc

Field	Bits	Type	Description
POUGH	15:0	RO RC	**Good Tx Packet Count High** This POUGH field represents the number of Tx packets from PHY GMII interface with correct CRC and a packet length < 64 bytes. These are the upper 16-bits of a 32-bit value. The lower 16-bits are in **UTP_EXT_PKG_TX_US_1.POUGL**. The default is 0$_B$.

7.2.18 Packet Tx Undersize Low Register (Register 00B2$_H$)

This section describes the Packet Tx Undersize Low Register in detail.

Packet Tx Undersize Low Register (Register 00B2$_H$)

This register is used for debugging Tx packets.

UTP_EXT_PKG_TX_US_1	Offset	Reset Value
Packet Tx Undersize Low Register (Register 00B2H)	**00B2$_H$**	**0000$_H$**

15 ... 0
POUGL
ro rc

Field	Bits	Type	Description
POUGL	15:0	RO RC	**Good Tx Packet Count Low** This POUGL field represents the number of Tx packets from PHY GMII interface with correct CRC and a packet length > 1518 bytes. These are the lower 16-bits of a 32-bit value. The upper 16-bits are in **UTP_EXT_PKG_TX_US_0.POUGH**. The default is 0$_B$.

7.2.19 Packet Tx CRC Register (Register $00B3_H$)

This section describes the Packet Tx CRC Register in detail.

Packet Tx Undersize Low Register (Register $00B3_H$)

This register is used for debugging Tx packets.

UTP_EXT_PKG_TX_ERR	Offset	Reset Value
Packet Tx CRC Register (Register 00B3H)	**$00B3_H$**	**0000_H**

15 ... 0
POE
ro rc

Field	Bits	Type	Description
POE	15:0	RO RC	**Tx Packet Error Count** This POE field represents the number of Tx packets from PHY GMII interface with wrong CRC and a packet length >= 64 bytes and <= 1518 bytes. The default is 0_B.

7.2.20 Packet Tx CRC Oversize Register (Register $00B4_H$)

This section describes the Packet Tx CRC Oversize Register in detail.

Packet Tx CRC Oversize Register (Register $00B4_H$)

This register is used for debugging Tx packets.

UTP_EXT_PKG_TX_OS_BAD	Offset	Reset Value
Packet Tx CRC Oversize Register (Register 00B4H)	**$00B4_H$**	**0000_H**

15 … 0
POOB
ro rc

Field	Bits	Type	Description
POOB	15:0	RO RC	**Tx Oversize Packet CRC Error Count** This POOB field represents the number of Tx packets from PHY GMII interface with wrong CRC and a packet length > 1518 bytes. The default is 0_B.

7.2.21 Packet Tx Fragment Register (Register 00B5$_H$)

This section describes the Packet Tx Fragment Register in detail.

Packet Tx Fragment Register (Register 00B5$_H$)

This register is used for debugging Tx packets.

UTP_EXT_PKG_TX_FRAGMENT	Offset	Reset Value
Packet Tx Fragment Register (Register 00B5H)	**00B5$_H$**	**0000$_H$**

15 ... 0
POF
ro rc

Field	Bits	Type	Description
POF	15:0	RO RC	**Tx Fragment Packet Error Count** This POF field represents the number of Tx packets from PHY GMII interface with a packet length < 64 bytes. The default is 0$_B$.

7.2.22 Packet Tx No SFD Register (Register $00B6_H$)

This section describes the Packet Tx No SFD Register in detail.

Packet Tx No SFD Register (Register $00B6_H$)

This register is used for debugging Tx packets.

UTP_EXT_PKG_TX_NOSFD	Offset	Reset Value
Packet Tx No SFD Register (Register 00B6H)	$00B6_H$	0000_H

15 … 0
PONF
ro rc

Field	Bits	Type	Description
PONF	15:0	RO RC	**Tx Packet Missing Start Frame Delimiter Count** This PONF field represents the number of Tx packets from PHY GMII interface, with missing SFD. The default is 0_B.

8 Electrical Characteristics

This chapter provides the electrical characteristics for the MxL86110.

8.1 Absolute Maximum Ratings

Table 23 provides the absolute maximum ratings.

Table 23 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage Temperature Limits	T_{STG}	–	–	40	°C	Devices should be stored according to these criteria: - The temperature must be less than 40 °C. - The relative humidity must be less than 90%. Before removing the devices from the moisture barrier bag, ensure that there is no condensation in the air.
Soldering Temperature	T_{SOL}	–	–	260	°C	Solder the devices with lead-free (Pb) solder that complies with J-STD-020D
Moisture Level 3 Temperature Limits	T_{ML3}	–	–	260	°C	According to IPS J-STD 020
Absolute Junction Temperature	T_{JABS}	–	–	125	°C	–
VDD3V3/VDDDAV3	V_{max}	-0.3	–	3.7	V	–
VDDA1V1/VDD	V_{max}	-0.2	1.1	1.4	V	–
2.5 V RGMII	V_{max}	-0.3	2.5	2.8	V	–
1.8 V RGMII	V_{max}	-0.3	1.8	2.3	V	–
3.3 V DC Input	V_{max}	-0.3	3.1	3.7	V	–
VDD/VDDA1V1 DC Input	V_{max}	-0.3	1.1	1.4	V	–

Attention: Stresses above the maximum values listed in this table may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.

8.2 Operating Range

Table 24 defines the maximum values of voltages and temperature that must be applied to guarantee proper operation of the Gigabit Ethernet PHY. The values are relative to a ground voltage source supply (VSS) of 0.0 V.

Table 24 Supply Voltage and Temperature

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VDD3V3/VDDDAV3	V_{max}	2.97	3.3	3.63	V	–
VDDA1V1/VDD	V_{max}	1.045	1.1	1.32	V	–
2.5 V RGMII	V_{max}	2.25	2.5	2.75	V	–
1.8 V RGMII	V_{max}	1.62	1.8	1.98	V	–
Maximum Operating Junction Temperature	T_{JMAX}	–	–	125	°C	–
3.3 V Minimum High Level Output Voltage	V_{OH}	2.4	–	3.63	V	–
3.3 V Maximum Low Level Output Voltage	V_{OL}	-0.3	–	0.4	V	–
2.5 V Minimum High Level Output Voltage	V_{OH}	2	–	2.8	V	–
2.5 V Maximum Low Level Output Voltage	V_{OL}	-0.3	–	0.4	V	–
1.8 V Minimum High Level Output Voltage	V_{OH}	1.62	–	2.1	V	–
1.8 V Maximum Low Level Output Voltage	V_{OL}	-0.3	–	0.4	V	–
3.3 V Minimum High Level Input Voltage	V_{IH}	2	–	–	V	–
3.3 V Maximum Low Level Input Voltage	V_{IL}	–	–	0.8	V	–
2.5 V Minimum High Level Input Voltage	V_{IH}	1.7	–	–	V	–
2.5 V Maximum Low Level Input Voltage	V_{IL}	–	–	0.7	V	–
1.8 V Minimum High Level Input Voltage	V_{IH}	1.2	–	–	V	–
1.8 V Maximum Low Level Input Voltage	V_{IL}	–	–	0.5	V	–

8.3 AC Characteristics

The following sections describe the AC characteristics of the external interfaces as well as the power up and power down sequence.

8.3.1 Power Up and Power Down Sequence

Figure 12 shows the power up and power down sequence.

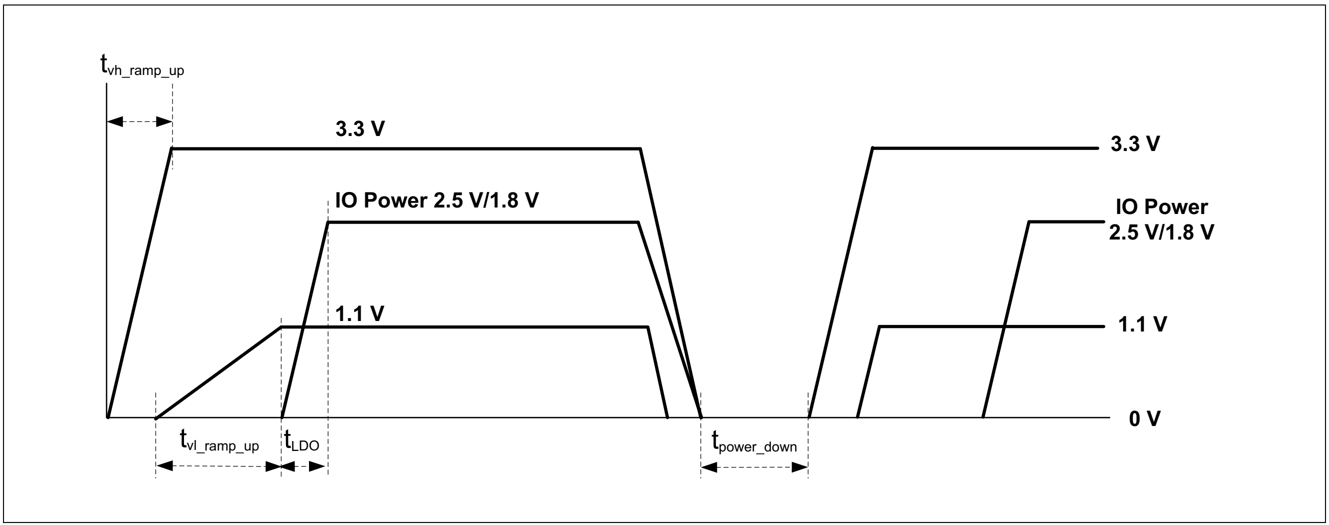

Figure 12 Power Up and Power Down Sequence

Note: When 1.1 V in external supply mode, the sequence for 3.3 V and 1.1 V can be powered up at the same time. The 1.1 V power supply must always be lower than 3.3 V power supply.

Table 25 Sequence Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
3.3 V Rising Time	Tvh_ramp_up	0.5	–	–	ms	–
3.3 V and 1.1 V Power-Down Duration	Tpower_down	100	–	–	ms	–
Core Power 1.1 V Ready Time	Tvl_ramp_up	–	–	2.5	ms	–
Internal LDO Ready Time	TLDO	–	–	100	us	–

8.3.2 Power Supply Rail Requirements

The maximum noise per power rail must be under these limits:

- 3.3 V: < 100 mV peak-to-peak
- VDD (1.1 V): < 80 mV peak-to-peak
- VDDA (1.1 V): < 50 mV peak-to-peak

8.3.3 Device Power Consumption

Table 26 and Table 27 show the power consumption for the MxL86110.

Power consumption at 25 °C ambient temperature is indicated in Table 26 for the different modes. The Link-up conditions are full-speed, bidirectional, and full-duplex. Power numbers are indicated for internal DCDC SVR.

Table 26 Device Power Consumption

Condition 25 °C 100 m Cable	VDDP (mA)	VDD3V3 (mA)	VDDA3V3 (mA)	Power Consumption (mW)
Link Down	1	7	21	95.7
Link Up at 1000 Mbps	13	51	61	412.5
Traffic at 1000 Mbps	28	57	61	481.8

Note: Test by typical corner chip with VDDP/VDD3V3/VDDA3V3 = 3.3 V and VDD/VDDA1V1 = 1.1 V under room temperature.

Table 27 Maximum Device Power Consumption

Condition 85 °C 100 m Cable	VDDP (mA)	VDD3V3 (mA)	VDDA3V3 (mA)	Power Consumption (mW)
Traffic at 1000 Mbps	30.8	62.7	67.1	530

Note: Test by fast corner chip with VDDP/VDD3V3/VDDA3V3 = 3.3 V and VDD/VDDA1V1 = 1.1 V at 85 °C.

8.3.4 MDIO Interface

Figure 13 shows a timing diagram of the slave MDIO interface for a clock cycle in the read, write, and turnaround modes. The timing measurements are annotated. The defined absolute values are summarized in Table 28.

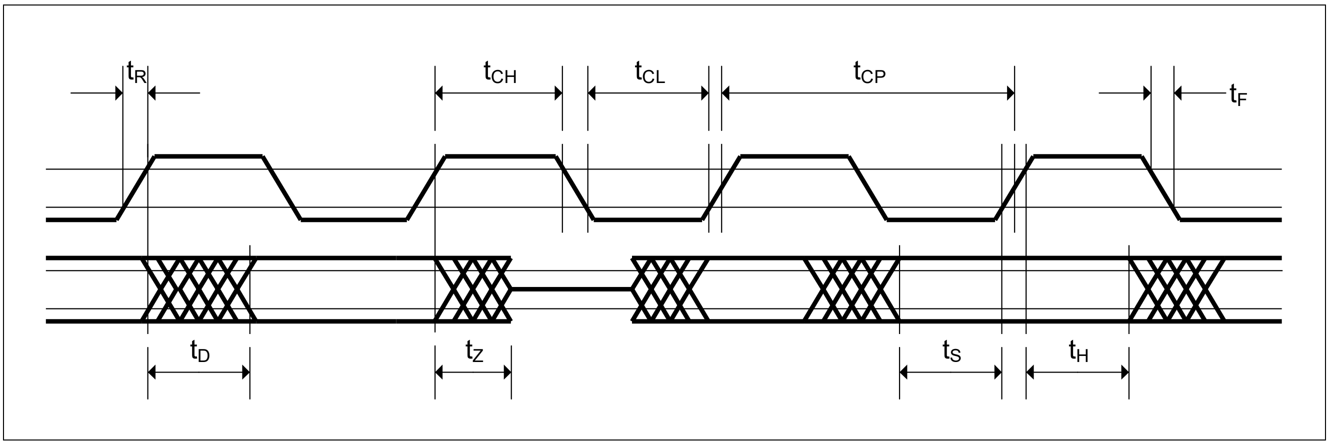

Figure 13 Timing Diagram for the MDIO Interface

Table 28 Timing Characteristics of the MDIO Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MDC High Time	t_{CH}	32.0	–	–	ns	All provided timings were captured from a probe attached to the MDC pin of the device.
MDC Low Time	t_{CL}	32.0	–	–	ns	
MDC Clock Period	t_{CP}	80.0	–	–	ns	
MDC Clock Frequency[1)]	t_{CP}	–	2.5	12.5	MHz	
MDC Rise Time	t_R	–	–	10.0	ns	
MDC Fall Time	t_F	–	–	10.0	ns	
MDIO Input Setup Time	t_S	10.0	–	–	ns	Gigabit Ethernet PHY receive
MDIO Input Hold Time	t_H	10.0	–	–	ns	Gigabit Ethernet PHY receive
MDIO Output Delay Time	t_D	0.0	–	20	ns	Gigabit Ethernet PHY transmit
MDIO Output Setup Time	t_S	10.0	–	–	ns	MAC transmit
MDIO Output Hold Time	t_H	10.0	–	–	ns	MAC transmit

1) MDC clock supports range of frequencies up to 12.5 MHz. The typical (and default) frequency is 2.5 MHz.

8.3.5 RGMII Interface

This section describes the AC characteristics of the RGMII interface on the MxL86110. This interface conforms to the RGMII specification version 1.3 and version 2.0, as defined in [2] and [3] respectively. The RGMII interface operates at speeds of 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s.

8.3.5.1 Transmit Timing Characteristics

Figure 14 shows the timing diagram of the transmit RGMII interface on the MxL86110. **Table 29** provides the RGMII timing requirements. Note the data and control signals are clocked in using the internal delayed version of the TX_CLK which is the external clock delayed by the integrated delay. The delay is adjustable in steps of 0.15 ns. This amount is configurable using the COM_EXT_RGMII_CFG1 register. See **Section 7.1**. An additional 2 ns of delay is available via pin strapping. See **Section 3.16**.

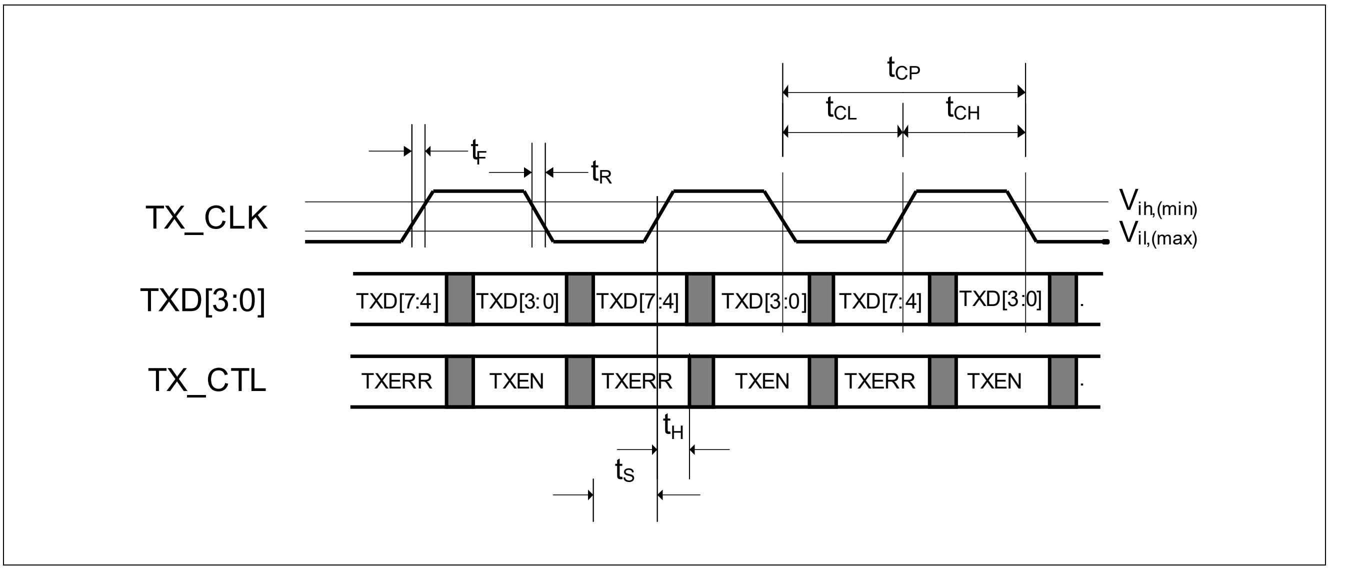

Figure 14 RGMII Transmit Timing Diagram

Table 29 RGMII Transmit Timing Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transmit Clock Frequency (TX_CLK)	f_{TX_CLK}	-50 ppm	125.0	+50 ppm	MHz	For 1000 Mbit/s speed
			25.0		MHz	For 100 Mbit/s speed
			2.5		MHz	For 10 Mbit/s speed
Transmit Clock Period (TX_CLK)	t_{CP}	7.2	8.0	8.8	ns	For 1000 Mbit/s speed
		36.0	40.0	44.0	ns	For 100 Mbit/s speed
		360.0	400.0	440.0	ns	For 10 Mbit/s speed
Duty Cycle	t_{CH}/t_{CP}, t_{CL}/t_{CP}	45.0	50.0	55.0	%	Speed-independent
Transmit Clock Rise Time (TX_CLK)	t_R	–	–	750.0	ps	20%→80%
Transmit Clock Fall Time (TX_CLK)	t_F	–	–	750.0	ps	80%→20%
Setup Time to ↑↓ TX_CLK	t_S	1.0	–	–	ns	–

Table 29 RGMII Transmit Timing Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Hold Time to ↑↓ TX_CLK	t_H	1.0	–	–	ns	–
Integrated Transmit Clock Delay	t_{ID}	0.0	k*0.15	4.25	ns	Adjustable via COM_EXT_RGMII_CFG1 and the TXDLY pin strapping

8.3.5.2 Receive Timing Characteristics

Figure 15 shows the timing diagram of the receive RGMII interface on the MxL86110. It is referred to by **Table 30**, which specifies the timing requirements. The external clock on the pin is delayed by the integrated delay, which is adjustable in steps of 0.15 ns. This amount is configurable using the COM_EXT_RGMII_CFG1 register. See **Section 7.1**. An additional 2 ns of delay is available via pin strapping. See **Section 3.16**. If the integrated delay is not used it must be set to zero, in which case all the timings are related directly to the RX_CLK on the pin.

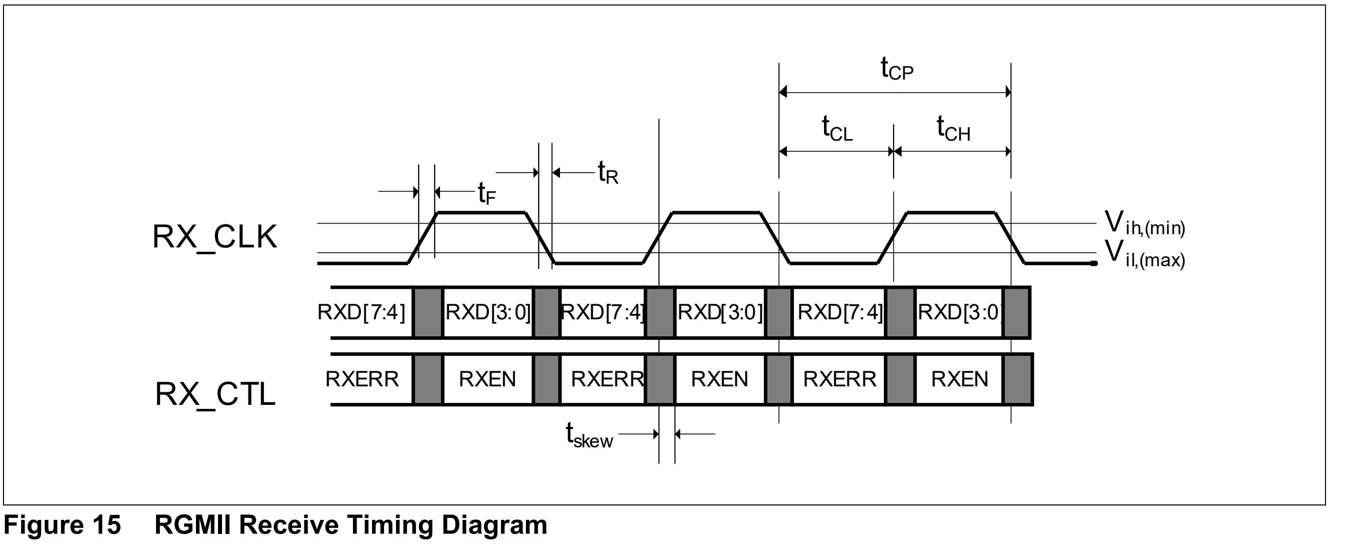

Figure 15 RGMII Receive Timing Diagram

Table 30 RGMII Receive Timing Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive Clock Frequency (RX_CLK)	f_{RX_CLK}	-50 ppm	125.0	+50 ppm	MHz	For 1000 Mbit/s speed
			25.0		MHz	For 100 Mbit/s speed
			2.5		MHz	For 10 Mbit/s speed
Receive Clock Period (RX_CLK)	t_{CP}	7.2	8.0	8.8	ns	For 1000 Mbit/s speed
		36	40.0	46	ns	For 100 Mbit/s speed
		360	400.0	460	ns	For 10 Mbit/s speed
Duty Cycle	t_{CH}/t_{CP}, t_{CL}/t_{CP}	45.0	50.0	55.0	%	Speed-independent
Receive Clock Rise Time (TX_CLK)	t_R	–	–	750.0	ps	20% → 80%
Receive Clock Fall Time (TX_CLK)	t_F	–	–	750.0	ps	80% → 20%

Table 30 RGMII Receive Timing Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock-to-Data Skew	t_{skew}	-0.5	0.0	0.5	ns	The skew between the RXC and RXC/RX_CTL should be less than 500 ps
Integrated Receive Clock Delay	t_{ID}	0.0	k*0.15	4.25	ns	Adjustable via COM_EXT_RGMII_CFG1 and the RXDLY pin strapping

8.3.6 Crystal Specification

The 25 MHz crystal must follow the specification given in **Table 31**.

Table 31 Specification of the Crystal

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	**Typ.**	**Max.**		
Frequency with 25 MHz Input	f_{clk25}	–	25.0	–	MHz	–
Total Frequency Stability[1)]	–	-50	–	+50	ppm	–
Series Resonant Resistance	–	–	–	50	Ω	–
Drive Level	–	–	–	0.5	mW	–
Crystal Output High Level	V_{ih}	1.4	–	–	V	–
Crystal Output Low Level	V_{il}	–	–	0.7	V	–

1) Total frequency stability refers to the sum all effects, not limited to general tolerance, aging, and temperature influences.

8.3.7 External Clock Requirements

Table 32 shows the external clock requirements.

Table 32 Specification of the External Clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency with 25 MHz Input	f_{clk25}	–	25.0	–	MHz	–
Total Frequency Stability	–	-50	–	+50	ppm	–
Duty Cycle	–	40	–	60	%	–
Crystal Output High	V_{ih}	1.4	–	VDDA3V3+0.3	V	–
Crystal Output Low	V_{il}	–	–	0.7	V	–
Rise Time (10% - 90%)	–	–	–	10	ns	–
Fall Time (10% - 90%)	–	–	–	10	ns	–

9 Package Outline

The MxL86110 device is available in a 40-pin QFN package with an exposed pin (EPAD). The pin pitch is 0.4 mm and the size of the EPAD is 3.7 x 3.7 mm. The EPAD is used as the common ground and must be connected to the PCB ground plane. The package is a lead-free “green package”, and its exact name for reference purposes is PG-QFN-40.

Table 33 provides the mechanical dimensions of the PG-QFN-40 package. **Figure 16** shows the top, side, and bottom dimension drawings of the package.

Table 33 PG-QFN-40 Mechanical Dimensions

Parameter		Symbol	Minimum	Nominal	Maximum
Total Thickness		A	0.80	0.85	0.95
Stand Off		A1	0	0.02	0.05
Mold Thickness		A2	-	0.65	-
L/F Thickness		A3	0.203 Ref		
Lead Width		b	0.15	0.20	0.25
Body Size	**X**	D	5.00 BSC		
	Y	E	5.00 BSC		
Lead Pitch		e	0.40 BSC		
EP Size	**X**	D2	3.60	3.70	3.80
	Y	E2	3.60	3.70	3.80
Lead Length		L	0.30	0.40	0.50

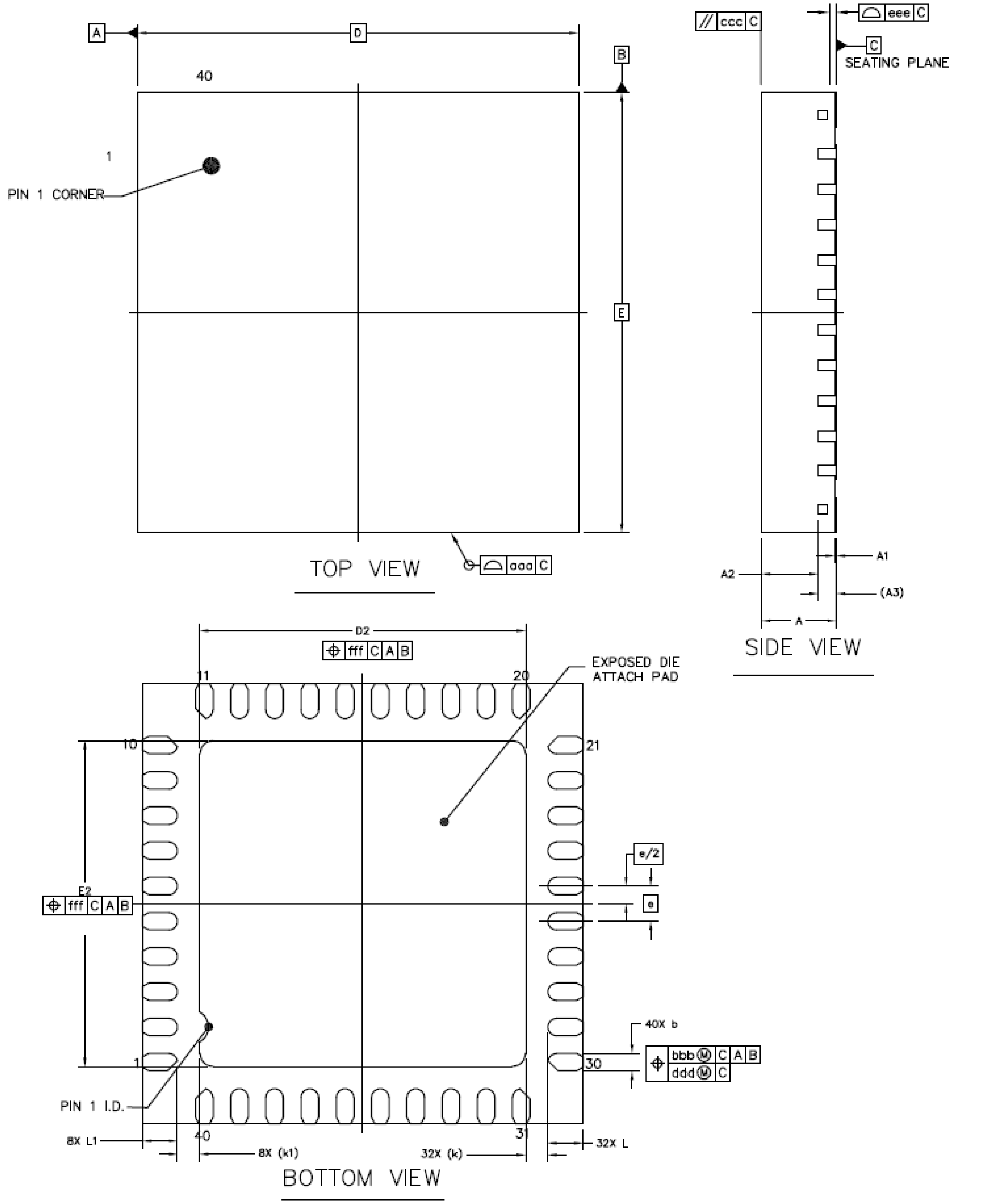

Figure 16 PG-QFN-40 Mechanical Drawing

9.1 Thermal Resistance

Table 2 shows the package thermal resistance values.

Table 34 Thermal Resistance

Symbol	Parameter	Condition	Typ	Units
θ_{JA}	Thermal resistance - junction to ambient $\theta_{JA} = (T_J - T_A)/ P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow TA=25 °C	33.4	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow TA=85 °C	31	°C/W
θ_{JB}	Thermal resistance - junction to board $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = Power dissipation from the bottom of the package to the PCB surface	JEDEC with no air flow	12.3	°C/W
$\theta_{JC\text{-}Top}$	Thermal resistance - junction to case $\theta_{JC} = (T_J - T_C)/ P_{top}$ P_{top} = Power dissipation from the top of the package	JEDEC with no air flow	28.4	°C/W

9.2 Chip Identification and Ordering Information

Figure 17 shows an example of the marking pattern on the MxL86110 device.

Figure 17 Chip Marking

Table 35 explains the chip marking information.

Table 35 Chip Marking Pattern

Marking	Description
MxL	MaxLinear Logo
AAAAA	MaxLinear Part Number
BBBBBB	Wafer Lot Number
XX	First wafer number in assembly lot, such as 01
YY	Year
WW	Work Week
S	Supplier Manufacturing Code

Table 36 provides the chip ordering information.

Table 36 Chip Ordering Information

Product Number	Ordering Code	Temperature Range	Package (X x Y mm)	MAC Interface	Description
MxL86110C	MxL86110C-AQB-R	0 °C to 70 °C	QFN40 (5 x 5)	RGMII	Ethernet Gigabit PHY with RGMII
MxL86110I	MxL86110I-AQB-R	-40 °C to 85 °C	QFN40 (5 x 5)	RGMII	

Table 37 provides the chip specific information.

Table 37 Chip Specific Information

RGMII Interface	MxL86110
OUI	F04CD5
Device ID	0018_H
Revision	0000_H
Register 2 PHY ID1	$C133_H$
Register 3 PHY ID2	5580_H

Standards References

[1] IEEE 802.3-2018: "IEEE Standard for Ethernet", IEEE Computer Society

[2] Hewlett Packard, “Reduced Gigabit Media Independent Interface (RGMII)”, Version 1.3, 12.10.2000

[3] Hewlett Packard, “Reduced Gigabit Media Independent Interface (RGMII)”, Version 2.0, 04.01.2002

Terminology

A	
ADS	Auto-Downspeed
ANEG	Auto-Negotiation
B	
BER	Bit Error Rate
C	
CAT5	Category 5 Cabling
CDR	Clock and Data Recovery
CRS	Carrier Sense
D	
DEC	Digital Echo Canceler
E	
EEE	Energy-Efficient Ethernet
EMI	Electromagnetic Interference
G	
GbE	Gigabit Ethernet
GMII	Gigabit Media-Independent Interface
H	
HCD	Highest Common Denominator
I	
IEEE	Institute of Electrical and Electronics Engineers
L	
LAN	Local Area Network
LED	Light Emitting Diode
LPI	Low Power Idle
LSB	Least Significant Bit
M	
MAC	Media Access Controller
MDI	Media-Dependent Interface
MDIO	Management Data Input/Output
MDIX	Media-Dependent Interface Crossover
MII	Media-Independent Interface
MMD	MDIO Manageable Device
MSB	Most Significant Bit
N	
NC	Not Connected
O	
OSI	Open Systems Interconnection

OUI	Organizationally Unique Identifier
P	
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PHY	Physical Layer (device)
Q	
QFN	Quad Flat Non-leaded
R	
Rx	Receive
S	
SDF	Start Frame Delimiter
SFP	Small Form-Factor Pluggable
SGMII	Serial Gigabit Media-Independent Interface
SoC	System on Chip
SQE	Signal Quality Errors
STA	Station Management Entity (MAC SoC), defined in IEEE 802.3
SVR	Selecting Voltage Regulator
T	
TPI	Twisted Pair Interface
Tx	Transmit
V	
VSS	Voltage Source Supply
W	
Wi-Fi	Wireless Local Area Network
WoL	Wake-on-LAN
X	
XNP	Extended Next Page