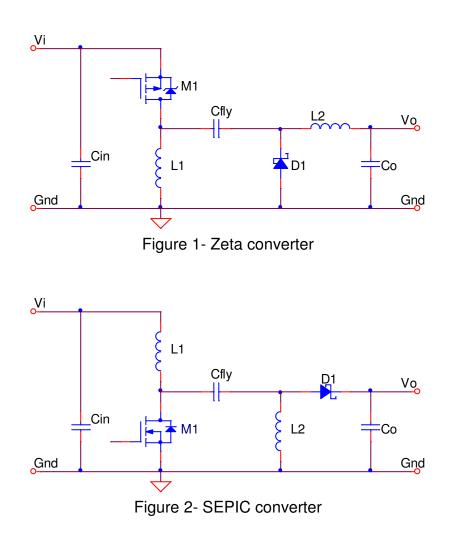
APPLICATION NOTE ANP29



Zeta Converter Basics based on Sipex's SP6125/6/7 controllers

Introduction

A Zeta converter performs a non-inverting buck-boost function similar to that of a SEPIC, which is an acronym for Single-Ended Primary Inductance Converter. The Zeta topology is also similar to the SEPIC, in that it uses two inductors, two switches and a capacitor to isolate the output from the input (see figures 1 and 2). However, Zeta conversion requires a P-Channel MOSFET as the primary switch, while SEPIC conversion uses an N-Channel MOSFET. This architecture makes Sipex's SP6125/6/7 controllers suitable for use in a Zeta topology.



Zeta Converter Waveforms

When analyzing Zeta waveforms it is helpful to keep in mind that at equilibrium, L1 average current equals IIN and L2 average current equals IOUT, since there is no DC current through the flying cap CFLY. Also there is no DC voltage across either inductor. Therefore, CFLY sees ground potential at its left side and VOUT at its right side, resulting in DC voltage across CFLY being equal to VOUT.

When M1 is on, L1 and L2 are energized. D1 sees a potential of $V_{IN+VOUT}$ across it (see figures 3, 4, and 5). When M1 is off, energy stored in L1 and L2 is released. D1 is forward biased.

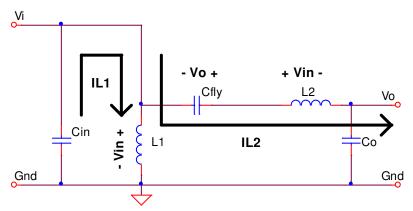


Figure 3- Zeta simplified circuit diagram during MOSFET ON time

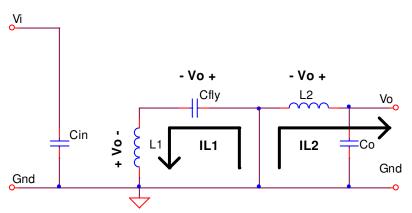


Figure 4- Zeta simplified circuit diagram during MOSFET OFF time

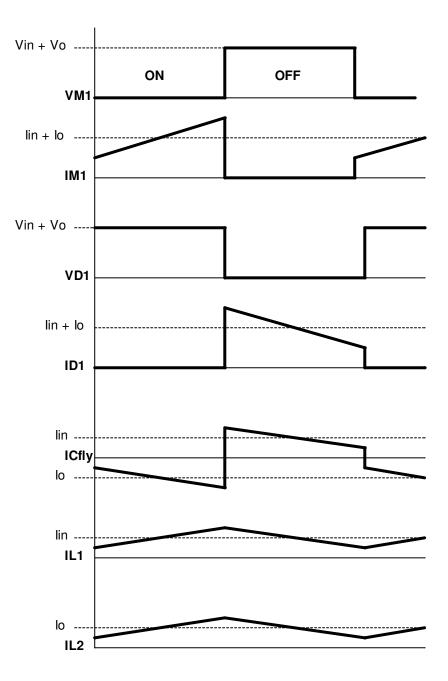


Figure 5- Zeta idealized waveforms

Voltage Conversion Ratio

Output voltage is given by the following equation:

$$Vo = Vin \times \frac{D}{1 - D}$$

Where D is duty cycle. VOUT is plotted as a function of D in figure 6. As can be seen, for D less than 0.5 the converter performs buck function and for D larger than 0.5 it is a boost topology.

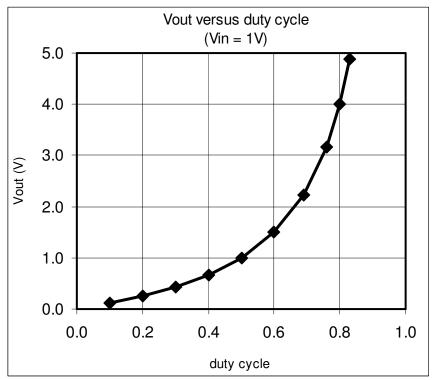


Figure 6- Output voltage versus duty cycle for VIN=1V

COMPONENT SELECTION

L1 Selection

Select L1 for inductance L, saturation current ISAT and DC rating IDC.

Calculate inductance from:

 $L1 = \frac{Vin, \max \times Vo}{Iripple \times f \times (Vin, \max + Vo)} \dots \dots \dots (1)$

Where:

IRIPPLE is the permissible peak-to-peak ripple current (nominally 50% of IOUT)

f is switching frequency VIN,max is maximum input voltage

Calculate DC rating of L1 from:

 $IDC = \frac{Io \times Vo}{Vin, \min \times Eff}$ (2)

Where: VIN,min is the minimum input voltage Eff is converter efficiency (nominally 85%)

Calculate saturation current from:

 $Isat \ge 1.15 \times IDC$ (3)

Where IDC is DC rating of L1 calculated above.

L2 Selection

Let L2 equal L1 thereby ensuring both inductors will have same ripple current. This is true since during ON time $L = Vin \times \left(\frac{Ton}{\Delta i}\right)$ for both inductors as seen in figure 3.

Selecting L2=L1 also makes it possible to wind both inductors on the same core if it is so desired. IDC should be at least equal to IOUT. Calculate saturation current as shown for L1.

CFLY Selection

Select CFLY for capacitance, voltage rating VDC and ripple current rating IRIPPLE.

Calculate CFLY from:

 $Cfly = \frac{Io \times Vo}{(Vin + Vo) \times f \times Vripple} \dots (4)$

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Where: VIN is minimum input voltage VRIPPLE is voltage ripple across CFLY (nominal 1% of VOUT)

DC Voltage rating should be greater than VOUT and ripple current should be greater than IOUT.

MOSFET Selection

Select MOSFET for voltage rating BVDSS, ON resistance RDS(ON), gate-to-drain charge QGD and thermal resistance RTH. BVDSS should be greater than VIN+VOUT, allowing a guard band against switching transients. The MOSFET should be able to handle the combined peak inductor current of both inductors. For an in-depth procedure see the section titled "MOSFET Selection" in any Sipex controller datasheet.

Diode Selection

Select diode for voltage rating VR and current rating I_F . VR should be greater than VIN+VOUT and I_F should be capable of conducting IIN+IOUT.

Cin Selection

Select the input capacitor CIN for Voltage rating, ripple current and Capacitance. A simplified expression for ripple current can be obtained by assuming D=0.5 and Efficiency =100%. Then IIN = IOUT and IRMS can be estimated from:

 $Icin = 0.5 \times Io$

In general, input voltage ripple should be kept below 1.5% of VIN (not to exceed 0.18V). By using the same assumptions that were applied for simplifying ripple current calculation, required input capacitance can be estimated from:

$$Cin = Io \times \frac{1}{2 \times f \times 0.18V} \dots (5)$$

Note that in the CIN equation the effect of ESR and ESL has been assumed to be negligible. This assumption is valid for ceramic capacitors and high quality Tantalum and Aluminum electrolytic capacitors.

COUT Selection

Select the output capacitor for capacitance, voltage rating and Equivalent Series Resistance (ESR). To simplify analysis, assume that a ceramic capacitor is used with ESR = 5mOhm. Then Vout ripple due to ESR is negligible. To calculate Cout, let inductor current ripple equal 30% of output current and use the following equation:

$$Co = \frac{Irip}{8 \times Vrip \times f}$$
(6)

Where:

IRIP is inductor ripple current (nominally 30% of IOUT) VRIP is output voltage permissible ripple (nominally 1% of VOUT)

Design Example

Design a Zeta converter to operate over input range of 10V-18V with output voltage of 12V and output current of 0.7A.

1- Controller selection

Use Sipex SP6126 operating at 600kHz and capable of driving a P-channel MOSFET.

2- Inductor L1

From equations (1) and (2), L1 and its corresponding DC current rating are calculated at 34uH and 1A respectively. From (3), saturation current should be larger than 1.15A. An inductor that meets the above specifications is Wurth Electronik dual inductor #744877100, 10uH, IDC=1.1A and ISAT=2.8A. Note that due to mutual inductance of the double inductor the effective inductance for calculating ripple current is 20uH. Even though this is less than the value calculated from (1), it is sufficient to ensure Continuous Conduction Mode of operation over the full input range.

3- Inductor L2

L2 is selected to be equal to L1 and thus a double inductor can be used.

4- Capacitor CFLY

Using (4) CFLY is calculated to be 3.9uF. In order to make the design more conservative a 22uF ceramic capacitor is selected.

5- MOSFET M1

One choice that meets this application's requirements is Vishay/Siliconix Si2319DS, BvDss=40V, $RDs(ON)=0.13\Omega$.

6- Diode D1

ON semiconductor MBRA340T3, 40V, 3A meets requirements.

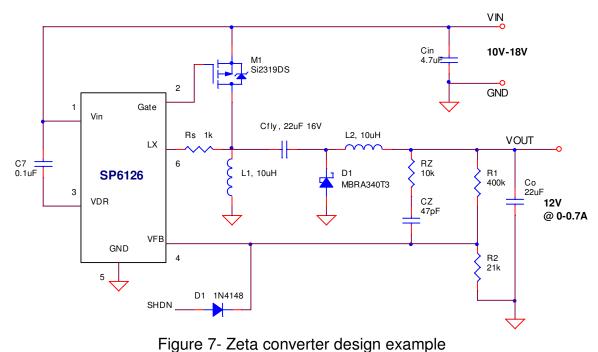
7- Capacitor CIN

Using (5) CIN is calculated to be 3.2uF. A 4.7uF ceramic capacitor meets this requirement.

8- Capacitor COUT

Using (6) COUT is calculated 0.36uF. However to allow for load transients a 22uF ceramic capacitor is selected.

The Zeta converter shown in figure 7 was thus built and tests showed satisfactory operation over voltage input range of 10V to 18V. Efficiency plots are shown in figure 8.



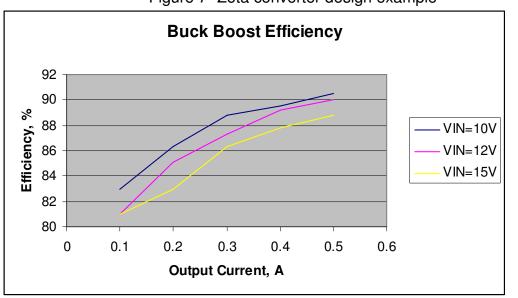


Figure 8- Zeta converter efficiency

Although Sipex's SP6125/6/7 are primarily used as buck controllers, by adding few inexpensive components they can be used as the heart of a Zeta non-inverting buck-boost converter that can provide output current up to 1A. The simple procedure outlined above can be followed to select the necessary components for a simple and inexpensive ZETA converter.

For further assistance:

Email: WWW Support page: Sipex Application Notes: <u>Sipexsupport@sipex.com</u> <u>http://www.sipex.com/content.aspx?p=support</u> <u>http://www.sipex.com/applicationNotes.aspx</u>



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