SIX CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH SONET DESYNCHRONIZER

DECEMBER 2004 *REV. 1.0.0*

GENERAL DESCRIPTION

The XRT75R06D is a six channel fully integrated Line Interface Unit (LIU) featuring EXAR's R^3 Technology (Reconfigurable, Relayless, Redundancy) for E3/DS3/STS-1 applications. The LIU incorporates 6 independent Receivers, Transmitters and Jitter Attenuators in a single 217 Lead BGA package.

Each channel of the XRT75R06D can be independently configured to operate in E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz). Each transmitter can be turned off and tri-stated for redundancy support or for conserving power.

The XRT75R06D's differential receiver provides high noise interference margin and is able to receive data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75R06D incorporates an advanced crystal-less jitter attenuator per channel that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications. Also, the jitter attenuators can be used for clock smoothing in SONET STS-1 to DS-3 de-mapping.

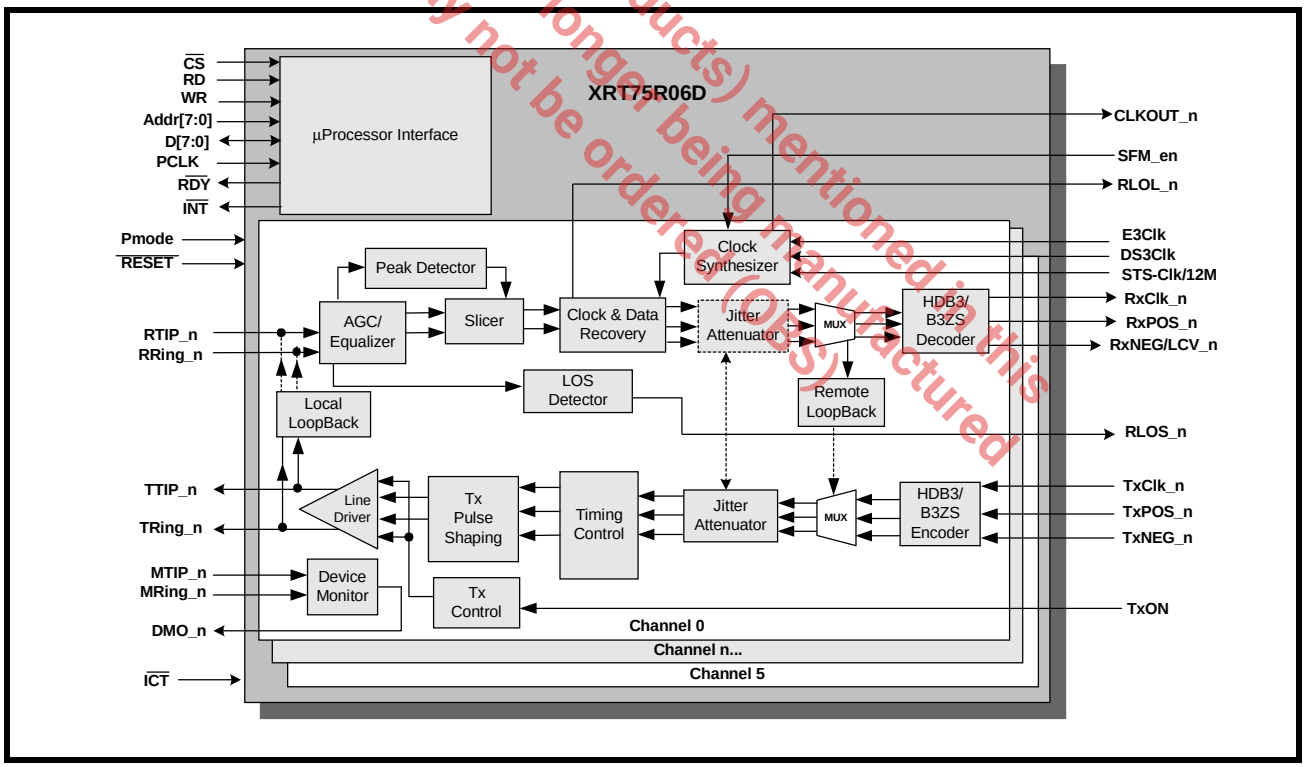
The XRT75R06D provides a Parallel Microprocessor Interface for programming and control.

The XRT75R06D supports analog, remote and digital loop-backs. The device also has a built-in Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error for diagnostic purposes.

APPLICATIONS

- E3/DS3 Access Equipment
- DSLAMs
- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals

FIGURE 1. BLOCK DIAGRAM OF THE XRT 75R06D



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75R06DIB	217 Lead BGA	-40°C to +85°C

FEATURES

RECEIVER

- R^3 Technology (Reconfigurable, Relayless, Redundancy)
- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3/STS-1 Jitter Tolerance Requirement
- Detects and Clears LOS as per G.775
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- Provides low jitter output clock

TRANSMITTER

- R^3 Technology (Reconfigurable, Relayless, Redundancy)
- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Each Transmitter can be independently turned on or off
- Transmitters provide Voltage Output Drive

JITTER ATTENUATOR

- On chip advanced crystal-less Jitter Attenuator for each channel
- Jitter Attenuator can be selected in Receive, Transmit path, or disabled
- Meets ETSI TBR 24 Jitter Transfer Requirements
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- 16 or 32 bits selectable FIFO size

CONTROL AND DIAGNOSTICS

- Parallel Microprocessor Interface for control and configuration
- Supports optional internal Transmit driver monitoring
- Each channel supports Analog, Remote and Digital Loop-backs
- Single 3.3 V ± 5% power supply
- 5 V Tolerant digital inputs
- Available in 217 pin BGA Package
- - 40°C to 85°C Industrial Temperature Range

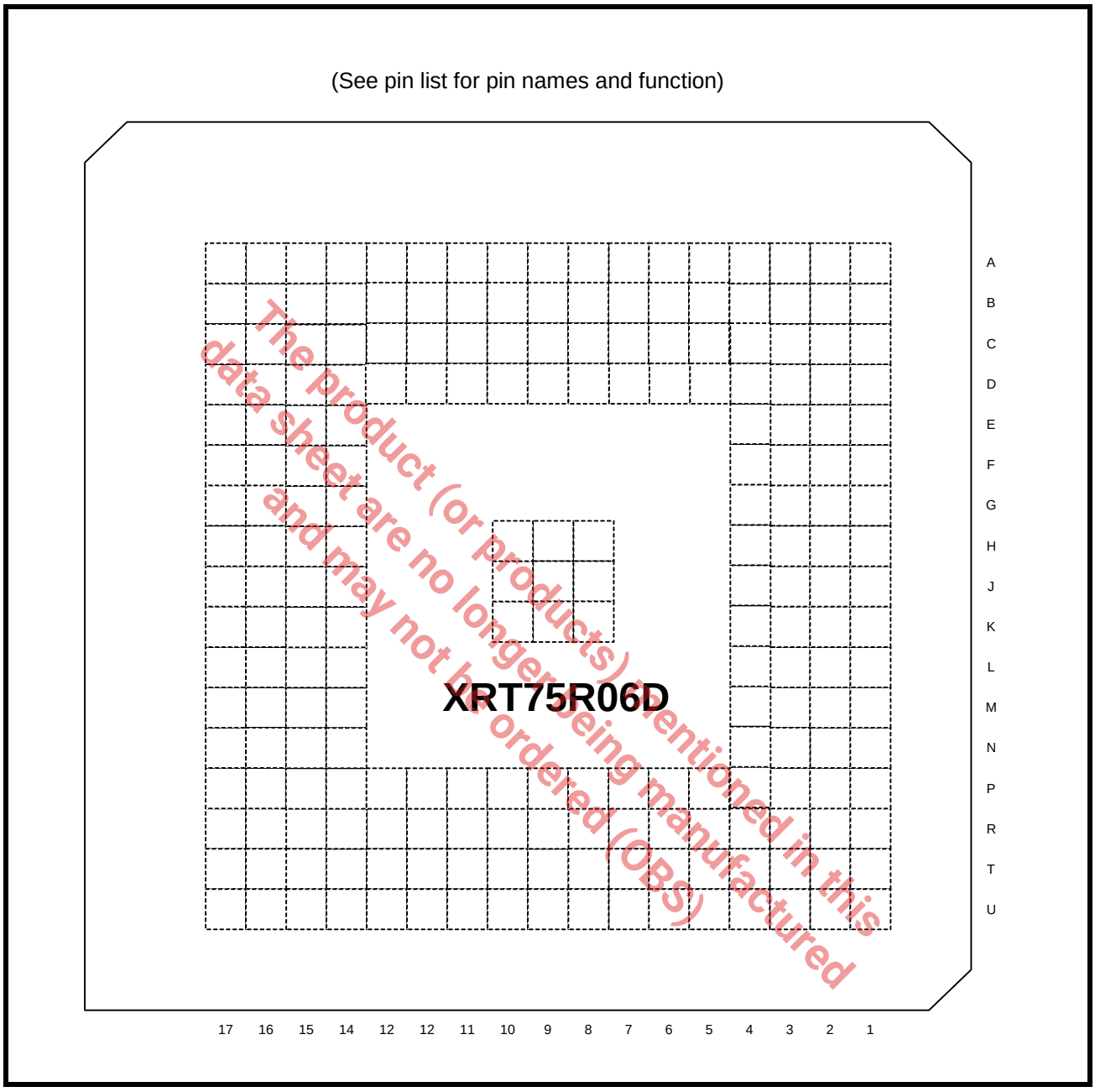
TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Accepts Transmit Clock with duty cycle of 30%-70%
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization (optional) for optimal Clock and Data Recovery
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications
- Declares Loss of Lock (LOL) Alarm
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment

FIGURE 2. XRT75R06D IN BGA PACKAGE (BOTTOM VIEW)



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PIN DESCRIPTIONS (BY FUNCTION)

TRANSMIT INTERFACE

<table>
<tr><th>LEAD #</th><th>SIGNAL NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>T15
R16
R15
N14
P14
P13</td><td>TxON_0
TxON_1
TxON_2
TxON_3
TxON_4
TxON_5</td><td>I</td><td>Transmitter ON Input - Channel 0:
Transmitter ON Input - Channel 1:
Transmitter ON Input - Channel 2:
Transmitter ON Input - Channel 3:
Transmitter ON Input - Channel 4:
Transmitter ON Input - Channel 5:
These pins are active only when the corresponding TxON bits are set.
Table below shows the status of the transmitter based on theTxON bit and TxON pin settings.
<table><tr><th>Bit</th><th>Pin</th><th>Transmitter Status</th></tr><tr><td>0</td><td>0</td><td>OFF</td></tr><tr><td>0</td><td>1</td><td>OFF</td></tr><tr><td>1</td><td>0</td><td>OFF</td></tr><tr><td>1</td><td>1</td><td>ON</td></tr></table>NOTES:
1. These pins will be active and can control the TTIP and TRING outputs only when the TxON_n bits in the channel register are set .
2. When Transmitters are turned off, the TTIP and TRING outputs are Tri-stated.
3. These pins are internally pulled up.</td></tr>
<tr><td>E3
M3
F15
P16
G3
H15</td><td>TxCLK_0
TxCLK_1
TxCLK_2
TxCLK_3
TxCLK_4
TxCLK_5</td><td>I</td><td>Transmit Clock Input for TPOS and TNEG - Channel 0:
Transmit Clock Input for TPOS and TNEG - Channel 1:
Transmit Clock Input for TPOS and TNEG - Channel 2:
Transmit Clock Input for TPOS and TNEG - Channel 3:
Transmit Clock Input for TPOS and TNEG - Channel 4:
Transmit Clock Input for TPOS and TNEG - Channel 5:
The frequency accuracy of this input clock must be of nominal bit rate ± 20 ppm. The duty cycle can be 30%-70%.
By default, input data is sampled on the falling edge of TxCLK.</td></tr>
</table>

TRANSMIT INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
F2 P2 G15 R17 H3 K15	TNEG_0 TNEG_1 TNEG_2 TNEG_3 TNEG_4 TNEG_5	I	**Transmit Negative Data Input - Channel 0:** **Transmit Negative Data Input - Channel 1:** **Transmit Negative Data Input - Channel 2:** **Transmit Negative Data Input - Channel 3:** **Transmit Negative Data Input - Channel 4:** **Transmit Negative Data Input - Channel 5:** In Dual-rail mode, these pins are sampled on the falling or rising edge of TxCLK_n . ***NOTES:*** 1. *These input pins are ignored and must be grounded if the Transmitter Section is configured to accept Single-Rail data from the Terminal Equipment.*
F3 N3 F16 P15 G2 J15	TPOS_0 TPOS_1 TPOS_2 TPOS_3 TPOS_4 TPOS_5	I	**Transmit Positive Data Input - Channel 0:** **Transmit Positive Data Input - Channel 1:** **Transmit Positive Data Input - Channel 2:** **Transmit Positive Data Input - Channel 3:** **Transmit Positive Data Input - Channel 4:** **Transmit Positive Data Input - Channel 5:** By default sampled on the falling edge of TxCLK.
D1 N1 D17 N17 H1 H17	TTIP_0 TTIP_1 TTIP_2 TTIP_3 TTIP_4 TTIP_5	O	**Transmit TTIP Output - Channel 0:** **Transmit TTIP Output - Channel 1:** **Transmit TTIP Output - Channel 2:** **Transmit TTIP Output - Channel 3:** **Transmit TTIP Output - Channel 4:** **Transmit TTIP Output - Channel 5:** These pins along with TRING transmit bipolar signals to the line using a 1:1 transformer.
E1 M1 E17 M17 J1 J17	TRING_0 TRING_1 TRING_2 TRING_3 TRING_4 TRING_5	O	**Transmit Ring Output - Channel 0:** **Transmit Ring Output - Channel 1:** **Transmit Ring Output - Channel 2:** **Transmit Ring Output - Channel 3:** **Transmit Ring Output - Channel 4:** **Transmit Ring Output - Channel 5:** These pins along with TTIP transmit bipolar signals to the line using a 1:1 transformer.

RECEIVE INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
A2 U2 A17 U17 D8 P8	RxCLK_0 RXCLK_1 RxCLK_2 RxCLK_3 RxCLK_4 RxCLK_5	O	**Receive Clock Output - Channel 0:** **Receive Clock Output - Channel 1:** **Receive Clock Output - Channel 2:** **Receive Clock Output - Channel 3:** **Receive Clock Output - Channel 4:** **Receive Clock Output - Channel 5:** By default, RPOS and RNEG data sampled on the rising edge RxCLK.. Set the RxCLKINV bit to sample RPOS/RNEG data on the falling edge of RxCLK
A1 U1 A16 U16 D9 P9	RPOS_0 RPOS_1 RPOS_2 RPOS_3 RPOS_4 RPOS_5	O	**Receive Positive Data Output - Channel 0:** **Receive Positive Data Output - Channel 1:** **Receive Positive Data Output - Channel 2:** **Receive Positive Data Output - Channel 3:** **Receive Positive Data Output - Channel 4:** **Receive Positive Data Output - Channel 5:** ***NOTE:*** *If the B3ZS/HDB3 Decoder is enabled in Single-rail mode, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") are removed and replaced with '0'.*
B2 T2 B16 T16 D10 P10	RNEG_0/ LCV_0 RNEG_1/ LCV_1 RNEG_2/ LCV_2 RNEG_3/ LCV_3 RNEG_4/ LCV_4 RNEG_5/ LCV_5	O	**Receive Negative Data Output/Line Code Violation Indicator - Channel 0:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 1:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 2:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 3:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 4:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 5:** In Dual Rail mode, a negative pulse is output through RNEG. **Line Code Violation Indicator - Channel n:** If configured in Single Rail mode then Line Code Violation will be output.

RECEIVE INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
A5 U5 A14 U14 A9 U9	RRING_0 RRING_1 RRING_2 RRING_3 RRING_4 RRING_5	I	**Receive Input - Channel 0:** **Receive Input - Channel 1:** **Receive Input - Channel 2:** **Receive Input - Channel 3:** **Receive Input - Channel 4:** **Receive Input - Channel 5:** These pins along with RTIP receive the bipolar line signal from the remote DS3/ E3/STS-1 Terminal.
A6 U6 A13 U13 A10 U10	RTIP_0 RTIP_1 RTIP_2 RTIP_3 RTIP_4 RTIP_5	I	**Receive Input - Channel 0:** **Receive Input - Channel 1:** **Receive Input - Channel 2:** **Receive Input - Channel 3:** **Receive Input - Channel 4:** **Receive Input - Channel 5:** These pins along with RRING receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.

CLOCK INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
E15	E3CLK	I	**E3 Clock Input (34.368 MHz ± 20 ppm):** If any of the channels is configured in E3 mode, a reference clock 34.368 MHz is applied on this pin. ***NOTE:*** *In single frequency mode, this reference clock is not required.*
G16	DS3CLK	I	**DS3 Clock Input (44.736 MHz ± 20 ppm):** If any of the channels is configured in DS3 mode, a reference clock 44.736 MHz. is applied on this pin. ***NOTE:*** *In single frequency mode, this reference clock is not required.*
C16	STS-1CLK/ 12M	I	**STS-1 Clock Input (51.84 MHz ± 20 ppm):** If any of the channels is configured in STS-1 mode, a reference clock 51.84 MHz is applied on this pin.. In Single Frequency Mode, a reference clock of 12.288 MHz ± 20 ppm is connected to this pin and the internal clock synthesizer generates the appropriate clock frequencies based on the configuration of the channels in E3, DS3 or STS-1 modes.
L15	SFM_EN	I	**Single Frequency Mode Enable:** Tie this pin "High" to enable the Single Frequency Mode. A reference clock of 12.288 MHz ± 20 ppm is applied. In the Single Frequency Mode (SFM) a low jitter output clock is provided for each channel if the CLK_EN bit is set thus eliminating the need for a separate clock source for the framer. Tie this pin "Low" if single frequency mode is not selected. In this case, the appropriate reference clocks must be provided. ***NOTE:*** *This pin is internally pulled down.*
B1 T1 B17 T17 D11 P11	CLKOUT_0 CLKOUT_1 CLKOUT_2 CLKOUT_3 CLKOUT_4 CLKOUT_5	O	**Clock output for channel 0** **Clock output for channel 1** **Clock output for channel 2** **Clock output for channel 3** **Clock output for channel 4** **Clock output for channel 5** Low jitter clock output for each channel based on the mode selection (E3,DS3 or STS-1) if the CLKOUTEN_n bit is set in the control register. This eliminates the need for a separate clock source for the framer. ***NOTES:*** *1. The maximum drive capability for the clockouts is 16 mA.* *2. This clock out is available both in SFM and non-SFM modes.*

CONTROL AND ALARM INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
B7 R6 C14 R14 C6 D14	MRING_0 MRING_1 MRING_2 MRING_3 MRING_4 MRING_5	I	**Monitor Ring Input - Channel 0:** **Monitor Ring Input - Channel 1:** **Monitor Ring Input - Channel 2:** **Monitor Ring Input - Channel 3:** **Monitor Ring Input - Channel 4:** **Monitor Ring Input - Channel 5:** The bipolar line output signal from TRING_n is connected to this pin via a 270 Ω resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled up.*
B8 R7 C13 R13 C7 D13	MTIP_0 MTIP_1 MTIP_2 MTIP_3 MTIP_4 MTIP_5	I	**Monitor Tip Input - Channel 0:** **Monitor Tip Input - Channel 1:** **Monitor Tip Input - Channel 2:** **Monitor Tip Input - Channel 3:** **Monitor Tip Input - Channel 4:** **Monitor Tip Input - Channel 5:** The bipolar line output signal from TTIP_n is connected to this pin via a 270-ohm resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled up.*
C5 T4 B12 T12 D5 B15	DMO_0 DMO_1 DMO_2 DMO_3 DMO_4 DMO_5	O	**Drive Monitor Output - Channel 0:** **Drive Monitor Output - Channel 1:** **Drive Monitor Output - Channel 2:** **Drive Monitor Output - Channel 3:** **Drive Monitor Output - Channel 4:** **Drive Monitor Output - Channel 5:** If MTIP_n and MRING_n has no transition pulse for 128 ± 32 TxCLK_n cycles, DMO_n goes “High” to indicate the driver failure. DMO_n output stays “High” until the next AMI signal is detected.
C8 T7 C12 T11 B11 R8	RLOS_0 RLOS_1 RLOS_2 RLOS_3 RLOS_4 RLOS_5	O	**Receive Loss of Signal - Channel 0:** **Receive Loss of Signal - Channel 1:** **Receive Loss of Signal - Channel 2:** **Receive Loss of Signal - Channel 3:** **Receive Loss of Signal - Channel 4:** **Receive Loss of Signal - Channel 5:** This output pin toggles "High" if the receiver has detected a Loss of Signal Condition.

CONTROL AND ALARM INTERFACE

C9 T8 D12 R11 C11 R9	RLOL_0 RLOL_1 RLOL_2 RLOL_3 RLOL_4 RLOL_5	O	**Receive Loss of Lock - Channel 0:** **Receive Loss of Lock - Channel 1:** **Receive Loss of Lock - Channel 2:** **Receive Loss of Lock - Channel 3:** **Receive Loss of Lock - Channel 4:** **Receive Loss of Lock - Channel 5:** This output pin toggles "High" if a Loss of Lock Condition is detected. LOL (Loss of Lock) condition occurs if the recovered clock frequency deviates from the Reference Clock frequency (available at either E3CLK or DS3CLK or STS-1CLK input pins) by more than 0.5%.
L16	RXA	****	**External Resistor of 3.01K Ω ± 1%.** Should be connected between RxA and RxB for internal bias.
K16	RXB	****	**External Resistor of 3.01K Ω ±1%.** Should be connected between RxA and RxB for internal bias.
P12	$\overline{ICT}$	I	**In-Circuit Test Input:** Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, tie this pin "High". ***NOTE:*** *This pin is internally pulled up.*
R12	TEST	****	**Factory Test Pin** ***NOTE:*** *This pin must be connected to GND for normal operation.*

MICROPROCESSOR INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
K3	$\overline{CS}$	I	**Chip Select** Tie this “Low” to enable the communication with the Microprocessor Interface.
R1	PCLK	I	**Processor Clock Input** To operate the Microprocessor Interface, appropriate clock frequency is provided through this pin. Maximum frequency is 66 Mhz.
K2	$\overline{WR}$	I	**Write Data :** To write data into the registers, this active low signal is asserted.
L2	$\overline{RD}$	I	**Read Data:** To read data from the registers, this active low pin is asserted.
J3	$\overline{RESET}$	I	**Register Reset:** Setting this input pin "Low" resets the contents of the Command Registers to their default settings and default operating configuration ***NOTE:*** *This pin is internally pulled up.*
L3	PMODE	I	**Processor Mode Select:** When this pin is tied “High”, the microprocessor is operating in synchronous mode which means that clock must be applied to the PCLK (pin 55). Tie this pin “Low” to select the Asynchronous mode. An internal clock is provided for the microprocessor interface.

MICROPROCESSOR INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
T3	$\overline{RDY}$	O	**Ready Acknowledge:** ***NOTE:*** *This pin must be connected to VDD via 3 kΩ ± 1% resistor.*
U3	$\overline{INT}$	O	**INTERRUPT Output:** A transition to "Low" indicates that an interrupt has been generated. The interrupt function can be disabled by clearing the interrupt enable bit in the Channel Control Register. ***NOTES:*** 1. *This pin will remain asserted "Low" until the interrupt is serviced.* 2. *This pin must be conneced to VDD via 3 kΩ ± 1% resistor.*
B4 A3 B3 C4 C3 C2 D3 D4	ADDR[0] ADDR[1] ADDR[2] ADDR[3] ADDR[4] ADDR[5] ADDR[6] ADDR[7]	I	**ADDRESS BUS:** 8 bit address bus for the microprocessor interface
N4 P3 P4 P5 R5 R4 R3 R2	D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	**DATA BUS:** 8 bit Data Bus for the microprocessor interface

ANALOG POWER AND GROUND

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
E2	TxAVDD_0	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 0**
N2	TxAVDD_1	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 1**
E16	TxAVDD_2	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 2**
N16	TxAVDD_3	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 3**
J2	TxAVDD_4	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 4**
J16	TxAVDD_5	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 5**
D2	TxAGND_0	****	**Transmitter Analog GND - Channel 0**
M2	TxAGND_1	****	**Transmitter Analog GND - Channel 1**
D16	TxAGND_2	****	**Transmitter Analog GND - Channel 2**
M16	TxAGND_3	****	**Transmitter Analog GND - Channel 3**
H2	TxAGND_4	****	**Transmitter Analog GND - Channel 4**
H16	TxAGND_5	****	**Transmitter Analog GND - Channel 5**
A4	RxAVDD_0	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 0**
U4	RxAVDD_1	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 1**
A15	RxAVDD_2	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 2**
U15	RxAVDD_3	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 3**
A8	RxAVDD_4	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 4**
U8	RxAVDD_5	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 5**
A7	RxAGND_0	****	**Receiver Analog GND - Channel 0**
U7	RxAGND_1	****	**Receive Analog GND - Channel 1**
A12	RxAGND_2	****	**Receive Analog GND - Channel 2**
U12	RxAGND_3	****	**Receive Analog GND - Channel 3**
A11	RxAGND_4	****	**Receive Analog GND - Channel 4**
U11	RxAGND_5	****	**Receive Analog GND - Channel 5**
E4	JaAVDD_0	****	**Analog 3.3 V ± 5% VDD - Jitter Attenuator Channel 0**
K4	JaAVDD_1	****	**Analog 3.3 V ± 5% VDD - Jitter Attenuator Channel 1**
E14	JaAVDD_2	****	**Analog 3.3 V ± 5% VDD - Jitter Attenuator Channel 2**
K14	JaAVDD_3	****	**Analog 3.3 V ± 5% VDD - Jitter Attenuator Channel 3**
G4	JaAVDD_4	****	**Analog 3.3 V ± 5% VDD - Jitter Attenuator Channel 4**
G14	JaAVDD_5	****	**Analog 3.3 V ± 5% VDD - Jitter attenuator Channel 5**
F4	JaAGND_0	****	**Analog GND - Jitter Attenuator Channel 0**

ANALOG POWER AND GROUND

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
J4	JaAGND_1	****	**Analog GND - Jitter Attenuator Channel 1**
F14	JaAGND_2	****	**Analog GND - Jitter Attenuator Channel 2**
J14	JaAGND_3	****	**Analog GND - Jitter Attenuator Channel 3**
H4	JaAGND_4	****	**Analog GND - Jitter Attenuator Channel 4**
H14	JaAGND_5	****	**Analog GND - Jitter Attenuator Channel 5**
C10	AGND	****	**Analog GND**
R10	AGND	****	**Analog GND**
H9	AGND	****	**Analog GND**
J9	AGND	****	**Analog GND**
K9	AGND	****	**Analog GND**
N15	REFAVDD	****	**Analog 3.3 V ± 5% VDD - Reference**
M15	REFGND	****	**Reference GND**

DIGITAL POWER AND GROUND

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
F1	TxVDD_0	****	**Transmitter 3.3 V ± 5% VDD Channel 0**
L1	TxVDD_1	****	**Transmitter 3.3 V ± 5% VDD Channel 1**
F17	TxVDD_2	****	**Transmitter 3.3 V ± 5% VDD Channel 2**
L17	TxVDD_3	****	**Transmitter 3.3 V ± 5% VDD Channel 3**
K1	TxVDD_4	****	**Transmitter 3.3 V ± 5% VDD Channel 4**
K17	TxVDD_5	****	**Transmitter 3.3 V ± 5% VDD Channel 5**
C1	TxGND_0	****	**Transmitter GND - Channel 0**
P1	TxGND_1	****	**Transmitter GND - Channel 1**
C17	TxGND_2	****	**Transmitter GND - Channel 2**
P17	TxGND_3	****	**Transmitter GND - Channel 3**
G1	TxGND_4	****	**Transmitter GND - Channel 4**
G17	TxGND_5	****	**Transmitter GND - Channel 5**
B5	RxDVDD_0	****	**Receiver 3.3 V ± 5% VDD - Channel 0**
T5	RxDVDD_1	****	**Receiver 3.3 V ± 5% VDD - Channel 1**
B14	RxDVDD_2	****	**Receiver 3.3 V ± 5% VDD - Channel 2**
T14	RxDVDD_3	****	**Receiver 3.3 V ± 5% VDD - Channel 3**
B9	RxDVDD_4	****	**Receiver 3.3 V ± 5% VDD - Channel 4**
T9	RxDVDD_5	****	**Receiver 3.3 V ± 5% VDD - Channel 5**
B6	RxDGND_0	****	**Receiver Digital GND - Channel 0**
T6	RxDGND_1	****	**Receiver Digital GND - Channel 1**
B13	RxDGND_2	****	**Receiver Digital GND - Channel 2**
T13	RxDGND_3	****	**Receiver Digital GND - Channel 3**
B10	RxDGND_4	****	**Receiver Digital GND - Channel 4**
T10	RxDGND_5	****	**Receiver Digital GND - Channel 5**
P6	DVDD_1	****	**VDD 3.3 V ± 5%**
C15	DVDD_2	****	**VDD 3.3 V ± 5%**
L4	JaDVDD_1	****	**VDD 3.3 V ± 5%**
D6	DVDD(uP)	****	**VDD 3.3 V ± 5%**
L14	JaDVDD_2	****	**VDD 3.3 V ± 5%**
D15	DGND_1	****	**Digital GND**
D7	DGND(uP)	****	**Digital GND**

DIGITAL POWER AND GROUND

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
M14	JaDGND_2	****	**Digital GND**
M4	JaDGND_1	****	**Digital GND**
P7	DGND	****	**Digital GND**
H8	DGND	****	**Digital GND**
J8	DGND	****	**Digital GND**
K8	DGND	****	**Digital GND**
H10	DGND	****	**Digital GND**
J10	DGND	****	**Digital GND**
K10	DGND	****	**Digital GND**

FUNCTIONAL DESCRIPTION

The XRT75R06D is a six channel fully integrated Line Interface Unit featuring EXAR's R^3 Technology (Reconfigurable, Relayless Redundancy) for E3/DS3/STS-1 applications. The LIU incorporates 6 independent Receivers, Transmitters and Jitter Attenuators in a single 217 Lead BGA package. Each channel can be independently programmed to support E3, DS-3 or STS-1 line rates using one input clock reference of 12.288MHz in Single Frequency Mode (SFM). The LIU is responsible for providing the physical connection between a line interface and an aggregate mapper or framing device. Along with the analog-to-digital processing, the LIU offers monitoring and diagnostic features to help optimize network design implementation. A key characteristic within the network topology is Automatic Protection Switching (APS).

EXAR's proven expertise in providing redundany solutions has paved the way for R^3 Technology.

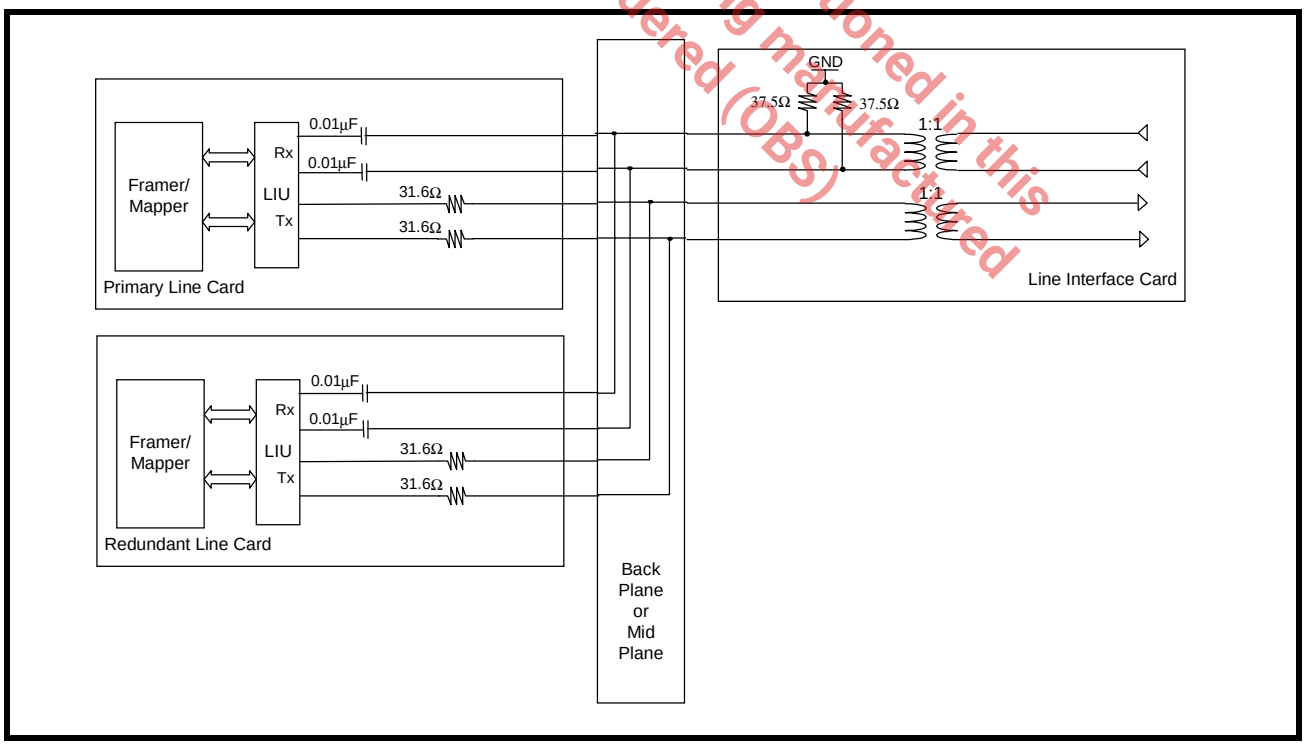
1.0 R^3 TECHNOLOGY (RECONFIGURABLE, RELAYLESS REDUNDANCY)

Redundancy is used to introduce reliability and protection into network card design. The redundant card in many cases is an exact replicate of the primary card, such that when a failure occurs the network processor can automatically switch to the backup card. EXAR's R^3 technology has re-defined E3/DS-3/STS-1 LIU design for 1:1 and 1+1 redundancy applications. Without relays and one Bill of Materials, EXAR offers multi-port, integrated LIU solutions to assist high density aggregate applications and framing requirements with reliability. The following section can be used as a reference for implementing R^3 Technology with EXAR's world leading line interface units.

1.1 Network Architecture

A common network design that supports 1:1 or 1+1 redundancy consists of N primary cards along with N backup cards that connect into a mid-plane or back-plane architecture without transformers installed on the network cards. In addition to the network cards, the design has a line interface card with one source of transformers, connectors, and protection components that are common to both network cards. With this design, the bill of materials is reduced to the fewest amount of components. See Figure 3. for a simplified block diagram of a typical redundancy design.

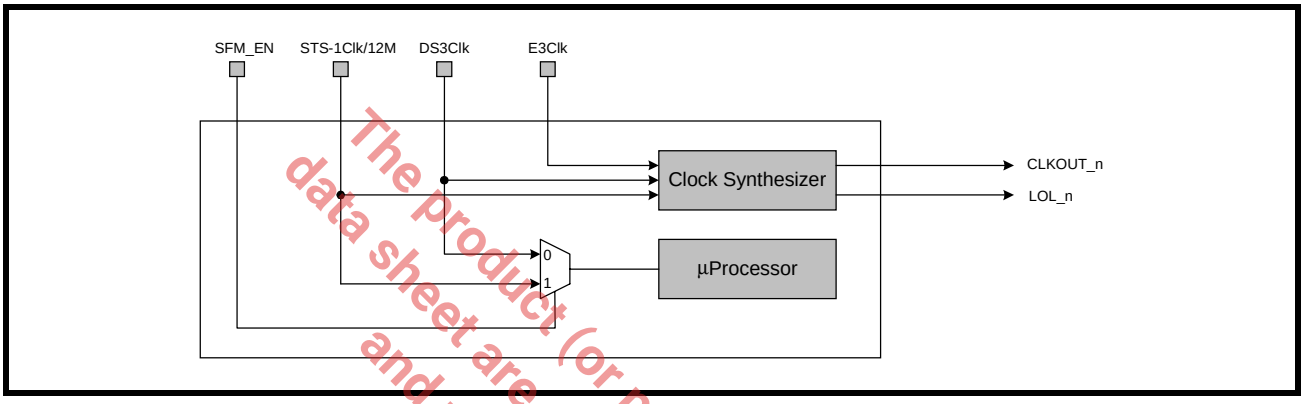
FIGURE 3. NETWORK REDUNDANCY ARCHITECTURE



2.0 CLOCK SYNTHESIZER

The LIU uses a flexible user interface for accepting clock references to generate the internal master clocks used to drive the LIU. The reference clock used to supply the microprocessor timing is generated from the DS-3 or SFM clock input. Therefore, if the chip is configured for STS-1 only or E3 only, then the DS-3 input pin must be connected to the STS-1 pin or E3 pin respectively. In DS-3 mode or when SFM is used, the STS-1 and E3 input pins can be left unconnected. If SFM is enabled by pulling the SFM_EN pin "High", 12.288MHz is the only clock reference necessary to generate DS-3, E3, or STS-1 line rates and the microprocessor timing. A simplified block diagram of the clock synthesizer is shown in Figure 4

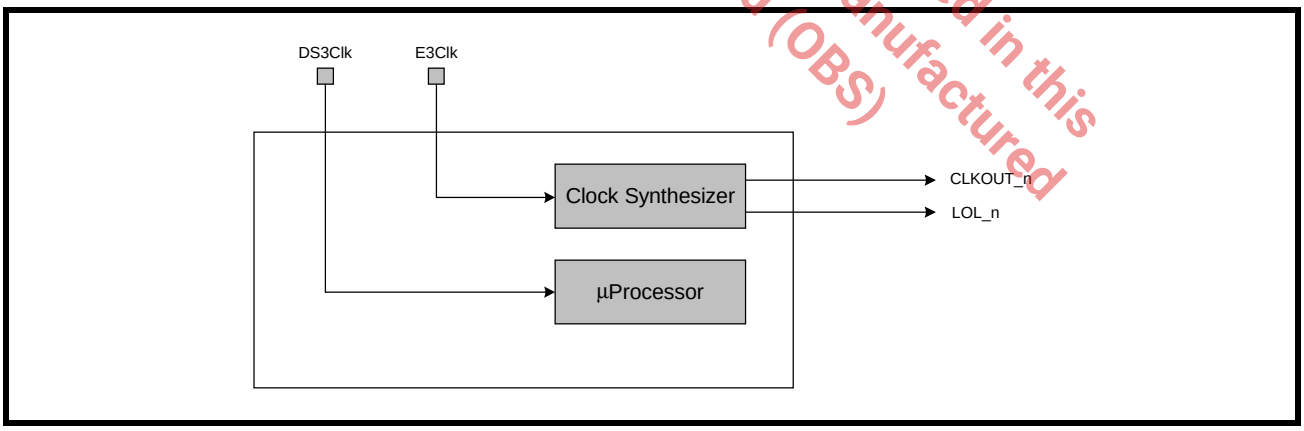
FIGURE 4. SIMPLIFIED BLOCK DIAGRAM OF THE INPUT CLOCK CIRCUITRY DRIVING THE MICROPROCESSOR



2.1 Clock Distribution

Network cards that are designed to support multiple line rates which are not configured for single frequency mode should ensure that a clock is applied to the DS3Clk input pin. For example: If the network card being supplied to an ISP requires E3 only, the DS-3 input clock reference is still necessary to provide read and write access to the internal microprocessor. Therefore, the E3 mode requires two input clock references. If however, multiple line rates will not be supported, i.e. E3 only, then the DS3Clk input pin may be hard wire connected to the E3Clk input pin.

FIGURE 5. CLOCK DISTRIBUTION CONGIFURED IN E3 MODE WITHOUT USING SFM

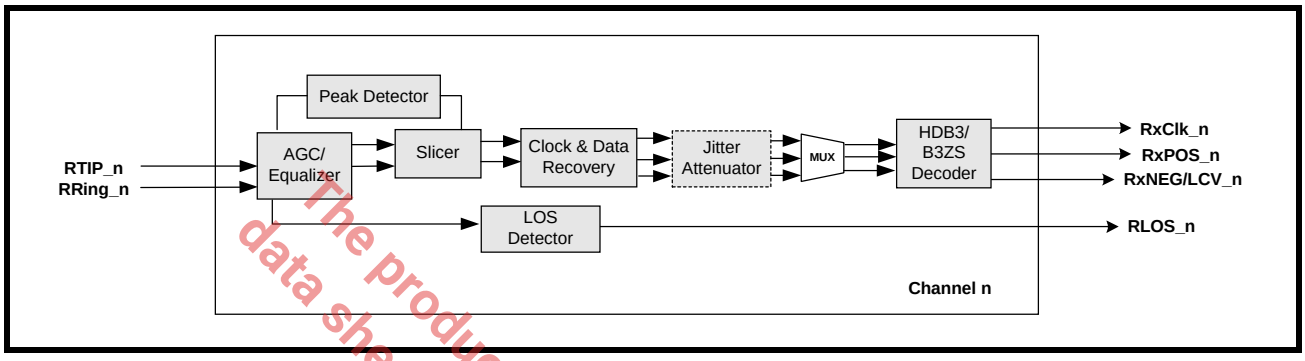


NOTE: *For one input clock reference, the single frequency mode should be used.*

3.0 THE RECEIVER SECTION

The receiver is designed so that the LIU can recover clock and data from an attenuated line signal caused by cable loss or flat loss according to industry specifications. Once data is recovered, it is processed and presented at the receiver outputs according to the format chosen to interface with a Framer/Mapper or ASIC. This section describes the detailed operation of various blocks within the receive path. A simplified block diagram of the receive path is shown in Figure 6.

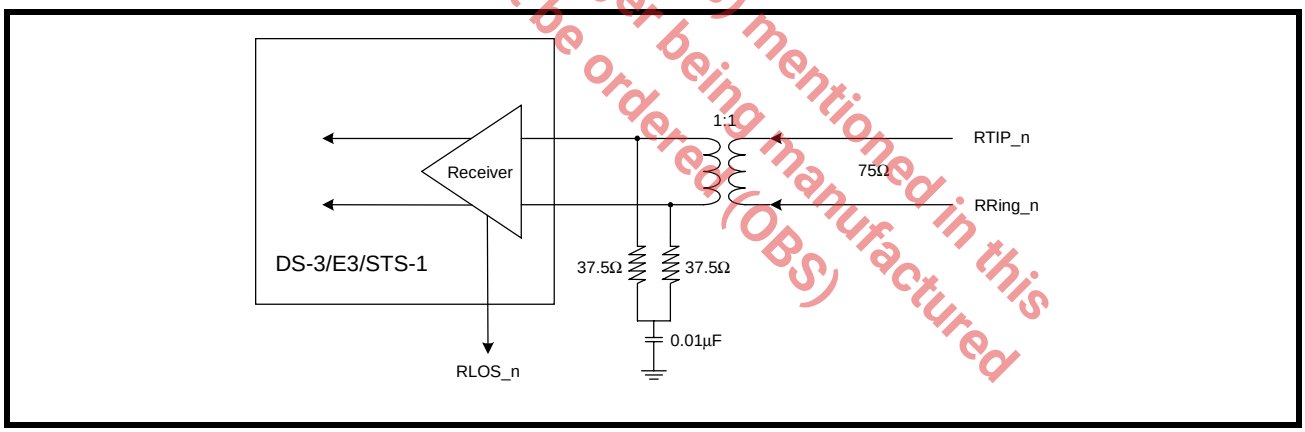
FIGURE 6. RECEIVE PATH BLOCK DIAGRAM



3.1 Receive Line Interface

Physical Layer devices are AC coupled to a line interface through a 1:1 transformer. The transformer provides isolation and a level shift by blocking the DC offset of the incoming data stream. The typical medium for the line interface is a 75Ω coxial cable. Whether using E3, DS-3 or STS-1, the LIU requires the same bill of materials, see Figure 7.

FIGURE 7. RECEIVE LINE INTERFACECONNECTION



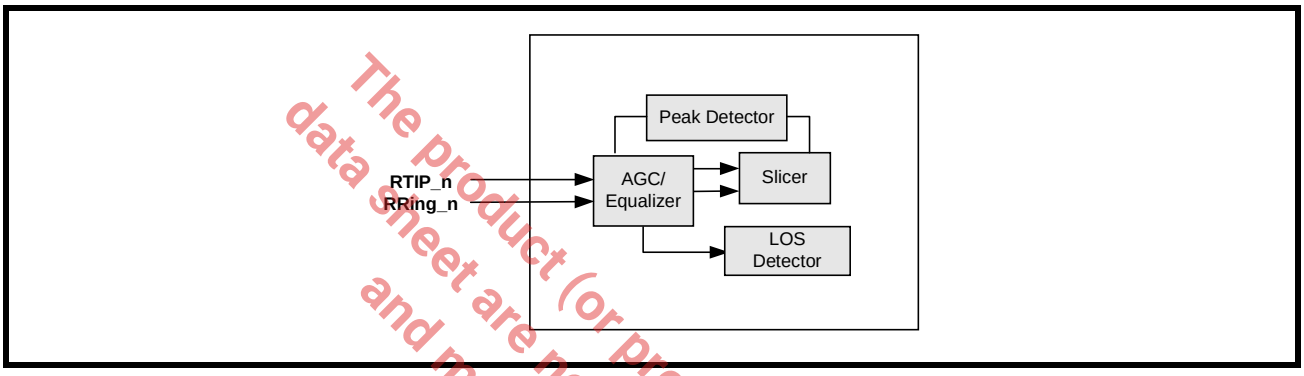
3.2 Adaptive Gain Control (AGC)

The Adaptive Gain Control circuit amplifies the incoming analog signal and compensates for the various flat losses and also for the loss at one-half symbol rate. The AGC has a dynamic range of 30 dB. The peak detector provides feedback to the equalizer before slicing occurs.

3.3 Receive Equalizer

The Equalizer restores the integrity of the signal and compensates for the frequency dependent attenuation of up to 900 feet of coaxial cable (1300 feet for E3). The Equalizer also boosts the high frequency content of the signal to reduce Inter-Symbol Interference (ISI) so that the slicer slices the signal at 50% of peak voltage to generate Positive and Negative data. The equalizer can be disabled by programming the appropriate register.

FIGURE 8. ACG/EQUALIZER BLOCK DIAGRAM



3.3.1 Recommendations for Equalizer Settings

The Equalizer has two gain settings to provide optimum equalization. In the case of normally shaped DS3/STS-1 pulses (pulses that meet the template requirements) that has been driven through 0 to 900 feet of cable, the Equalizer can be enabled. However, for square-shaped pulses such as E3 or for DS3/STS-1 high pulses (that does not meet the pulse template requirements), it is recommended that the Equalizer be disabled for cable length less than 300 feet. This would help to prevent over-equalization of the signal and thus optimize the performance in terms of better jitter transfer characteristics. The Equalizer also contains an additional 20 dB gain stage to provide the line monitoring capability of the resistively attenuated signals which may have 20dB flat loss. The equalizer gain mode can be enabled by programming the appropriate register.

NOTE: *The results of extensive testing indicate that even when the Equalizer was enabled, regardless of the cable length, the integrity of the E3 signal was restored properly over 0 to 12 dB cable loss at Industrial Temperature.*

3.4 Clock and Data Recovery

The Clock and Data Recovery Circuit extracts the embedded clock, RxClk_n from the sliced digital data stream and provides the retimed data to the B3ZS (HDB3) decoder. The Clock Recovery PLL can be in one of the following two modes:

3.4.1 Data/Clock Recovery Mode

In the presence of input line signals on the RTIP_n and RRing_n input pins and when the frequency difference between the recovered clock signal and the reference clock signal is less than 0.5%, the clock that is output on the RxClk_n out pins is the Recovered Clock signal.

3.4.2 Training Mode

In the absence of input signals at RTIP_n and RRing_n pins, or when the frequency difference between the recovered line clock signal and the reference clock applied on the ExClk_n input pins exceed 0.5%, a Loss of Lock condition is declared by toggling RLOL_n output pin “High” or setting the RLOL_n bit to “1” in the control register. Also, the clock output on the RxClk_n pins are the same as the reference channel clock.

3.5 LOS (Loss of Signal) Detector

3.5.1 DS3/STS-1 LOS Condition

A Digital Loss of SIgnal (DLOS) condition occurs when a string of 175 ± 75 consecutive zeros occur on the line. When the DLOS condition occurs, the DLOS_n bit is set to "1" in the status control register. DLOS condition is cleared when the detected average pulse density is greater than 33% for 175 ± 75 pulses. Analog Loss of Signal (ALOS) condition occurs when the amplitude of the incoming line signal is below the threshold as shown in the Table 1.The status of the ALOS condition is reflected in the ALOS_n status control register. RLOS is the logical OR of the DLOS and ALOS states. When the RLOS condition occurs the RLOS_n output pin is toggled "High" and the RLOS_n bit is set to "1" in the status control register.

TABLE 1: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF LOSTHR AND REQEN (DS3 AND STS-1 APPLICATIONS)

APPLICATION	REQEN SETTING	LOSTHR SETTING	SIGNAL LEVEL TO DECLARE ALOS DEFECT	SIGNAL LEVEL TO CLEAR ALOS DEFECT
DS3	0	0	< 75mVpk	> 130mVpk
	1	0	< 45mVpk	> 60mVpk
	0	1	< 120mVpk	> 45mVpk
	1	1	< 55mVpk	> 180mVpk
STS-1	0	0	< 120mVpk	> 170mVpk
	1	0	< 50mVpk	> 75mVpk
	0	1	< 125mVpk	> 205mVpk
	1	1	< 55mVpk	> 90mVpk

3.5.2 Disabling ALOS/DLOS Detection

For debugging purposes it is useful to disable the ALOS and/or DLOS detection. Writing a "1" to both ALOSDIS_n and DLOSDIS_n bits disables the LOS detection on a per channel basis.

3.5.3 E3 LOS Condition:

If the level of incoming line signal drops below the threshold as described in the ITU-T G.775 standard, the LOS condition is detected. Loss of signal is defined as no transitions for 10 to 255 consecutive zeros. No transitions is defined as a signal level between 15 and 35 dB below the normal. This is illustrated in Figure 9. The LOS condition is cleared within 10 to 255 UI after restoration of the incoming line signal. Figure 10 shows the LOS declaration and clearance conditions.

FIGURE 9. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775

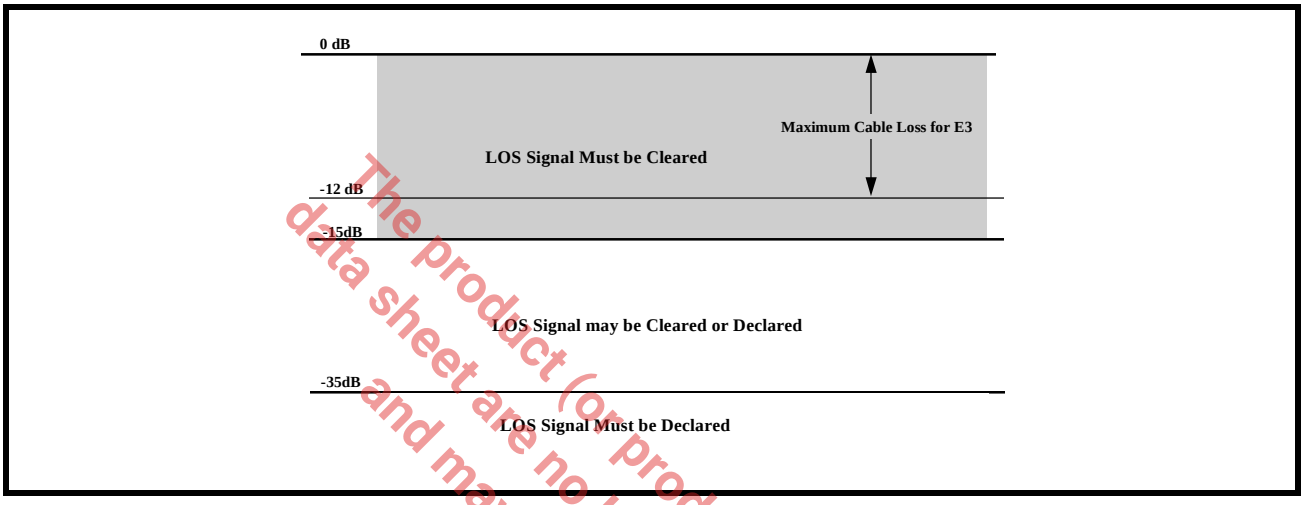
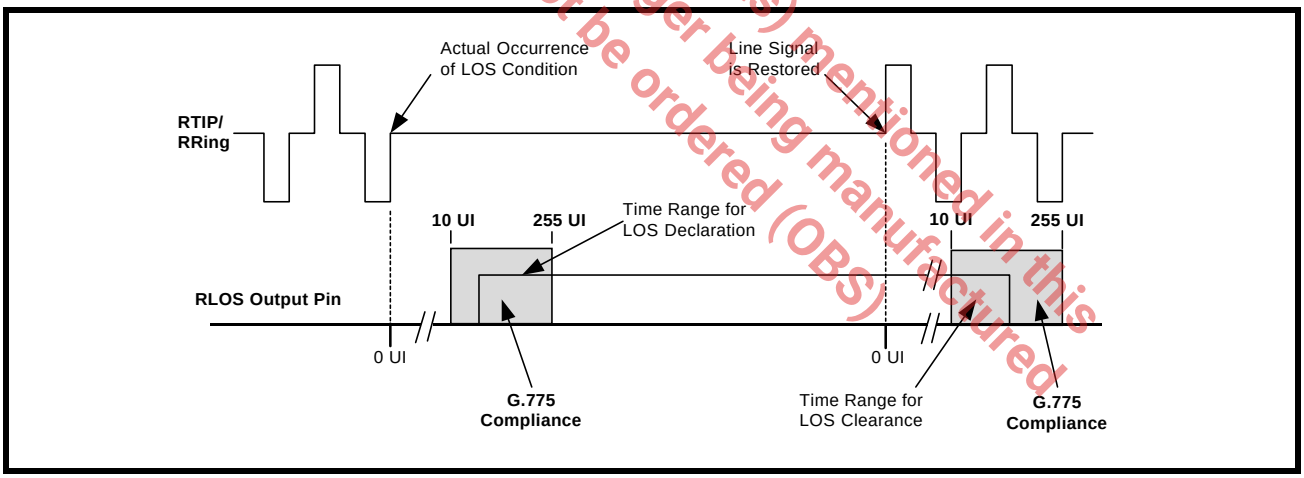


FIGURE 10. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775.



3.5.4 Interference Tolerance

For E3 mode, ITU-T G.703 Recommendation specifies that the receiver be able to recover error free clock and data in the presence of a sinusoidal interfering tone signal. For DS3 and STS-1 modes, the same recommendation is being used. Figure 11 shows the configuration to test the interference margin for DS3/ STS1. Figure 12 shows the set up for E3.

FIGURE 11. INTERFERENCE MARGIN TEST SET UP FOR DS3/STS-1

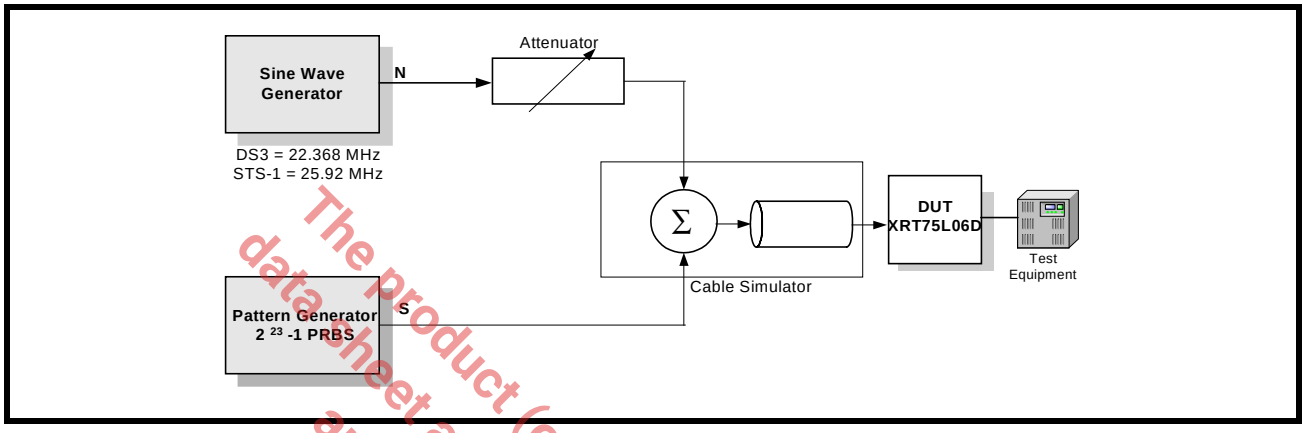


FIGURE 12. INTERFERENCE MARGIN TEST SET UP FOR E3.

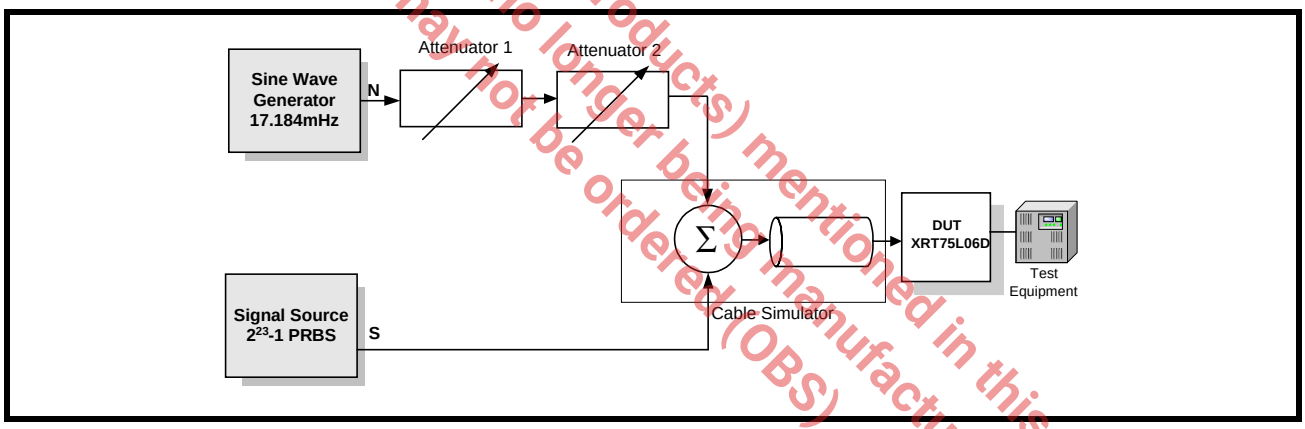


TABLE 2: INTERFERENCE MARGIN TEST RESULTS

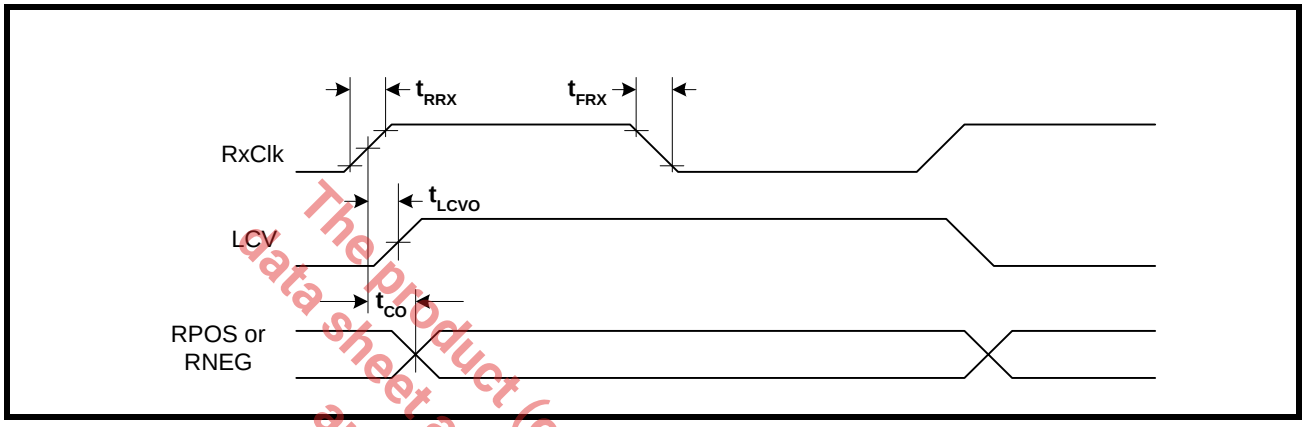
MODE	CABLE LENGTH (ATTENUATION)	INTERFERENCE TOLERANCE
E3	0 dB	Equalizer "IN"
		-17 dB
	12 dB	-14 dB
DS3	0 feet	-15 dB
	225 feet	-15 dB
	450 feet	-14 dB
STS-1	0 feet	-15 dB
	225 feet	-14 dB
	450 feet	-14 dB

3.5.5 Muting the Recovered Data with LOS condition:

When the LOS condition is declared, the clock recovery circuit locks into the reference clock applied to the internal master clock outputs this clock onto the RxClk_n output pin. The data on the RxPOS_n and RxNEG_n pins can be forced to zero by setting the LOSMUT_n bits in the individual channel control register to "1".

NOTE: *When the LOS condition is cleared, the recovered data is output on RxPOS_n and RxNEG_n pins.*

FIGURE 13. RECEIVER DATA OUTPUT AND CODE VIOLATION TIMING



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
RxClk	Duty Cycle	45	50	55	%
	RxClk Frequency E3 DS-3 STS-1		 34.368 44.736 51.84		 MHz MHz MHz
t_{RRX}	RxClk rise time (10% o 90%)		2	4	ns
t_{FRX}	RxClk falling time (10% to 90%)		2	4	ns
t_{CO}	RxClk to RPOS/RNEG delay time			4	ns
t_{LCVO}	RxClk to rising edge of LCV output delay		2.5		ns

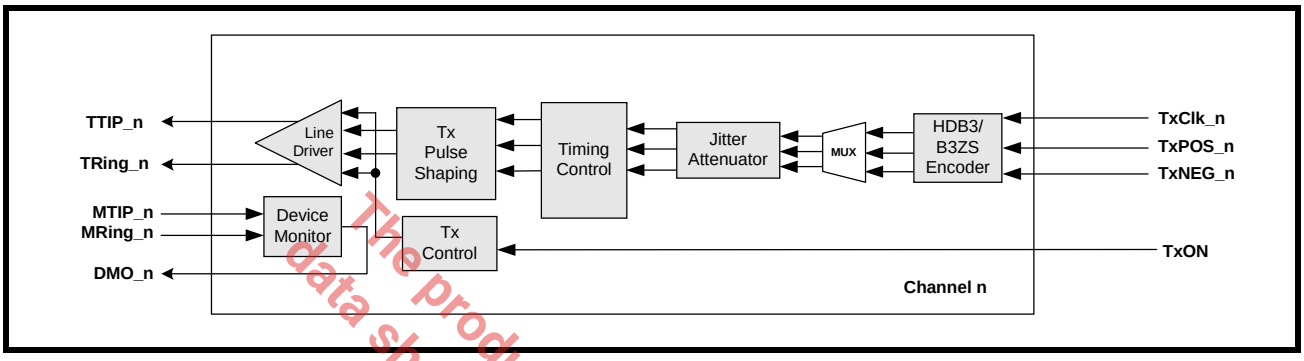
3.6 B3ZS/HDB3 Decoder

The decoder block takes the output from the clock and data recovery block and decodes the B3ZS (for DS3 or STS-1) or HDB3 (for E3) encoded line signal and detects any coding errors or excessive zeros in the data stream. Whenever the input signal violates the B3ZS or HDB3 coding sequence for bipolar violation or contains three (for B3ZS) or four (for HDB3) or more consecutive zeros, an active "High" pulse is generated on the RLCV_n output pins to indicate line code violation.

4.0 THE TRANSMITTER SECTION

The transmitter is designed so that the LIU can accept serial data from a local device, encode the data properly, and then output an analog pulse according to the pulse shape chosen in the appropriate registers. This section describes the detailed operation of various blocks within the transmit path. A simplified block diagram of the transmit path is shown in Figure 14.

FIGURE 14. TRANSMIT PATH BLOCK DIAGRAM



4.1 Transmit Digital Input Interface

The method for applying data to the transmit inputs of the LIU is a serial interface consisting of TxClk, TxPOS, and TxNEG. For single rail mode, only TxClk and TxPOS are necessary for providing the local data from a Framer device or ASIC. Data can be sampled on either edge of the input clock signal by programming the appropriate register. A typical interface is shown in Figure 15.

FIGURE 15. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT75R06D (DUAL-RAIL DATA)

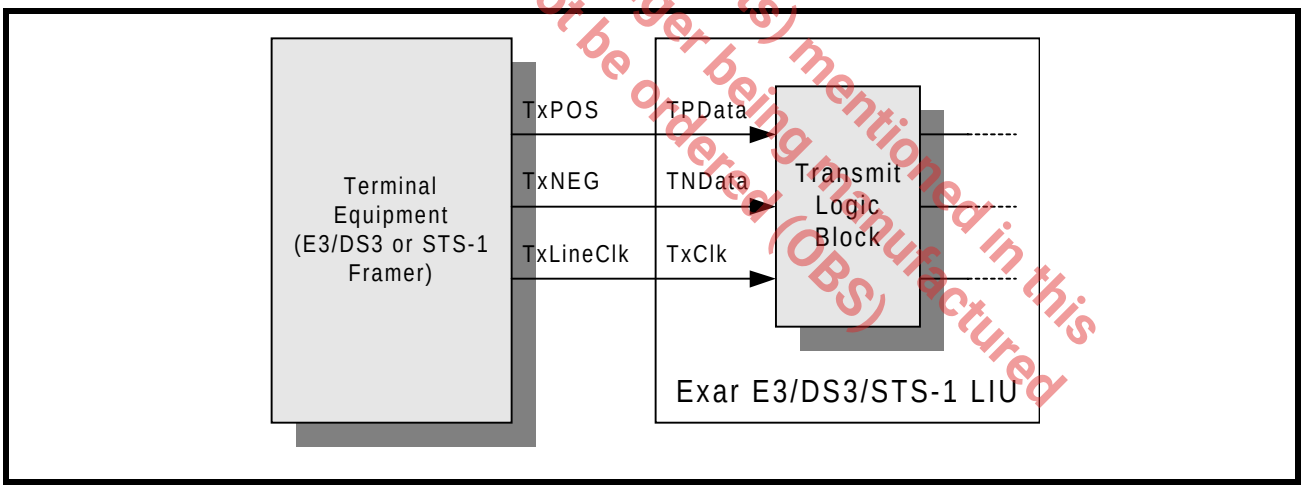
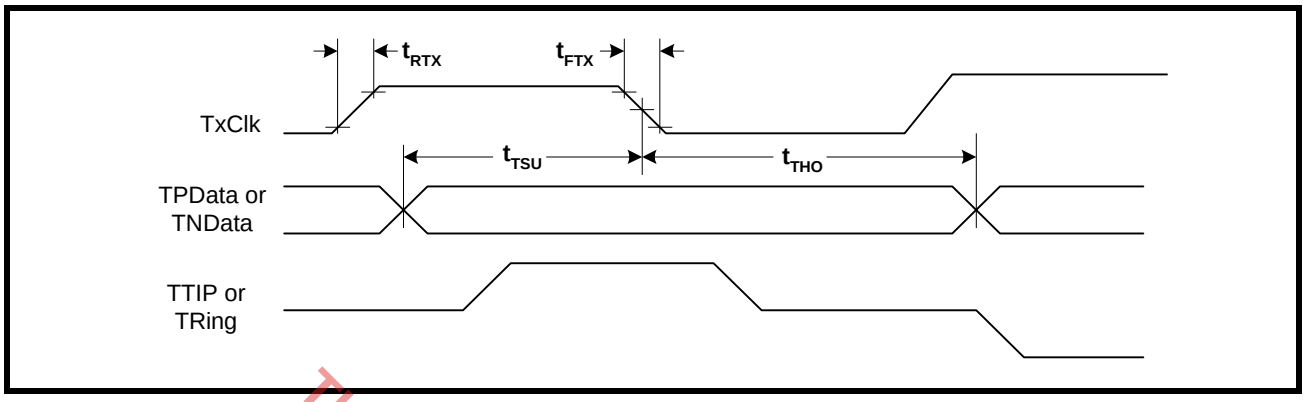


FIGURE 16. TRANSMITTER TERMINAL INPUT TIMING



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
TxClk	Duty Cycle	30	50	70	%
	TxClk Frequency E3 DS-3 STS-1		 34.368 44.736 51.84		 MHz MHz MHz
t_{RTX}	TxClk Rise Time (10% to 90%)			4	ns
t_{FTX}	TxClk Fall Time (10% to 90%)			4	ns
t_{TSU}	TPData/TNData to TxClk falling set up time	3			ns
t_{THO}	TPData/TNData to TxClk falling hold time	3			ns

FIGURE 17. SINGLE-RAIL OR NRZ DATA FORMAT (ENCODER AND DECODER ARE ENABLED)

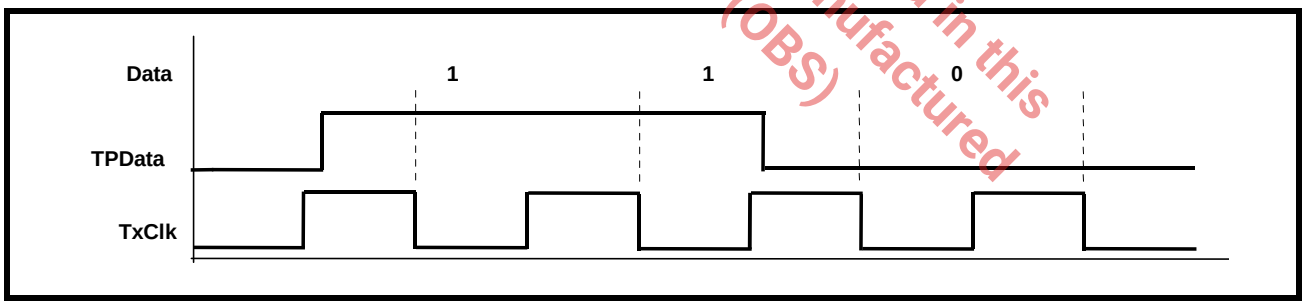
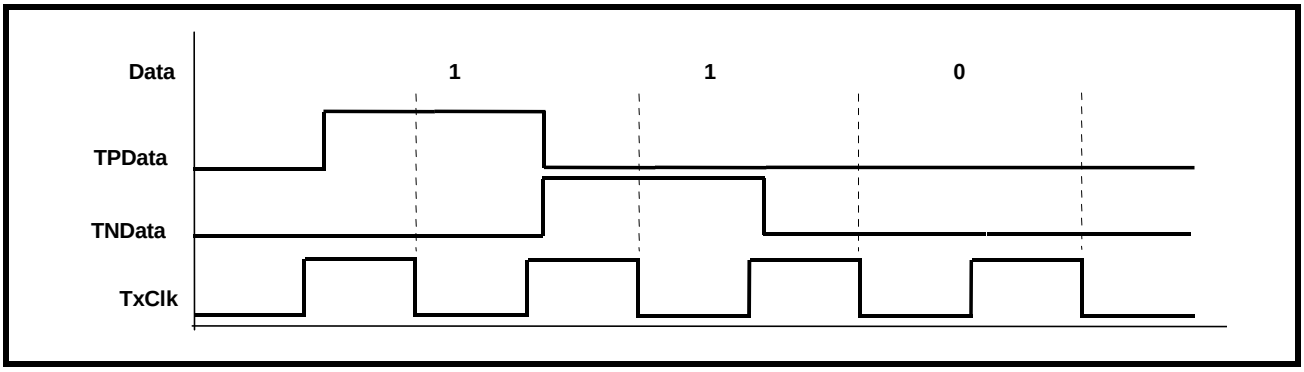


FIGURE 18. DUAL-RAIL DATA FORMAT (ENCODER AND DECODER ARE DISABLED)



4.2 Transmit Clock

The Transmit Clock applied via TxClk_n pins, for the selected data rate (for E3 = 34.368 MHz, DS3 = 44.736 MHz or STS-1 = 51.84 MHz), is duty cycle corrected by the internal PLL circuit to provide a 50% duty cycle clock to the pulse shaping circuit. This allows a 30% to 70% duty cycle Transmit Clock to be supplied.

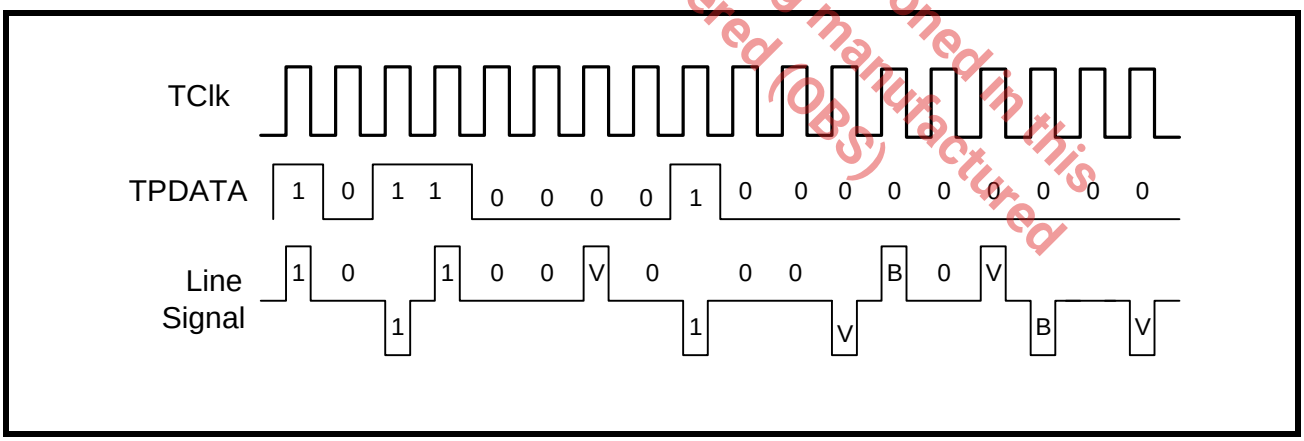
4.3 B3ZS/HDB3 ENCODER

When the Single-Rail (NRZ) data format is selected, the Encoder Block encodes the data into either B3ZS format (for either DS3 or STS-1) or HDB3 format (for E3).

4.3.1 B3ZS Encoding

An example of B3ZS encoding is shown in Figure 19. If the encoder detects an occurrence of three consecutive zeros in the data stream, it is replaced with either B0V or 00V, where 'B' refers to Bipolar pulse that is compliant with the Alternating polarity requirement of the AMI (Alternate Mark Inversion) line code and 'V' refers to a Bipolar Violation (e.g., a bipolar pulse that violates the AMI line code). The substitution of B0V or 00V is made so that an odd number of bipolar pulses exist between any two consecutive violation (V) pulses. This avoids the introduction of a DC component into the line signal.

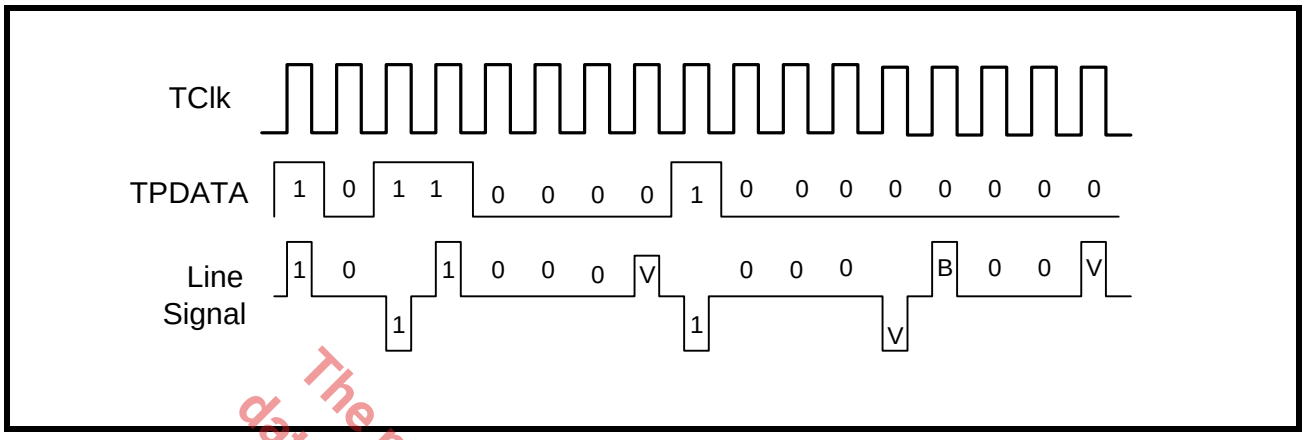
FIGURE 19. B3ZS ENCODING FORMAT



4.3.2 HDB3 Encoding

An example of the HDB3 encoding is shown in Figure 20. If the HDB3 encoder detects an occurrence of four consecutive zeros in the data stream, then the four zeros are substituted with either 000V or B00V pattern. The substitution code is made in such a way that an odd number of pulses exist between any consecutive V pulses. This avoids the introduction of DC component into the analog signal.

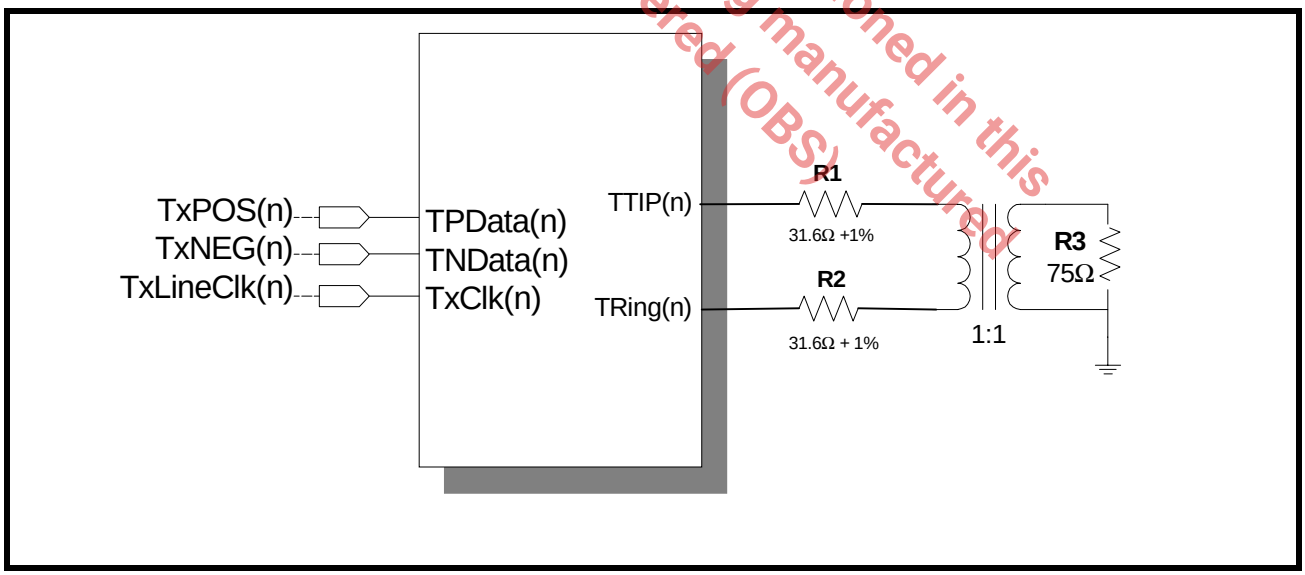
FIGURE 20. HDB3 ENCODING FORMAT



4.4 TRANSMIT PULSE SHAPER

The Transmit Pulse Shaper converts the B3ZS encoded digital pulses into a single analog Alternate Mark Inversion (AMI) pulse that meets the industry standard mask template requirements for STS-1 and DS3. For E3 mode, the pulse shaper converts the HDB3 encoded pulses into a single full amplitude square shaped pulse with very little slope. The Pulse Shaper Block also includes a Transmit Build Out Circuit, which can either be disabled or enabled by setting the TxLEV_n bit to "1" or "0" in the control register. For DS3/STS-1 rates, the Transmit Build Out Circuit is used to shape the transmit waveform that ensures that transmit pulse template requirements are met at the Cross-Connect system. The distance between the transmitter output and the Cross-Connect system can be between 0 to 450 feet. For E3 rate, since the output pulse template is measured at the secondary of the transformer and since there is no Cross-Connect system pulse template requirements, the Transmit Build Out Circuit is always disabled. The differential line driver increases the transmit waveform to appropriate level and drives into the 75Ω load as shown in Figure 21.

FIGURE 21. TRANSMIT PULSE SHAPE TEST CIRCUIT



4.4.1 Guidelines for using Transmit Build Out Circuit

If the distance between the transmitter and the DSX3 or STSX-1, Cross-Connect system, is less than 225 feet, enable the Transmit Build Out Circuit by setting the TxLEV_n control bit to "0". If the distance between the transmitter and the DSX3 or STSX-1 is greater than 225 feet, disable the Transmit Build Out Circuit.

4.5 E3 line side parameters

The XRT75R06D line output at the transformer output meets the pulse shape specified in ITU-T G.703 for 34.368 Mbits/s operation. The pulse mask as specified in ITU-T G.703 for 34.368 Mbits/s is shown in Figure 7.

FIGURE 22. PULSE MASK FOR E3 (34.368 MBITS/S) INTERFACE AS PER ITU-T G.703

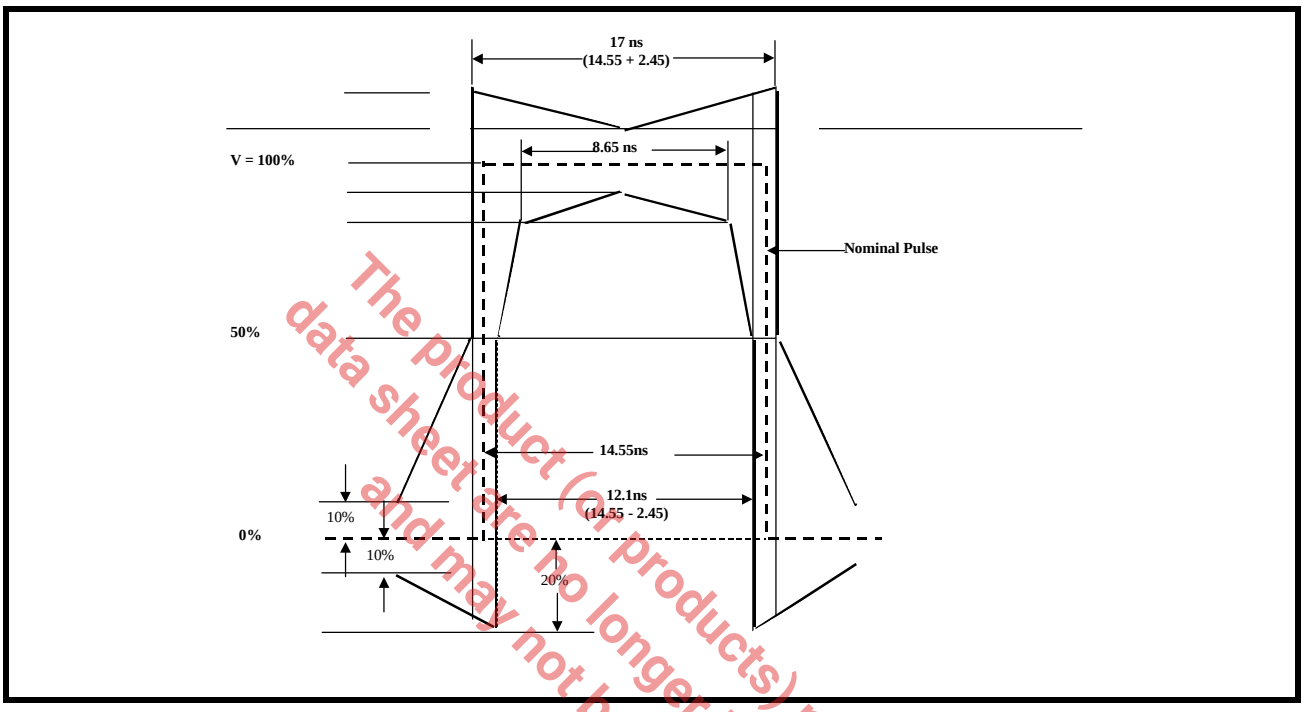


TABLE 3: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (Measured at secondary of the transformer)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
Transmit Output Pulse Width	12.5	14.55	16.5	ns
Transmit Intrinsic Jitter		0.02	0.05	UI_{PP}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1200		feet
Interference Margin	-20	-14		dB
Jitter Tolerance @ Jitter Frequency 800KHz	0.15	0.28		UI_{PP}
Signal level to Declare Loss of Signal			-35	dB
Signal Level to Clear Loss of Signal	-15			dB
Occurence of LOS to LOS Declaration Time	10		255	UI
Termination of LOS to LOS Clearance Time	10		255	UI

NOTE: *The above values are at TA = 25^{0}C and V_{DD} = 3.3 V± 5%.*

FIGURE 23. BELLCORE GR-253 CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

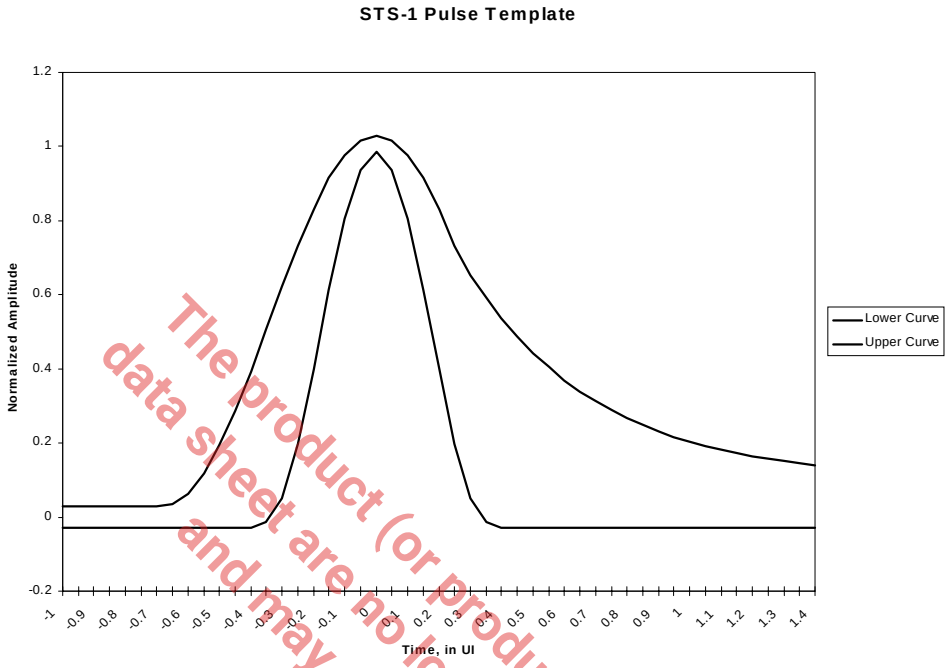


TABLE 4: STS-1 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.38$	- 0.03
$-0.38 \leq T \leq 0.36$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right\}\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.26$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right\}\right] + 0.03$
$0.26 \leq T \leq 1.4$	$0.1 + 0.61 \times e^{-2.4[T-0.26]}$

TABLE 5: STS-1 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-253)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.90	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	8.6	9.65	10.6	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
Transmit Intrinsic Jitter		0.02	0.05	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ Jitter Frequency 400 KHz	0.15			UI_{pp}
Signal Level to Declare Loss of Signal	Refer to Table 10			
Signal Level to Clear Loss of Signal	Refer to Table 10			

NOTE: *The above values are at TA = 25^{0}C and V_{DD} = 3.3 V ± 5%.*

FIGURE 24. TRANSMIT OUPUT PULSE TEMPLATE FOR DS3 AS PER BELLCORE GR-499

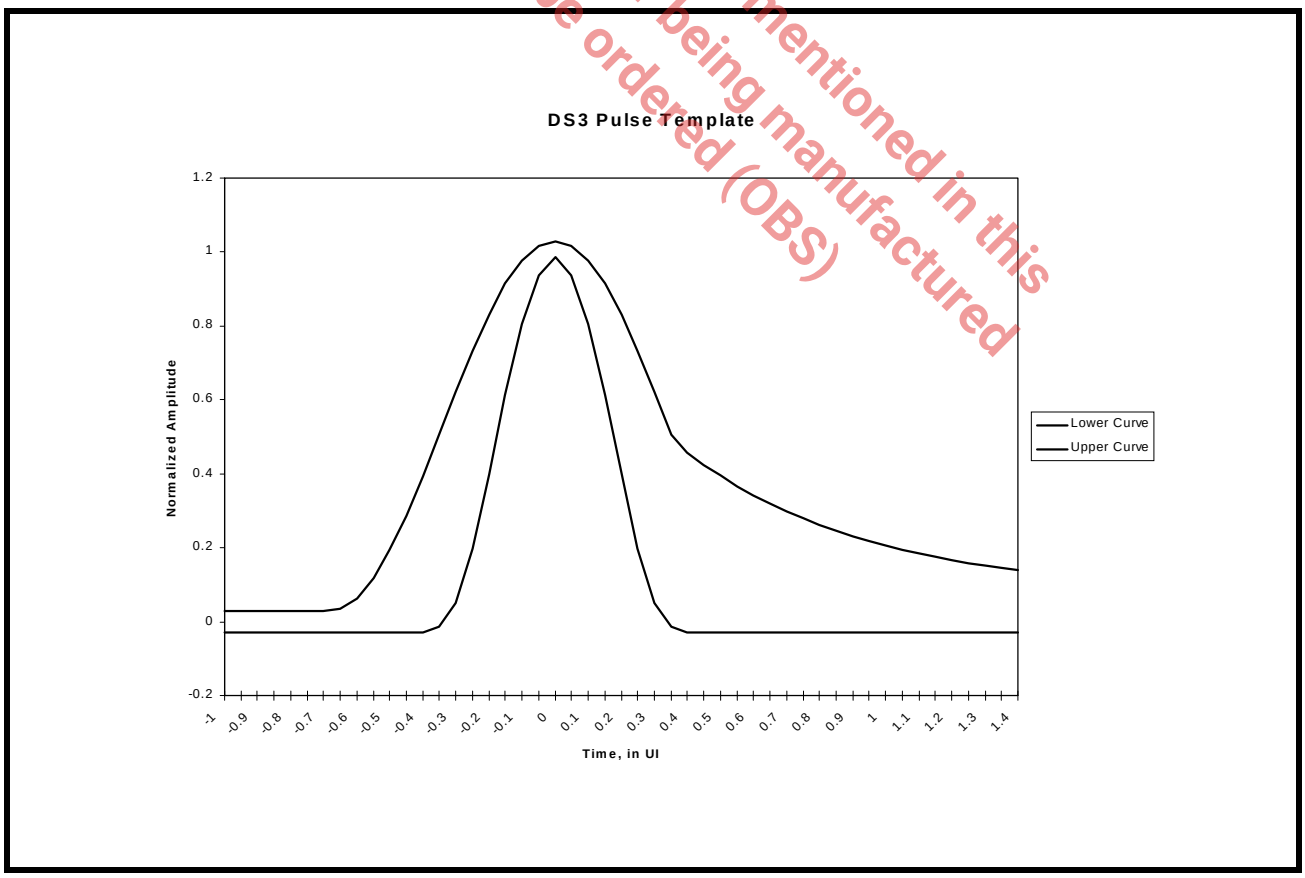


TABLE 6: DS3 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.36$	- 0.03
$-0.36 \leq T \leq 0.36$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right\}\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.36$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right\}\right] + 0.03$
$0.36 \leq T \leq 1.4$	$0.08 + 0.407 \times e^{-1.84[T-0.36]}$

TABLE 7: DS3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-499)

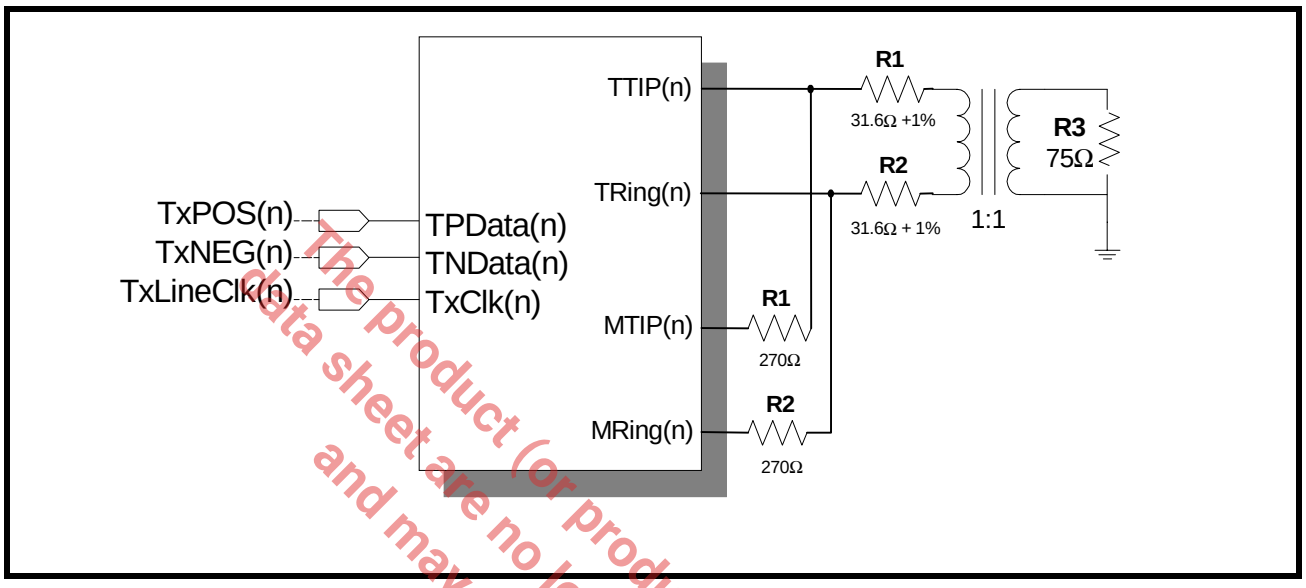
PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.85	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	10.10	11.18	12.28	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
Transmit Intrinsic Jitter		0.02	0.05	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ 400 KHz (Cat II)	0.15			UI_{pp}
Signal Level to Declare Loss of Signal	Refer to Table 10			
Signal Level to Clear Loss of Signal	Refer to Table 10			

NOTE: *The above values are at TA = 25^0C and V_{DD} = 3.3V ± 5%.*

4.6 Transmit Drive Monitor

This feature is used for monitoring the transmit line for occurrence of fault conditions such as a short circuit on the line or a defective line driver. To activate this function, connect MTIP_n pins to the TTIP_n lines via a 270Ω resistor and MRing_n pins to TRing_n lines via 270Ω resistor as shown in Figure 25.

FIGURE 25. TRANSMIT DRIVER MONITOR SET-UP.



When the MTIP_n and MRing_n are connected to the TTIP_n and TRing_n lines, the drive monitor circuit monitors the line for transitions. The DMO_n (Drive Monitor Output) will be asserted "Low" as long as the transitions on the line are detected via MTIP_n and MRing_n. If no transitions on the line are detected for 128 ± 32 TxClk_n periods, the DMO_n output toggles "High" and when the transitions are detected again, DMO_n toggles "Low".

NOTE: *The Drive Monitor Circuit is only for diagnostic purpose and does not have to be used to operate the transmitter.*

4.7 Transmitter Section On/Off

The transmitter section of each channel can either be turned on or off. To turn on the transmitter, set the input pin TxON to "High" and write a "1" to the TxON_n control bit. When the transmitter is turned off, TTIP_n and TRing_n are tri-stated.

NOTES:

1. *This feature provides support for Redundancy.*
2. *To permit a system designed for redundancy to quickly shut-off the defective line card and turn on the back-up line card, writing a "1" to the TxON_n control bits transfers the control to TxON pin.*

5.0 JITTER

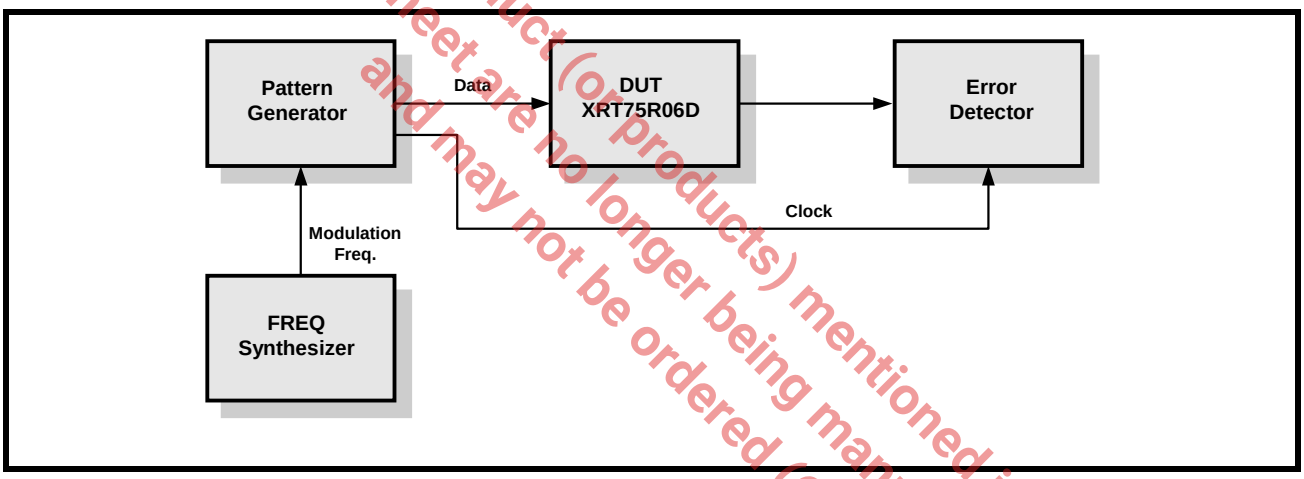
There are three fundamental parameters that describe circuit performance relative to jitter

- **Jitter Tolerance**
- **Jitter Transfer**
- **Jitter Generation**

5.1 JITTER TOLERANCE

Jitter tolerance is a measure of how well a Clock and Data Recovery unit can successfully recover data in the presence of various forms of jitter. It is characterized by the amount of jitter required to produce a specified bit error rate. The tolerance depends on the frequency content of the jitter. Jitter Tolerance is measured as the jitter amplitude over a jitter spectrum for which the clock and data recovery unit achieves a specified bit error rate (BER). To measure the jitter tolerance as shown in Figure 26, jitter is introduced by the sinusoidal modulation of the serial data bit sequence. Input jitter tolerance requirements are specified in terms of compliance with jitter mask which is represented as a combination of points. Each point corresponds to a minimum amplitude of sinusoidal jitter at a given jitter frequency.

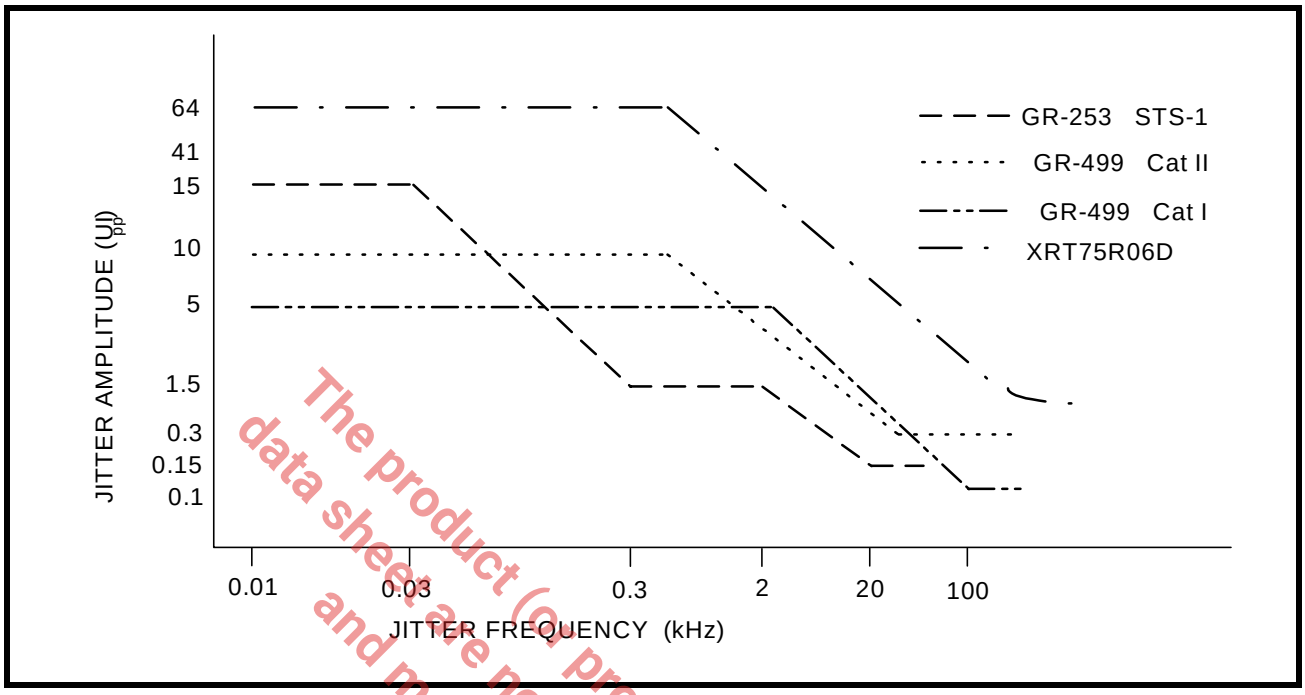
FIGURE 26. JITTER TOLERANCE MEASUREMENTS



5.1.1 DS3/STS-1 Jitter Tolerance Requirements

Bellcore GR-499 CORE specifies the minimum requirement of jitter tolerance for Category I and Category II. The jitter tolerance requirement for Category II is the most stringent. Figure 27 shows the jitter tolerance curve as per GR-499 specification.

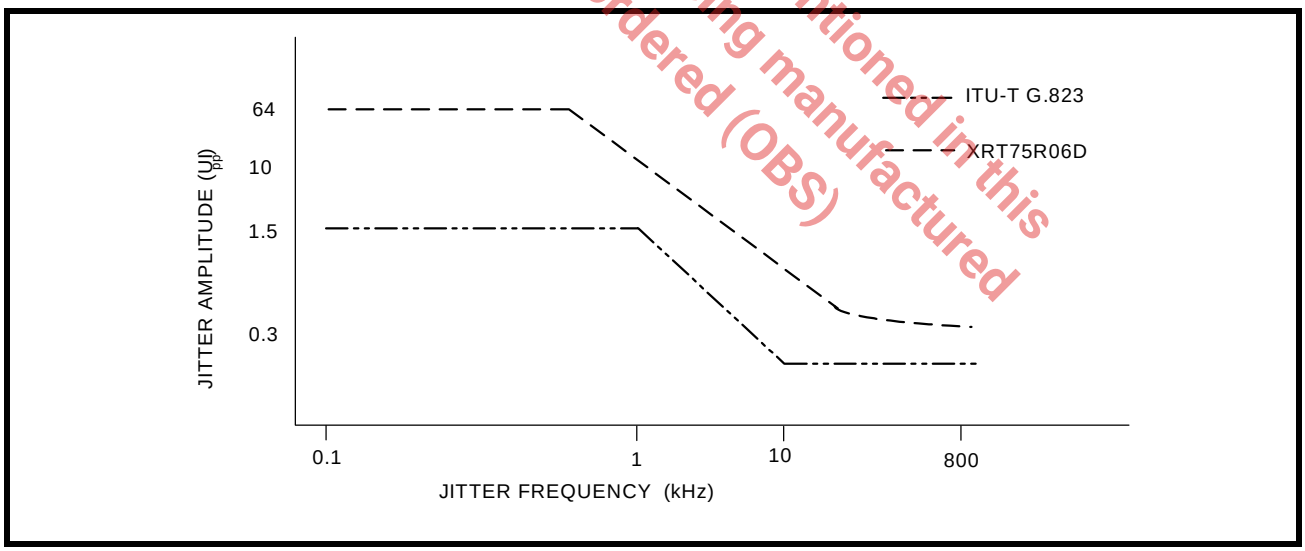
FIGURE 27. INPUT JITTER TOLERANCE FOR DS3/STS-1



5.1.2 E3 Jitter Tolerance Requirements

ITU-T G.823 standard specifies that the clock and data recovery unit must be able to tolerate jitter up to certain specified limits. Figure 28 shows the tolerance curve.

FIGURE 28. INPUT JITTER TOLERANCE FOR E3



As shown in the Figures above, in the jitter tolerance measurement, the dark line indicates the minimum level of jitter that the E3/DS3/STS-1 compliant component must tolerate. Table 8 below shows the jitter amplitude versus the modulation frequency for various standards.

TABLE 8: JITTER AMPLITUDE VERSUS MODULATION FREQUENCY (JITTER TOLERANCE)

BIT RATE (KB/S)	STANDARD	INPUT JITTER AMPLITUDE (UI P-P)			MODULATION FREQUENCY				
		A1	A2	A3	F1(HZ)	F2(HZ)	F3(KHZ)	F4(KHZ)	F5(KHZ)
34368	ITU-T G.823	1.5	0.15	-	100	1000	10	800	-
44736	GR-499 CORE Cat I	5	0.1	-	10	2.3k	60	300	-
44736	GR-499 CORE Cat II	10	0.3	-	10	669	22.3	300	-
51840	GR-253 CORE Cat II	15	1.5	0.15	10	30	300	2	20

5.2 JITTER TRANSFER

Jitter Transfer function is defined as the ratio of jitter on the output relative to the jitter applied on the input versus frequency. There are two distinct characteristics in jitter transfer, jitter gain (jitter peaking) defined as the highest ratio above 0dB and jitter transfer bandwidth. The overall jitter transfer bandwidth is controlled by a low bandwidth loop, typically using a voltage-controlled crystal oscillator (VCXO).

The jitter transfer function is a ratio between the jitter output and jitter input for a component, or system often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter. A zero dB jitter transfer indicates the element had no effect on jitter. Table 9 shows the jitter transfer characteristics and/or jitter attenuation specifications for various data rates:

TABLE 9: JITTER TRANSFER SPECIFICATION/REFERENCES

E3	DS3	STS-1
ETSI TBR-24	GR-499 CORE section 7.3.2 Category I and Category II	GR-253 CORE section 5.6.2.1

NOTE: *The above specifications can be met only with a jitter attenuator that supports E3/DS3/STS-1 rates.*

5.3 Jitter Attenuator

An advanced crystal-less jitter attenuator per channel is included in the XRT75R06D. The jitter attenuator requires no external crystal nor high-frequency reference clock. By clearing or setting the JATx/Rx_n bits in the channel control registers selects the jitter attenuator either in the Receive or Transmit path on per channel basis. The FIFO size can be either 16-bit or 32-bit. The bits JA0_n and JA1_n can be set to appropriate combination to select the different FIFO sizes or to disable the Jitter Attenuator on a per channel basis. Data is clocked into the FIFO with the associated clock signal (TxClk or RxClk) and clocked out of the FIFO with the dejittered clock. When the FIFO is within two bits of overflowing or underflowing, the FIFO limit status bit, FL_n is set to “1” in the Alarm status register. Reading this bit clears the FIFO and resets the bit into default state.

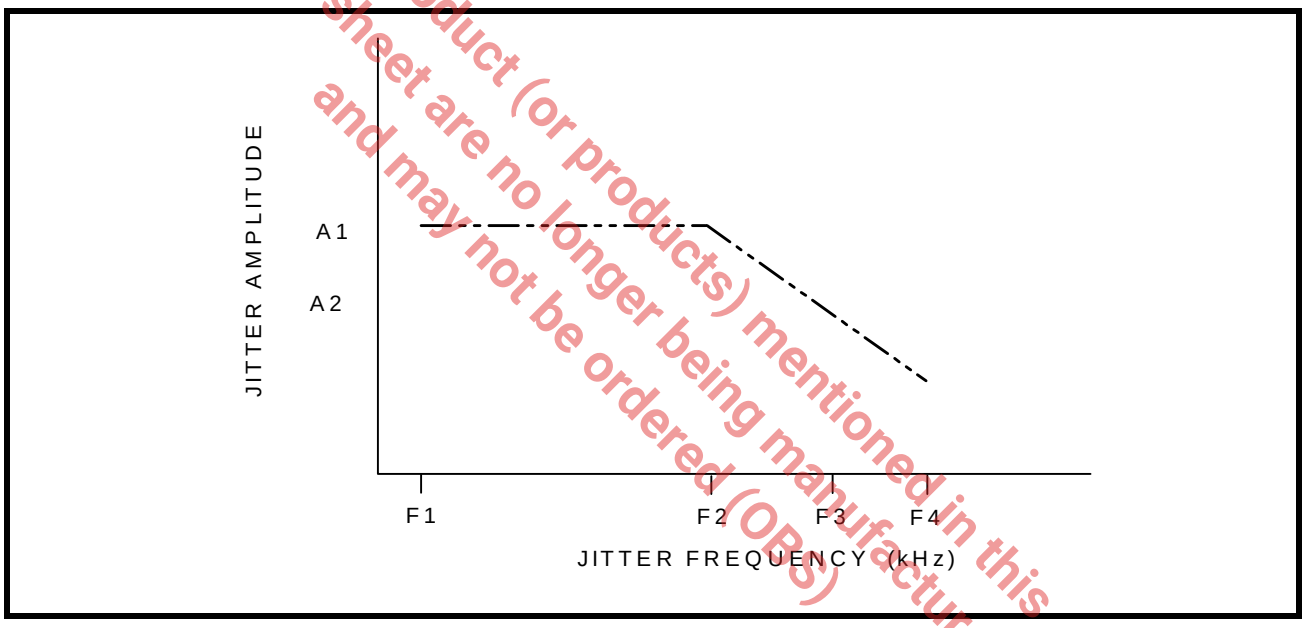
NOTE: *It is recommended to select the 16-bit FIFO for delay-sensitive applications as well as for removing smaller amounts of jitter. Table 10 specifies the jitter transfer mask requirements for various data rates:*

TABLE 10: JITTER TRANSFER PASS MASKS

RATE (KBITS)	MASK	F1 (HZ)	F2 (HZ)	F3 (HZ)	F4 (KHZ)	A1(dB)	A2(dB)
34368	G.823 ETSI-TBR-24	100	300	3K	800K	0.5	-19.5
44736	GR-499, Cat I GR-499, Cat II GR-253 CORE	10 10 10	10k 56.6k 40	- - -	15k 300k 15k	0.1 0.1 0.1	- - -
51840	GR-253 CORE	10	40k	-	400k	0.1	-

The jitter attenuator within the XRT75R06D meets the latest jitter attenuation specifications and/or jitter transfer characteristics as shown in the Figure 29.

FIGURE 29. JITTER TRANSFER REQUIREMENTS AND JITTER ATTENUATOR PERFORMANCE



5.3.1 JITTER GENERATION

Jitter Generation is defined as the process whereby jitter appears at the output port of the digital equipment in the absence of applied input jitter. Jitter Generation is measured by sending jitter free data to the clock and data recovery circuit and measuring the amount of jitter on the output clock or the re-timed data. Since this is essentially a noise measurement, it requires a definition of bandwidth to be meaningful. The bandwidth is set according to the data rate. In general, the jitter is measured over a band of frequencies.

6.0 DIAGNOSTIC FEATURES

6.1 PRBS Generator and Detector

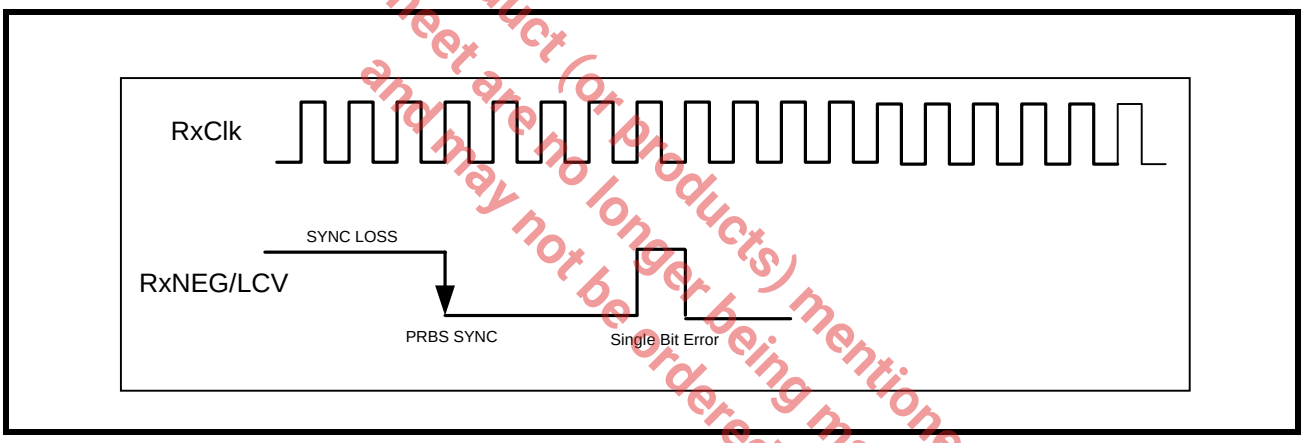
The XRT75R06D contains an on-chip Pseudo Random Binary Sequence (PRBS) generator and detector for diagnostic purpose. With the PRBSEN_n bit = "1", the transmitter will send out PRBS of 2^{23}-1 in E3 rate or 2^{15}-1 in STS-1/DS3 rate. At the same time, the receiver PRBS detector is also enabled. When the correct PRBS pattern is detected by the receiver, the RNEG/LCV pin will go "Low" to indicate PRBS synchronization has been achieved. When the PRBS detector is not in sync the PRBSLS bit will be set to "1" and RNEG/LCV pin will go "High".

With the PRBS mode enabled, the user can also insert a single bit error by toggling "INSPRBS" bit. This is done by writing a "1" to INSPRBS bit. The receiver at RNEG/LCV pin will pulse "High" for one RxClk cycle for every bit error detected. Any subsequent single bit error insertion must be done by first writing a "0" to INSPRBS bit and followed by a "1".

Figure 30 shows the status of RNEG/LCV pin when the XRT75R06D is configured in PRBS mode.

NOTE: *In PRBS mode, the device is forced to operate in Single-Rail Mode.*

FIGURE 30. PRBS MODE



6.2 LOOPBACKS

The XRT75R06D offers three loopback modes for diagnostic purposes. The loopback modes are selected via the RLB_n and LLB_n bits n the Channel control registers select the loopback modes.

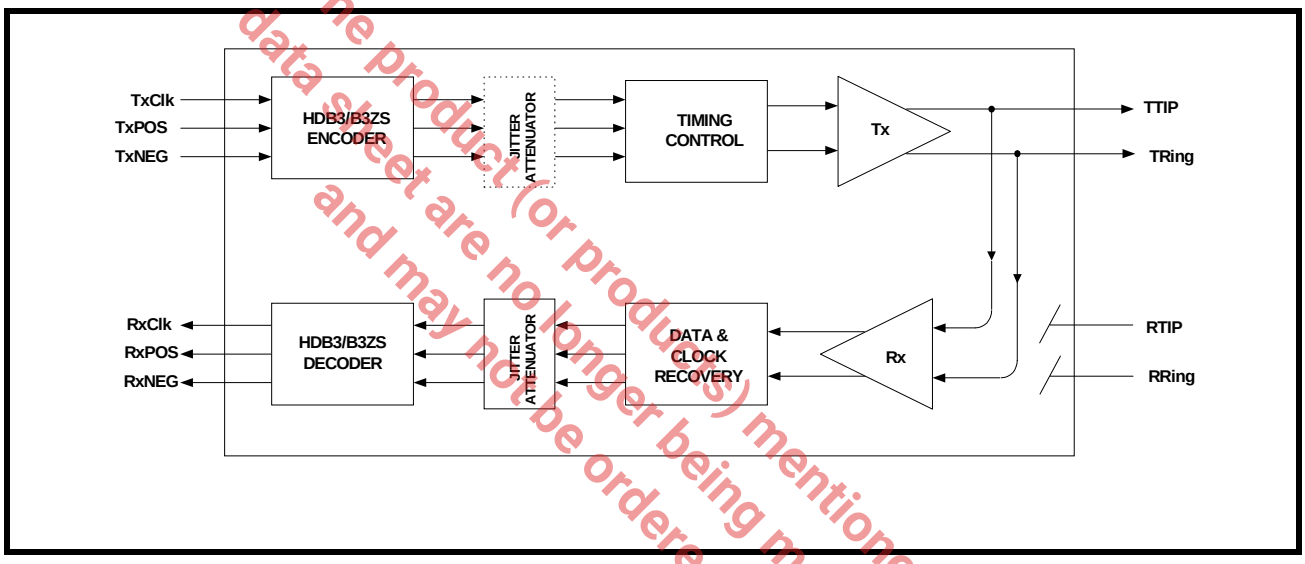
6.2.1 ANALOG LOOPBACK

In this mode, the transmitter outputs TTIP_n and TRing_n are internally connected to the receiver inputs RTIP_n and RRing_n as shown in Figure 31. Data and clock are output at RxClk_n, RxPOS_n and RxNEG_n pins for the corresponding transceiver. Analog loopback exercises most of the functional blocks of the device including the jitter attenuator which can be selected in either the transmit or receive path.

NOTES:

1. *In the Analog loopback mode, data is also output via TTIP_n and TRing_n pins.*
2. *Signals on the RTIP_n and RRing_n pins are ignored during analog loopback.*

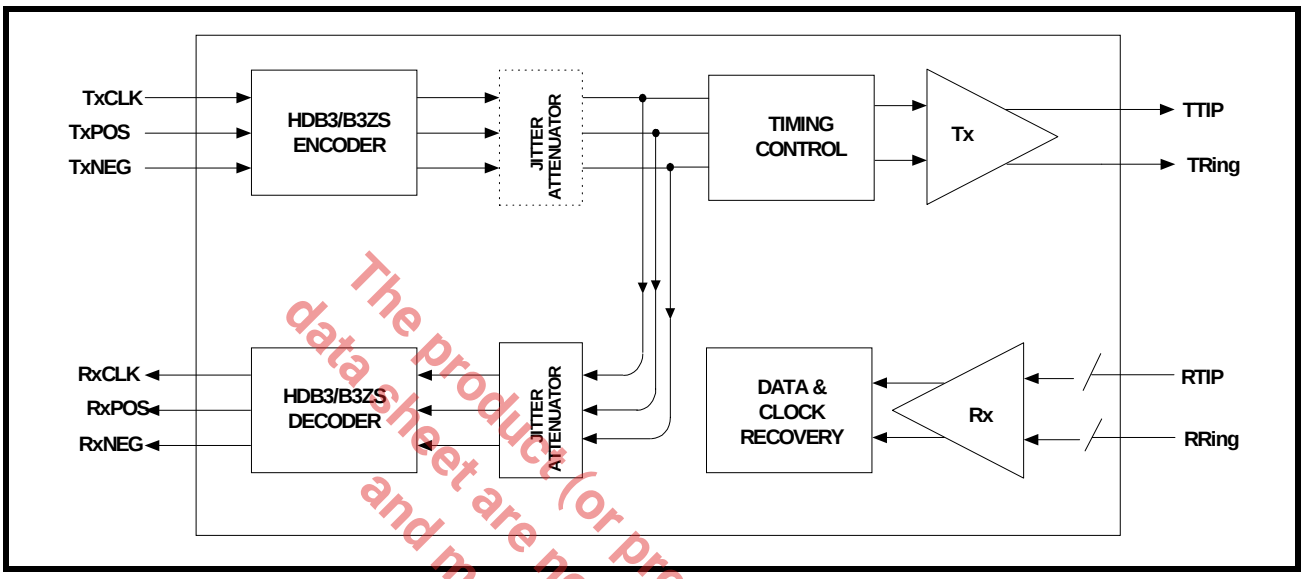
FIGURE 31. ANALOG LOOPBACK



6.2.2 DIGITAL LOOPBACK

When the Digital Loopback is selected, the transmit clock TxClk_n and transmit data inputs (TxPOS_n & TxNEG_n are looped back and output onto the RxClk_n, RxPOS_n and RxNEG_n pins as shown in Figure 32.

FIGURE 32. DIGITAL LOOPBACK

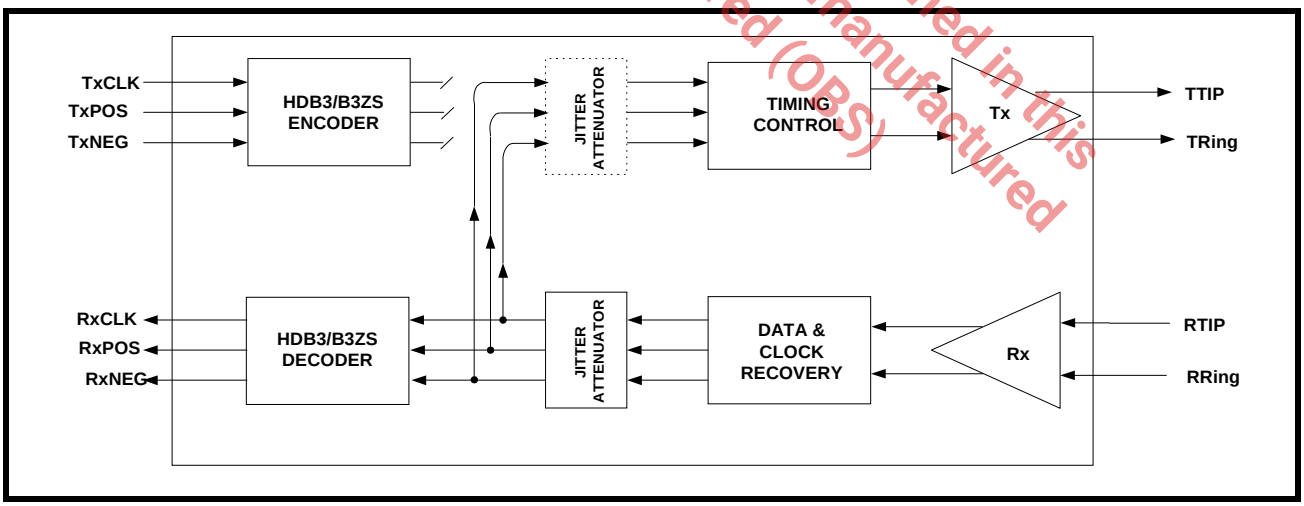


6.2.3 REMOTE LOOPBACK

With Remote loopback activated as shown in Figure 33, the receive data on RTIP and RRing is looped back after the jitter attenuator (if selected in receive or transmit path) to the transmit path using RxClk as transmit timing. The receive data is also output via the RxPOS and RxNEG pins.

NOTE: *Input signals on TxClk, TxPOS and TxNEG are ignored during Remote loopback.*

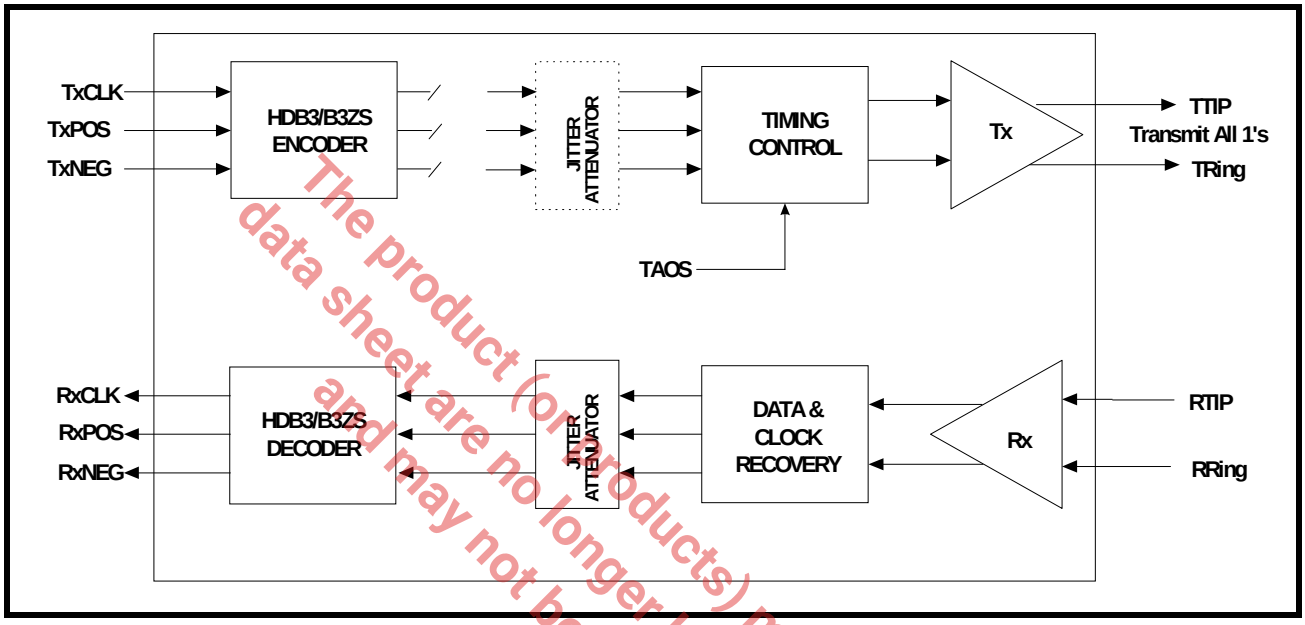
FIGURE 33. REMOTE LOOPBACK



6.3 TRANSMIT ALL ONES (TAOS)

Transmit All Ones (TAOS) can be set by setting the TAOS_n control bits to “1” in the Channel control registers. When the TAOS is set, the Transmit Section generates and transmits a continuous AMI all “1’s” pattern on TTIP_n and TRing_n pins. The frequency of this ones pattern is determined by TxClk_n. the TAOS data path is shown in Figure 34. TAOS does not operate in Analog loopback or Remote loopback modes, however will function in Digital loopback mode.

FIGURE 34. TRANSMIT ALL ONES (TAOS)



7.0 MICROPROCESSOR INTERFACE BLOCK

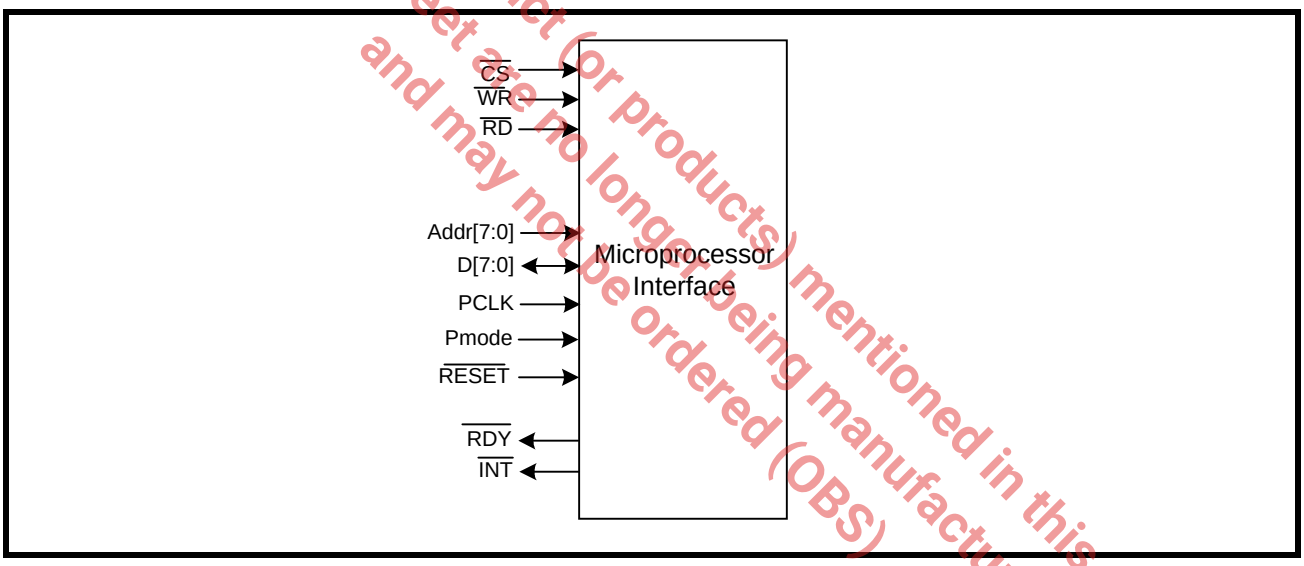
The Microprocessor Interface section supports communication between the local microprocessor (µP) and the LIU. The XRT75R06D supports a parallel interface asynchronously or synchronously timed to the LIU. The microprocessor interface is selected by the state of the Pmode input pin. Selecting the microprocessor interface mode is shown in Table 11.

TABLE 11: SELECTING THE MICROPROCESSOR INTERFACE MODE

PMODE	MICROPROCESSOR MODE
"Low"	Asynchronous Mode
"High"	Synchronous Mode

The local µP configures the LIU by writing data into specific addressable, on-chip Read/Write registers. The µP provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The µP also supports polled and interrupt driven environments. A simplified block diagram of the microprocessor is shown in Figure 35.

FIGURE 35. SIMPLIFIED BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK



7.1 THE MICROPROCESSOR INTERFACE BLOCK SIGNALS

The LIU may be configured into different operating modes and have its performance monitored by software through a standard microprocessor using data, address and control signals. These interface signals are described below in Table 12. The microprocessor interface can be configured to operate in Asynchronous mode or Synchronous mode.

TABLE 12: XRT75R06D MICROPROCESSOR INTERFACE SIGNALS

PIN NAME	TYPE	DESCRIPTION
Pmode	I	**Microprocessor Interface Mode Select Input pin** This pin is used to specify the microprocessor interface mode.
D[7:0]	I/O	**Bi-Directional Data Bus for register "Read" or "Write" Operations.**
Addr[7:0]	I	**Eight-Bit Address Bus Inputs** The XRT75R06D LIU microprocessor interface uses a direct address bus. This address bus is provided to permit the user to select an on-chip register for Read/Write access.
$\overline{CS}$	I	**Chip Select Input** This active low signal selects the microprocessor interface of the XRT75R06D LIU and enables Read/Write operations with the on-chip register locations.
$\overline{RD}$	I	**Read Signal** This active low input functions as the read signal from the local µP. When this pin is pulled "Low" (if $\overline{CS}$ is "Low") the LIU is informed that a read operation has been requested and begins the process of the read cycle.
$\overline{WR}$	I	**Write Signal** This active low input functions as the write signal from the local µP. When this pin is pulled "Low" (if $\overline{CS}$ is "Low") the LIU is informed that a write operation has been requested and begins the process of the write cycle.
$\overline{RDY}$	O	**Ready Output** This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command.
$\overline{INT}$	O	**Interrupt Output** This active low signal is provided by the LIU to alert the local mP that a change in alarm status has occured. This pin is Reset Upon Read (RUR) once the alarm status registers have been cleared.
$\overline{RESET}$	I	**Reset Input** This active low input pin is used to Reset the LIU.

7.2 ASYNCHRONOUS AND SYNCHRONOUS DESCRIPTION

Whether the LIU is configured for Asynchronous or Synchronous mode, the following descriptions apply. The synchronous mode requires an input clock (PCLK) to be used as the microprocessor timing reference. Read and Write operations are described below.

Read Cycle (For Pmode = "0" or "1")

Whenever the local µP wishes to read the contents of a register, it should do the following.

1. Place the address of the target register on the address bus input pins Addr[7:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables communication between the µP and the LIU microprocessor interface block.
3. Next, the µP should indicate that this current bus cycle is a Read operation by toggling the $\overline{RD}$ input pin "Low". This action enables the bi-directional data bus output drivers of the LIU.
4. After the µP toggles the Read signal "Low", the LIU will toggle the $\overline{RDY}$ output pin "Low". The LIU does this to inform the µP that the data is available to be read by the µP, and that it is ready for the next command.
5. After the µP detects the $\overline{RDY}$ signal and has read the data, it can terminate the Read Cycle by toggling the $\overline{RD}$ input pin "High".
6. The $\overline{CS}$ input pin must be pulled "High" before a new command can be issued.

Write Cycle (For Pmode = "0" or "1")

Whenever a local µP wishes to write a byte or word of data into a register within the LIU, it should do the following.

1. Place the address of the target register on the address bus input pins Addr[7:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables communication between the µP and the LIU microprocessor interface block.
3. The µP should then place the byte or word that it intends to write into the target register, on the bi-directional data bus D[7:0].
4. Next, the µP should indicate that this current bus cycle is a Write operation by toggling the $\overline{WR}$ input pin "Low". This action enables the bi-directional data bus input drivers of the LIU.
5. After the µP toggles the Write signal "Low", the LIU will toggle the $\overline{RDY}$ output pin "Low". The LIU does this to inform the µP that the data has been written into the internal register location, and that it is ready for the next command.
6. The $\overline{CS}$ input pin must be pulled "High" before a new command can be issued.

FIGURE 36. ASYNCHRONOUS µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

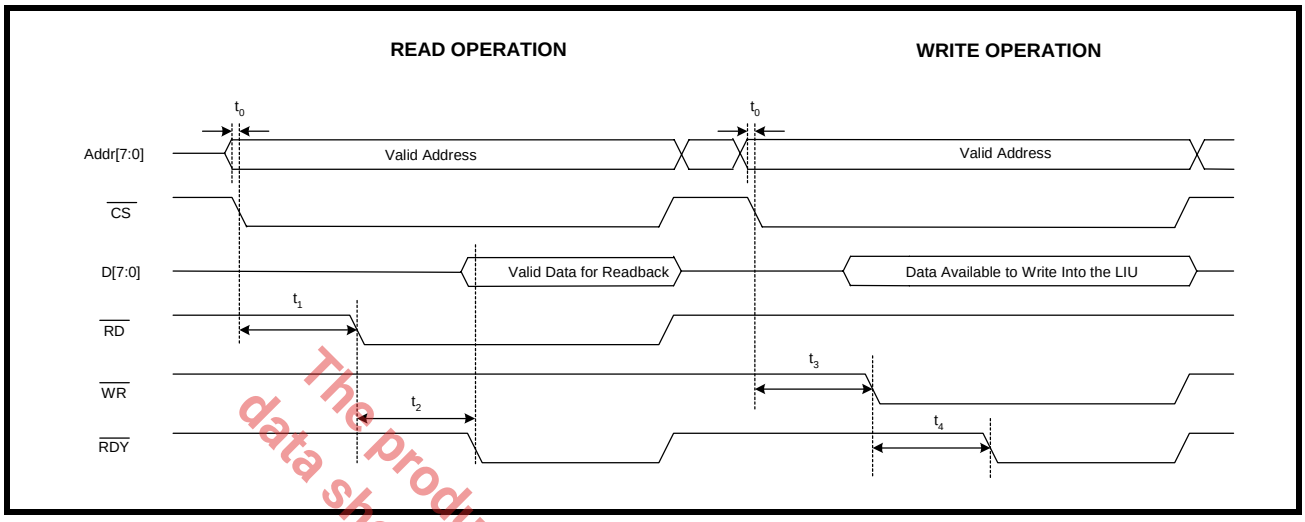


TABLE 13: ASYNCHRONOUS TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	0	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	65	ns
NA	$\overline{RD}$ Pulse Width (t_2)	70	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	0	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	65	ns
NA	$\overline{WR}$ Pulse Width (t_4)	70	-	ns

FIGURE 37. SYNCHRONOUS µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

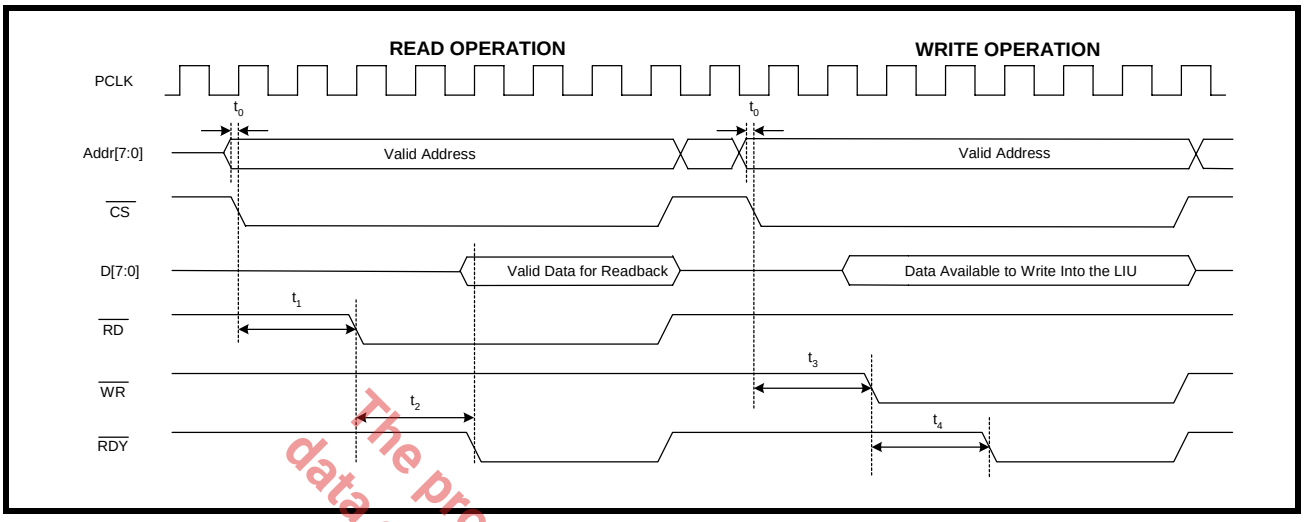
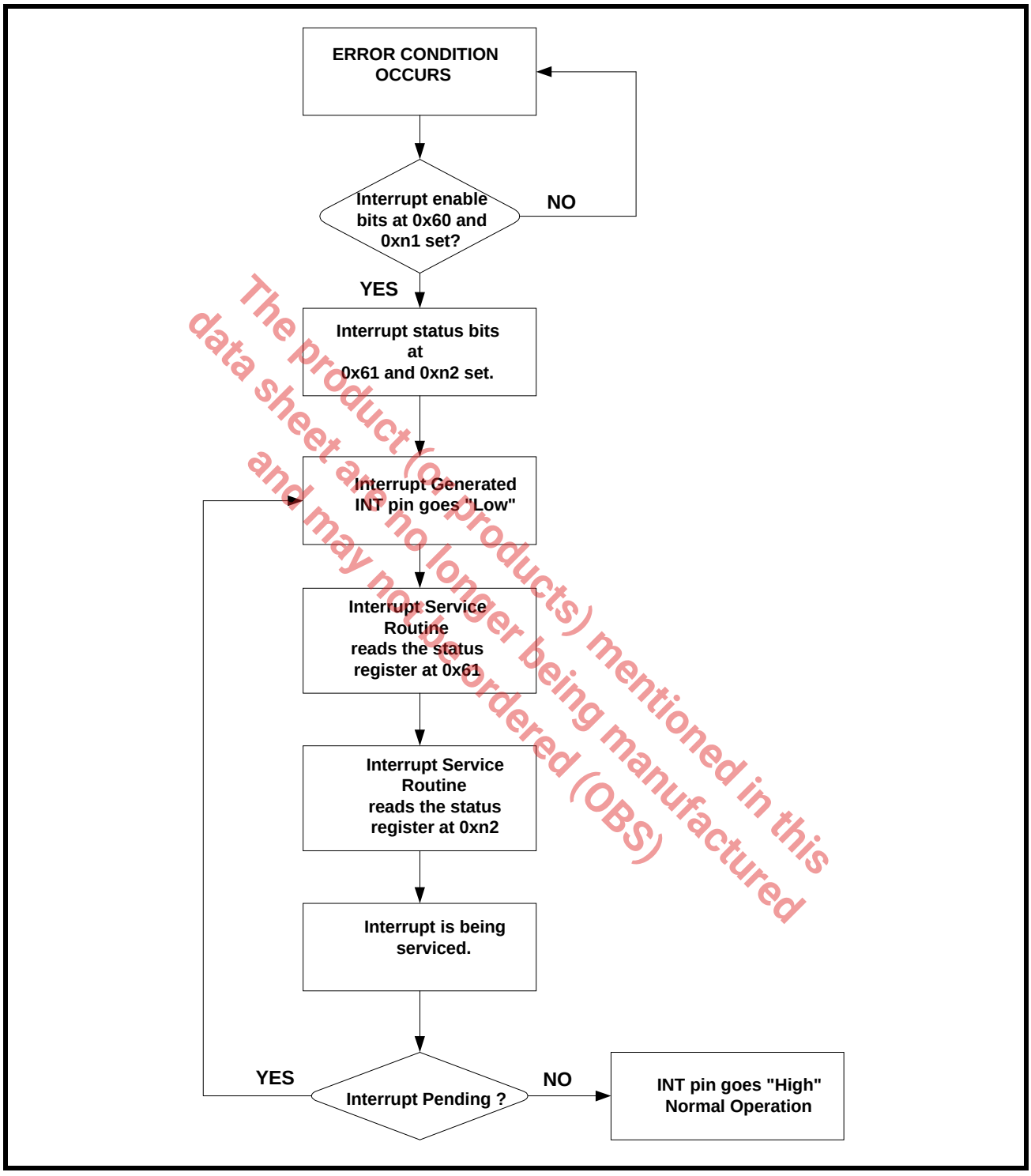


TABLE 14: SYNCHRONOUS TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	0	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	35	ns, see note 1
NA	$\overline{RD}$ Pulse Width (t_2)	40	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	0	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	35	ns, see note 1
NA	$\overline{WR}$ Pulse Width (t_4)	40	-	ns
	PCLK Period	15		ns
	PCLK Duty Cycle			
	PCLK "High/Low" time			

*NOTE: 1. This timing parameter is based on the frequency of the synchronous clock (PCLK). To determine the access time, use the following formula: ($PCLK_{period}$ * 2) + 5ns*

FIGURE 38. INTERRUPT PROCESS



7.2.1 Hardware Reset:

The hardware reset is initiated by pulling the $\overline{\text{RESET}}$ pin "Low" for a minimum of 5 µs. After the $\overline{\text{RESET}}$ pin is released, the register values are put in default states.

TABLE 15: REGISTER MAP AND BIT NAMES

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x00	APS/Redun-dancy #1	Reserved		TxON_5	TxON_4	TxON_3	TxON_2	TxON-1	TxON_0
0x08	APS/ Redun-dancy #2	Reserved		RxON_5	RxON_4	RxON_3	RxON_2	RxON_1	RxON_0
0x60	Interrupt Enable (read/write)	Reserved		INTEN_5	INTEN_4	INTEN_3	INTEN_2	INTEN_1	INTEN_0
0x61	Interrupt Status (read only)	Reserved		INTST_5	INTST_4	INTST_3	INTST_2	INTST_1	INTST_0
0x62 - 0x6D		Reserved							
0x6E	Chip_id (read only)	0	1	0	1	0	1	0	1
0x6F	Chip_revision _id (read only)	Chip version number							

TABLE 16: REGISTER MAP DESCRIPTION - GLOBAL

<table>
<tr><th>ADDRESS (HEX)</th><th>TYPE</th><th>REGISTER NAME</th><th>SYMBOL</th><th>DESCRIPTION</th><th>DEFAULT VALUE</th></tr>
<tr><td>0x00</td><td>R/W</td><td>APS # 1</td><td>TxON_n</td><td>Table below shows the status of the transmitter based on the bit and pin setting.

<table><tr><th>Bit</th><th>Pin</th><th>Transmitter Status</th></tr><tr><td>0</td><td>0</td><td>OFF</td></tr><tr><td>0</td><td>1</td><td>OFF</td></tr><tr><td>1</td><td>0</td><td>OFF</td></tr><tr><td>1</td><td>1</td><td>ON</td></tr></table></td><td>0</td></tr>
<tr><td>0x08</td><td>R/W</td><td>APS # 2</td><td>RxON_n</td><td>Set this bit to turn on individual Receiver.</td><td>0</td></tr>
<tr><td>0x60</td><td>R/W</td><td>Interrupt Enable</td><td>INTEN_n</td><td>Set this bit to enable the interrupts on per channel basis.</td><td>0</td></tr>
<tr><td>0x61</td><td>ROR</td><td>Interrupt Status</td><td>INTST_n</td><td>Bits are set when an interrupt occurs.The respective source level interrupt status registers are read to determine the cause of interrupt.</td><td>0</td></tr>
<tr><td>0x62 - 0x6D</td><td colspan="5">Reserved</td></tr>
<tr><td>0x6E</td><td>R</td><td>Device _ id</td><td>Chip_id</td><td>This read only register contains device id.</td><td>01010101</td></tr>
<tr><td>0x6F</td><td>R</td><td>Version Number</td><td>Chip_version</td><td>This read only register contains chip version number</td><td></td></tr>
</table>

TABLE 17: REGISTER MAP AND BIT NAMES - CHANNEL N REGISTERS (N = 0,1,2,3,4,5)

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x01 (ch 0) 0x11 (ch 1) 0x21 (ch 2) 0x31 (ch 3) 0x41 (ch 4) 0x51 (ch 5)	Interrupt Enable (read/write)	Reserved		PRBSERCNTIE_n	PRBSERIE_n	FLIE_n	RLOLIE_n	RLOSIE_n	DMOIE_n
0x02 (ch 0) 0x12 (ch 1) 0x22 (ch 2) 0x32 (ch 3) 0x42 (ch 4) ox52 (ch 5)	Interrupt Status (reset on read)	Reserved		PRBSERCNTIS_n	PRBSERIS_n	FLIS_n	RLOLIS_n	RLOSIS_n	DMOIS_n

TABLE 17: REGISTER MAP AND BIT NAMES - CHANNEL N REGISTERS (N = 0,1,2,3,4,5)

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x03 (ch 0) 0x13 (ch 1) 0x23 (ch 2) 0x33 (ch 3) 0x43 (ch 4) 0x53 (ch 5)	Alarm Status (read only)	Reserved	PRBSLS_n	DLOS_n	ALOS_n	FL_n	RLOL_n	RLOS_n	DMO_n
0x04 (ch 0) 0x14 (ch 1) 0x24 (ch 2) 0x34 (ch 3) 0x44 (ch 4) 0x54 (ch 5)	Transmit Control (read/write)	Reserved		TxMON_n	INSPRBS_n	Reserved	TAOS_n	TxCLKINV_n	TxLEV_n
0x05 (ch 0) 0x15 (ch 1) 0x25 (ch 2) 0x35 (ch 3) 0x45 (ch 4) 0x55 (ch 5)	Receive Control (read/write)	Reserved		DLOSDIS_n	ALOSDIS_n	RxCLKINV_n	LOSMUT_n	RxMON_n	REQEN_n
0x06 (ch 0) 0x16 (ch 1) 0x26 (ch 2) 0x36 (ch 3) 0x46 (ch 4) 0x56 (ch 5)	Block Control (read/write)	Reserved	CLKOUTEN_n	PRBSEN_0	RLB_n	LLB_n	E3_n	STS1/$\overline{DS3}$_n	SR/$\overline{DR}$_n
0x07 (ch 0) 0x17 (ch 1) 0x27 (ch 2) 0x37 (ch 3) 0x47 (ch 4) 0x57 (ch 5)	Jitter Attenuator Control (read/write)	Reserved			DFLCK_n	PNTRST_n	JA1_n	JATx/$\overline{Rx}$_n	JA0_n
0x0A (ch 0) 0x1A (ch 1) 0x2A (ch 2) 0x3A (ch 3) 0x4A (ch 4) 0x5A (ch 5)	PRBS Error Count Reg. MSB	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x0B (ch 0) 0x1B (ch 1) 0x2B (ch 2) 0x3B (ch 3) 0x4B (ch 4) 0x5B (ch 5)	PRBS Error Count Reg. LSB	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C (ch 0) 0x1C (ch 1) 0x2C (ch 2) 0x3C (ch 3) 0x4C (ch 4) 0x5C (ch 5)	PRBS Error Count Holding Register								

TABLE 18: REGISTER MAP DESCRIPTION - CHANNEL N

ADDRESS (HEX)	TYPE	REGISTER NAME	BIT#	SYMBOL	DESCRIPTION	DEFAULT VALUE
0x01 (ch 0) 0x11 (ch 1) 0x21 (ch 2) 0x31 (ch 3) 0x41 (ch 4) 0x51 (ch 5)	R/W	Interrupt Enable (source level)	D0	DMOIE_n	If the Driver Monitor (connected to the output of the channel) detects the absence of pulses for 128 consecutive cycles, it will set the interrupt flag if this bit has been set.	0
			D1	RLOSIE_n	This flag will allow a loss of receive signal(for that channel) to send an interrupt to the Host when this bit is set.	0
			D2	RLOLIE_n	This flag will allow a loss of lock condition to send an interrupt to the Host when this bit is set.	0
			D3	FLIE_n	Set this bit to enable the interrupt when the FIFO Limit of the Jitter Attenuator is within 2 bits of overflow/underflow condition. ***NOTE:*** *This bit field is ignored when the Jitter Attenuator is disabled.*	0
			D4	PRBSERIE_n	Set this bit to enable the interrupt when the PRBS error is detected.	0
			D5	PRBSERCNTIE_n	Set this bit to enable the interrupt when the PRBS error count register saturates.	0
			D6-D7		Reserved	
0x02 (ch 0) 0x12 (ch 1) 0x22 (ch 2) 0x32 (ch 3) 0x42 (ch 4) 0x52 (ch 5)	Reset on Read	Interrupt Status (source level)	D0	DMOIS_n	If the Drive monitor circuot detects the absence of pulses for 128 consecutive cycles, t will set this interrupt status flag (if enabled) This bit is set on a change of state of the DMO circuit.	0
			D1	RLOSIS_n	This flag will indicate a change of “loss of Receive signal” to the Host when this bit is set.	0
			D2	RLOLIS_n	This flag will allow a change in the loss of lock condition to send an interrupt to the Host when this bit is enabled.Loss of lock is defined as a difference of greater than 0.5% between the recovered clock and the channel’s reference clock. Any change (return to lock) will trigger the interrupt status flag again.	0
			D3	FLIS_n	This bit will generate an interrupt if the jitter attenuator FIFO reaches (or leaves) a limit condition. This limit condition is defined as the FIFO being within two counts of full or empty.	0
			D4	PRBSERIS_n	This bit is set when the PRBS error occurs.	0
			D5	PRBSERCNTIS_n	This bit is set when the PRBS error count register saturates.	0
			D7-D6		Reserved	

TABLE 18: REGISTER MAP DESCRIPTION - CHANNEL N

ADDRESS (HEX)	TYPE	REGISTER NAME	BIT#	SYMBOL	DESCRIPTION	DEFAULT VALUE
0x03 (ch 0) 0x13 (ch 1) 0x23 (ch 2) 0x33 (ch 3) 0x43 (ch 4) 0x53 (ch 5)	Read Only	Alarm Status	D0	DMO_n	This bit is set when no transitions on the TTIP/ TRING have been detected for 128 ± 32 TxCLK periods.It will be cleared when pulses resume.	0
			D1	RLOS_n	This bit is set every time the receiver declares an LOS condition.It will be cleared when the signal is recognized again.	0
			D2	RLOL_n	This bit is set when the detected clock is greater than 0.5% oof frequency from the reference clock.By definition, the two frequencies are “not in lock” with each other. It will be cleared when they are “in lock” again..	0
			D3	FL_n	This bit is set when the FIFO reaches its limit.The limit is defined to be within two bits of either underflow or overflow.	0
			D4	ALOS_n	This bit is set when the receiver declares that the Analog signal has degraded to the point that the signal has been lost.	0
			D5	DLOS_n	This bit is set when no input signals have been received for 10 to 255 bit times in E3 or 100 to 250 bit times in DS3 or STS-1 modes.This is a complete lack of incoming pulses rather than signal attenuation (ALOS). It should be noted that this time period is built into the Analog detector for E3 mode. Even though DS3/STS-1 mode does not require analog detection level, but it is provided and could help to determine the “quality of the line” for DS/STS-1 applications.	0
			D6	PRBSLS_n	This bit is set when the PRBS detector has been enabled and it is not in sync with the incoming data pattern. Once the sync is achieved, it will be cleared.	0
			D7	Reserved		

TABLE 18: REGISTER MAP DESCRIPTION - CHANNEL N

ADDRESS (HEX)	TYPE	REGISTER NAME	BIT#	SYMBOL	DESCRIPTION	DEFAULT VALUE
0x04 (ch 0) 0x14 (ch 1) 0x24 (ch 2) 0x34 (ch 3) 0x44 (ch 4) 0x54 (ch 5)	R/W	Transmit Control	D0	TxLEV_n	This bit should be set when the transmitter is driving a line greater than 225 feet in the DS3 or STS-1 modes. It is not active in E3 mode.	0
			D1	TxCLKINV_n	Set this bit to sample the data on TPOS/TNEG pins on the rising edge of TxCLK.Default is to sample on the falling edge of TxCLK.	0
			D2	TAOS_n	This bit should be set to transmit a continuous “all ones” data pattern. Timing will come from TxCLK if available otherwise from channel refernce clock.	0
			D3	Reserved		
			D4	INSPRBS_n	This bit causes a single bit error to be inserted in the transmitted PRBS pattern if the PRBS generator/ detector has been enabled.	0
			D5	TxMON_n	When set, this bit enables the DMO circuit to monitor its own channel’s transmit driver. Otherwise, it uses the MTIP/MRING pins to monitor another channel or device.	0
			D7-D6	Reserved		
0x05 (ch 0) 0x15 (ch 1) 0x25 (ch 2) 0x35 (ch 3) 0x45 (ch 4) 0x55 (ch 5)	R/W	Receive Control	D0	REQEN_n	This bit enables the Receiver Equalizer. When set, the equalizer boosts the high frequency components of the signal to make up for cable losses. ***NOTE:*** *See section 5.01 for detailed description.*	0
			D1	RxMON_n	Set this bit to place the Receiver in the monitoring mode. In this mode, it can process signals (at RTIP/ RRING) with 20dB of flat loss. This mode allows the channel to act as monitor of aline without loading the circuit.	0
			D2	LOSMUT_n	When set, the data on RPOS/RNEG is forced to zero when LOS occurs. Thus any residual noise on the line is not output as spurious data. ***NOTE:*** *If this bit has been set, it will remain set evan after the LOS condition is cleared.*	0
			D3	RxCLKINV_n	When this bit is set, RPOS and RNEG will change on the falling edge of RCLK.Default is for the data to change on the rising edge of RCLK and be sampled by the terminal equipment on the falling edge of RCLK.	0
			D4	ALOSDIS_n	This bit is set to disable the ALOS detector. This flag and the DLOSDIS are normally used in diagnostic mode. Normal operation of DS3 and STS-1 would have ALOS disabled.	0
			D5	DLOSDIS_n	This bit disables the digital LOS detector. This would normally be disabled in E3 mode as E3 is a function of the level of the input.	0
			D7-D6	Reserved		

TABLE 18: REGISTER MAP DESCRIPTION - CHANNEL N

ADDRESS (HEX)	TYPE	REGISTER NAME	BIT#	SYMBOL	DESCRIPTION	DEFAULT VALUE
0x06 (ch 0) 0x16 (ch 1) 0x26 (ch 2) 0x36 (ch 3) 0x46 (ch 4) 0x56 (ch 5)	R/W	Block Control	D0	SR/$\overline{DR}$_n	Setting this bit configures the Receiver and Transmitter in Single-Rail (NRZ) mode. ***NOTE:*** *See section 4.0 for detailed description.*	0
			D1	STS-1/$\overline{DS3}$_n	Setting this bit configures the channel into STS-1 mode. ***NOTE:*** *This bit field is ignored if the channel is configured to operate in E3 mode.*	0
			D2	E3_n	Setting this bit configures the channel in E3 mode.	0
			D3	LLB_n	Setting this bit configures the channel in Local Loopback mode.	0
			D4	RLB_n	This bit along with LLB_n determine the diagnostic mode as shown in the table below.	0
			D5	PRBSEN_n	Setting this bit enables the PRBS generator/detector. When in E3 mode, an unframed 2^{23}-1 pattern is used. For DS3 and STS-1, unframed 2^{15}-1 pattern is used. This mode of operation will use TCLK for timing. One should insure that a stable frequency is provided. Looping this signal back to its own receive channel and using RCLK to generate TCLK will cause an unstable condition and should be avoided.	0
			D6	CLKOUTEN_n	Set this bit to enable the CLKOUTs on a per channel basis. The frequency of the output clock is dependent on the configuration of the channels, either E3, DS3 or STS-1.	0
			D7	Reserved		

RLB_n	LLB_n	Loopback Mode
0	0	Normal Operation
0	1	Analog Local
1	0	Remote
1	1	Digital

TABLE 18: REGISTER MAP DESCRIPTION - CHANNEL N

<table>
<tr><th>ADDRESS (HEX)</th><th>TYPE</th><th>REGISTER NAME</th><th>BIT#</th><th>SYMBOL</th><th>DESCRIPTION</th><th>DEFAULT VALUE</th></tr>
<tr><td rowspan="6">0x07 (ch 0)
0x17 (ch 1)
0x27 (ch 2)
0x37 (ch 3)
0x47 (ch 4)
0x57 (ch 5)</td><td rowspan="6">R/W</td><td rowspan="6">Jitter Attenuator</td><td>D0</td><td>JA0_n</td><td>This bit along with JA1_n bit configures the Jitter Attenuator as shown in the table below.

<table><tr><th>JA0_n</th><th>JA1_n</th><th>Mode</th></tr><tr><td>0</td><td>0</td><td>16 bit FIFO</td></tr><tr><td>0</td><td>1</td><td>32 bit FIFO</td></tr><tr><td>1</td><td>0</td><td>Disable Jitter Attenuator</td></tr><tr><td>1</td><td>1</td><td>Disable Jitter Attenuator</td></tr></table></td><td>0</td></tr>
<tr><td>D1</td><td>JATx/$\overline{Rx}$_n</td><td>Setting this bit selects the Jitter Attenuator in the Transmit Path. A “0” selects in the Receive Path.</td><td>0</td></tr>
<tr><td>D2</td><td>JA1_n</td><td>This bit along with the JA0_n configures the Jitter Attenuator as shown in the table.</td><td>0</td></tr>
<tr><td>D3</td><td>PNTRST_n</td><td>Setting this bit resets the FIFO pointers to their initial state and flushes the FIFO. All existing FIFO data is lost.</td><td>0</td></tr>
<tr><td>D4</td><td>DFLCK_n</td><td>Set this bit to “1” to disable fast locking of the PLL. This helps to reduce the time for the PLL to lock to incoming frequency when the Jitter Attenuator switches to narrow band.</td><td>0</td></tr>
<tr><td>D7-D5</td><td colspan="3">Reserved</td></tr>
</table>

8.0 THE SONET/SDH DE-SYNC FUNCTION WITHIN THE LIU

The LIU with D-SYNC is very similar to the non D-SYNC LIU in that they both contain Jitter Attenuator blocks within each channel. They are also pin to pin compatible with each other. However, the Jitter Attenuators within the D-SYNC have some enhancements over and above those within the non D-SYNC device. The Jitter Attenuator blocks will support all of the modes and features that exist in the non D-SYNC device and in addition they also support a SONET/SDH De-Sync Mode.

NOTE: *The "D" suffix within the part number stands for "De-Sync".*

The SONET/SDH De-Sync feature of the Jitter Attenuator blocks permits the user to design a SONET/SDH PTE (Path Terminating Equipment) that will comply with all of the following Intrinsic Jitter and Wander requirements.

- **For SONET Applications**
  - Category I Intrinsic Jitter Requirements per Telcordia GR-253-CORE (for DS3 Applications)
  - ANSI T1.105.03b-1997 - SONET Jitter at Network Interfaces - DS3 Wander Supplement
- **For SDH Applications**
  - Jitter and Wander Generation Requirements per ITU-T G.783 (for DS3 and E3 Applications)

Specifically, if the user designs in the LIU along with a SONET/SDH Mapper IC (which can be realized as either a standard product or as a custom logic solution, in an ASIC or FPGA), then the following can be accomplished.

- The Mapper can receive an STS-N or an STM-M signal (which is carrying asynchronously-mapped DS3 and/or E3 signals) and byte de-interleave this data into N STS-1 or 3*M VC-3 signals
- The Mapper will then terminate these STS-1 or VC-3 signals and will de-map out this DS3 or E3 data from the incoming STS-1 SPEs or VC-3s, and output this DS3 or E3 to the DS3/E3 Facility-side towards the LIU
- This DS3 or E3 signal (as it is output from these Mapper devices) will contain a large amount of intrinsic jitter and wander due to (1) the process of asynchronously mapping a DS3 or E3 signal into a SONET or SDH signal, (2) the occurrence of Pointer Adjustments within the SONET or SDH signal (transporting these DS3 or E3 signals) as it traverses the SONET/SDH network, and (3) clock gapping.
- When the LIU has been configured to operate in the "SONET/SDH De-Sync" Mode, then it will (1) accept this jittery DS3 or E3 clock and data signal from the Mapper device (via the Transmit System-side interface) and (2) through the Jitter Attenuator, the LIU will reduce the Jitter and Wander amplitude within these DS3 or E3 signals such that they (when output onto the line) will comply with the above-mentioned intrinsic jitter and wander specifications.

8.1 BACKGROUND AND DETAILED INFORMATION - SONET DE-SYNC APPLICATIONS

This section provides an in-depth discussion on the mechanisms that will cause Jitter and Wander within a DS3 or E3 signal that is being transported across a SONET or SDH Network. A lot of this material is introductory, and can be skipped by the engineer that is already experienced in SONET/SDH designs.

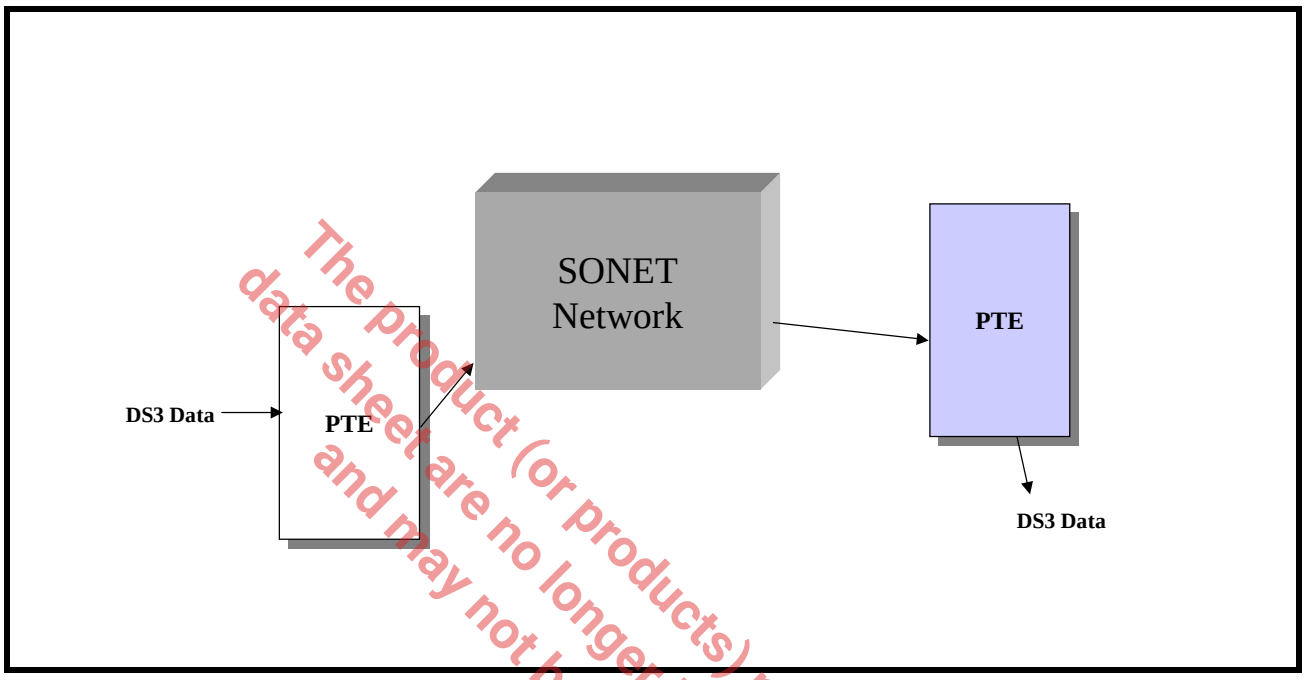
In the wide-area network (WAN) in North America it is often necessary to transport a DS3 signal over a long distance (perhaps over a thousand miles) in order to support a particular service. Now rather than realizing this transport of DS3 data, by using over a thousand miles of coaxial cable (interspaced by a large number of DS3 repeaters) a common thing to do is to route this DS3 signal to a piece of equipment (such as a Terminal MUX, which in the "SONET Community" is known as a PTE or Path Terminating Equipment). This Terminal MUX will asynchronously map the DS3 signal into a SONET signal. At this point, the SONET network will now transport this asynchronously mapped DS3 signal from one PTE to another PTE (which is located at the other end of the SONET network). Once this SONET signal arrives at the remote PTE, this DS3 signal will then be extracted from the SONET signal, and will be output to some other DS3 Terminal Equipment for further processing.

Similar things are done outside of North America. In this case, this DS3 or E3 signal is routed to a PTE, where it is asynchronously mapped into an SDH signal. This asynchronously mapped DS3 or E3 signal is then transported across the SDH network (from one PTE to the PTE at the other end of the SDH network). Once

this SDH signal arrives at the remote PTE, this DS3 or E3 signal will then be extracted from the SDH signal, and will be output to some other DS3/E3 Terminal Equipment for further processing.

Figure 39 presents an illustration of this approach to transporting DS3 data over a SONET Network

FIGURE 39. A SIMPLE ILLUSTRATION OF A DS3 SIGNAL BEING MAPPED INTO AND TRANSPORTED OVER THE SONET NETWORK



As mentioned above a DS3 or E3 signal will be asynchronously mapped into a SONET or SDH signal and then transported over the SONET or SDH network. At the remote PTE this DS3 or E3 signal will be extracted (or de-mapped) from this SONET or SDH signal, where it will then be routed to DS3 or E3 terminal equipment for further processing.

In order to insure that this "de-mapped" DS3 or E3 signal can be routed to any industry-standard DS3 or E3 terminal equipment, without any complications or adverse effect on the network, the Telcordia and ITU-T standard committees have specified some limits on both the Intrinsic Jitter and Wander that may exist within these DS3 or E3 signals as they are de-mapped from SONET/SDH. As a consequence, all PTEs that maps and de-mapped DS3/E3 signals into/from SONET/SDH must be designed such that the DS3 or E3 data that is de-mapped from SONET/SDH by these PTEs must meet these Intrinsic Jitter and Wander requirements.

As mentioned above, the LIU can assist the System Designer (of SONET/SDH PTE) by ensuring that their design will meet these Intrinsic Jitter and Wander requirements.

This section of the data sheet will present the following information to the user.

- Some background information on Mapping DS3/E3 signals into SONET/SDH and de-mapping DS3/E3 signals from SONET/SDH.
- A brief discussion on the causes of jitter and wander within a DS3 or E3 signal that mapped into a SONET/SDH signal, and is transported across the SONET/SDH Network.
- A brief review of these Intrinsic Jitter and Wander requirements in both SONET and SDH applications.
- A brief review on the Intrinsic Jitter and Wander measurement results (of a de-mapped DS3 or E3 signal) whenever the LIU device is used in a system design.
- A detailed discussion on how to design with and configure the LIU device such that the end-system will meet these Intrinsic Jitter and Wander requirements.

In a SONET system, the relevant specification requirements for Intrinsic Jitter and Wander (within a DS3 signal that is mapped into and then de-mapped from SONET) are listed below.

- Telcordia GR-253-CORE Category I Intrinsic Jitter Requirements for DS3 Applications (Section 5.6), and
- ANSI T1.105.03b-1997 - SONET Jitter at Network Interfaces - DS3 Wander Supplement

In general, there are three (3) sources of Jitter and Wander within an asynchronously-mapped DS3 signal that the system designer must be aware of. These sources are listed below.

- Mapping/De-Mapping Jitter
- Pointer Adjustments
- Clock Gapping

Each of these sources of jitter/wander will be defined and discussed in considerable detail within this Section. In order to accomplish all of this, this particular section will discuss all of the following topics in details.

- How DS3 data is mapped into SONET, and how this mapping operation contributes to Jitter and Wander within this "eventually de-mapped" DS3 signal.
- How this asynchronously-mapped DS3 data is transported throughout the SONET Network, and how occurrences on the SONET network (such as pointer adjustments) will further contributes to Jitter and Wander within the "eventually de-mapped" DS3 signal.
- A review of the Category I Intrinsic Jitter Requirements (per Telcordia GR-253-CORE) for DS3 applications
- A review of the DS3 Wander requirements per ANSI T1.105.03b-1997
- A review of the Intrinsic Jitter and Wander Capabilities of the LIU in a typical system application
- An in-depth discussion on how to design with and configure the LIU to permit the system to the meet the above-mentioned Intrinsic Jitter and Wander requirements

NOTE: *An in-depth discussion on SDH De-Sync Applications will be presented in the next revision of this data sheet.*

8.2 MAPPING/DE-MAPPING JITTER/WANDER

Mapping/De-Mapping Jitter (or Wander) is defined as that intrinsic jitter (or wander) that is induced into a DS3 signal by the "Asynchronous Mapping" process. This section will discuss all of the following aspects of Mapping/De-Mapping Jitter.

- How DS3 data is mapped into an STS-1 SPE
- How frequency offsets within either the DS3 signal (being mapped into SONET) or within the STS-1 signal itself contributes to intrinsic jitter/wander within the DS3 signal (being transported via the SONET network).

8.2.1 HOW DS3 DATA IS MAPPED INTO SONET

Whenever a DS3 signal is asynchronously mapped into SONET, this mapping is typically accomplished by a PTE accepting DS3 data (from some remote terminal) and then loading this data into certain bit-fields within a given STS-1 SPE (or Synchronous Payload Envelope). At this point, this DS3 signal has now been asynchronously mapped into an STS-1 signal. In most applications, the SONET Network will then take this particular STS-1 signal and will map it into "higher-speed" SONET signals (e.g., STS-3, STS-12, STS-48, etc.) and will then transport this asynchronously mapped DS3 signal across the SONET network, in this manner. As this "asynchronously-mapped" DS3 signal approaches its "destination" PTE, this STS-1 signal will eventually be de-mapped from this STS-N signal. Finally, once this STS-1 signal reaches the "destination" PTE, then this asynchronously-mapped DS3 signal will be extracted from this STS-1 signal.

8.2.1.1 A Brief Description of an STS-1 Frame

In order to be able to describe how a DS3 signal is asynchronously mapped into an STS-1 SPE, it is important to define and understand all of the following.

- The STS-1 frame structure
- The STS-1 SPE (Synchronous Payload Envelope)

- Telcordia GR-253-CORE's recommendation on mapping DS3 data into an STS-1 SPE

An STS-1 frame is a data-structure that consists of 810 bytes (or 6480 bits). A given STS-1 frame can be viewed as being a 9 row by 90 byte column array (making up the 810 bytes). The frame-repetition rate (for an STS-1 frame) is 8000 frames/second. Therefore, the bit-rate for an STS-1 signal is (6480 bits/frame * 8000 frames/sec =) 51.84Mbps.

A simple illustration of this SONET STS-1 frame is presented below in Figure 40.

FIGURE 40. A SIMPLE ILLUSTRATION OF THE SONET STS-1 FRAME

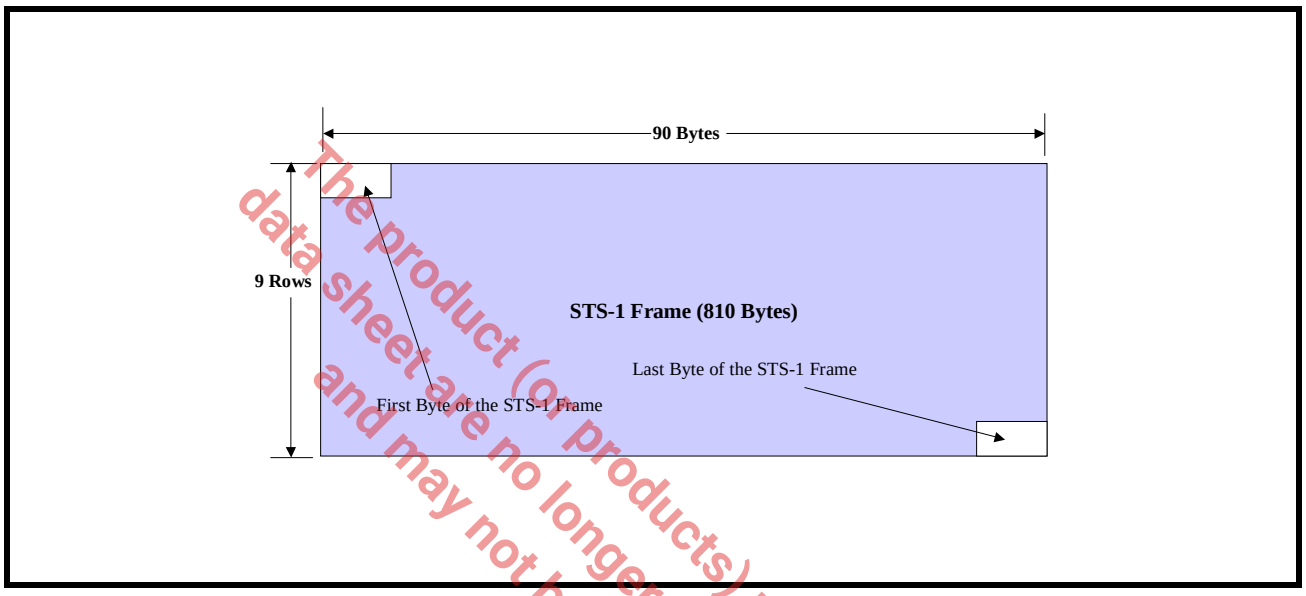


Figure 40 indicates that the very first byte of a given STS-1 frame (to be transmitted or received) is located in the extreme upper left hand corner of the 90 column by 9 row array, and that the very last byte of a given STS-1 frame is located in the extreme lower right-hand corner of the frame structure. Whenever a Network Element transmits a SONET STS-1 frame, it starts by transmitting all of the data, residing within the top row of the STS-1 frame structure (beginning with the left-most byte, and then transmitting the very next byte, to the right). After the Network Equipment has completed its transmission of the top or first row, it will then proceed to transmit the second row of data (again starting with the left-most byte, first). Once the Network Equipment has transmitted the last byte of a given STS-1 frame, it will proceed to start transmitting the very next STS-1 frame.

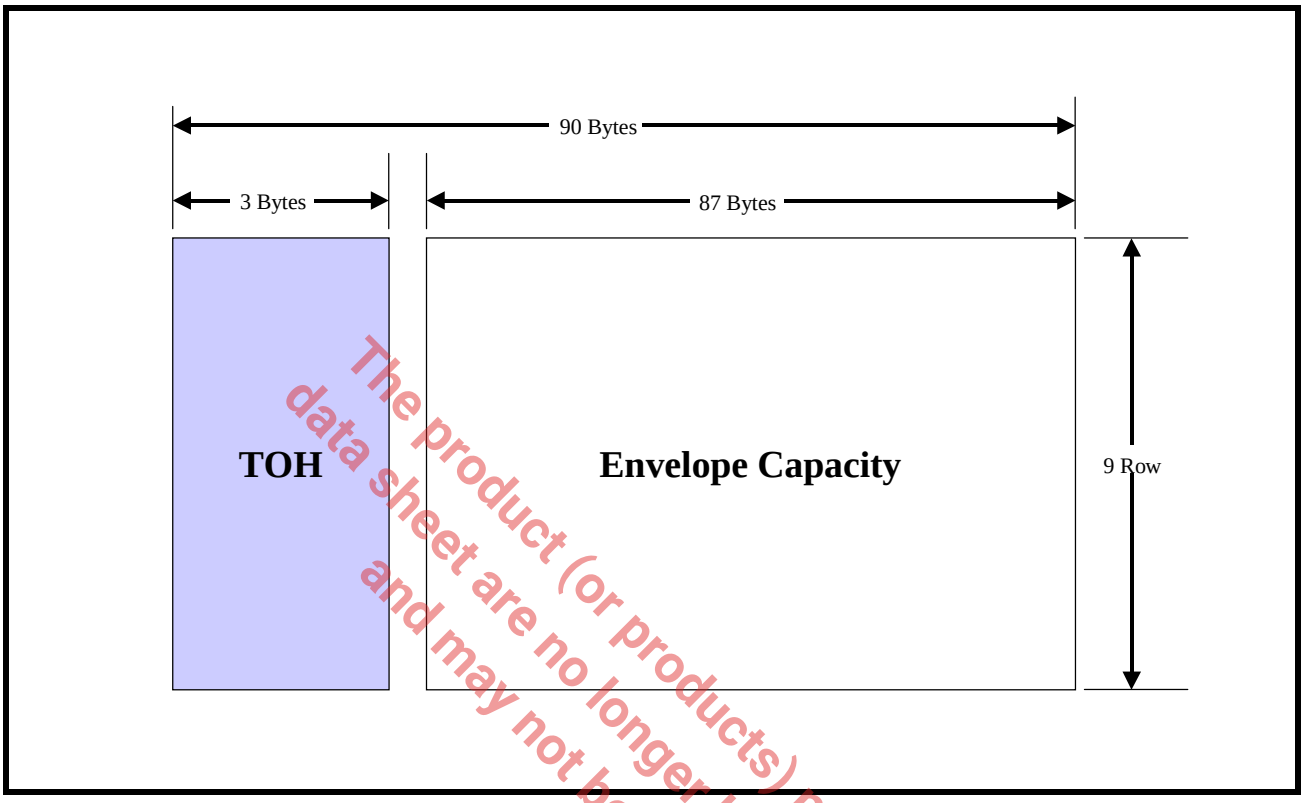
The illustration of the STS-1 frame (in Figure 40) is very simplistic, for multiple reasons. One major reason is that the STS-1 frame consists of numerous types of bytes. For the sake of discussion within this data sheet, the STS-1 frame will be described as consisting of the following types (or groups) of bytes.

- The Transport Overheads (or TOH) Bytes
- The Envelope Capacity Bytes

8.2.1.1.1 The Transport Overhead (TOH) Bytes

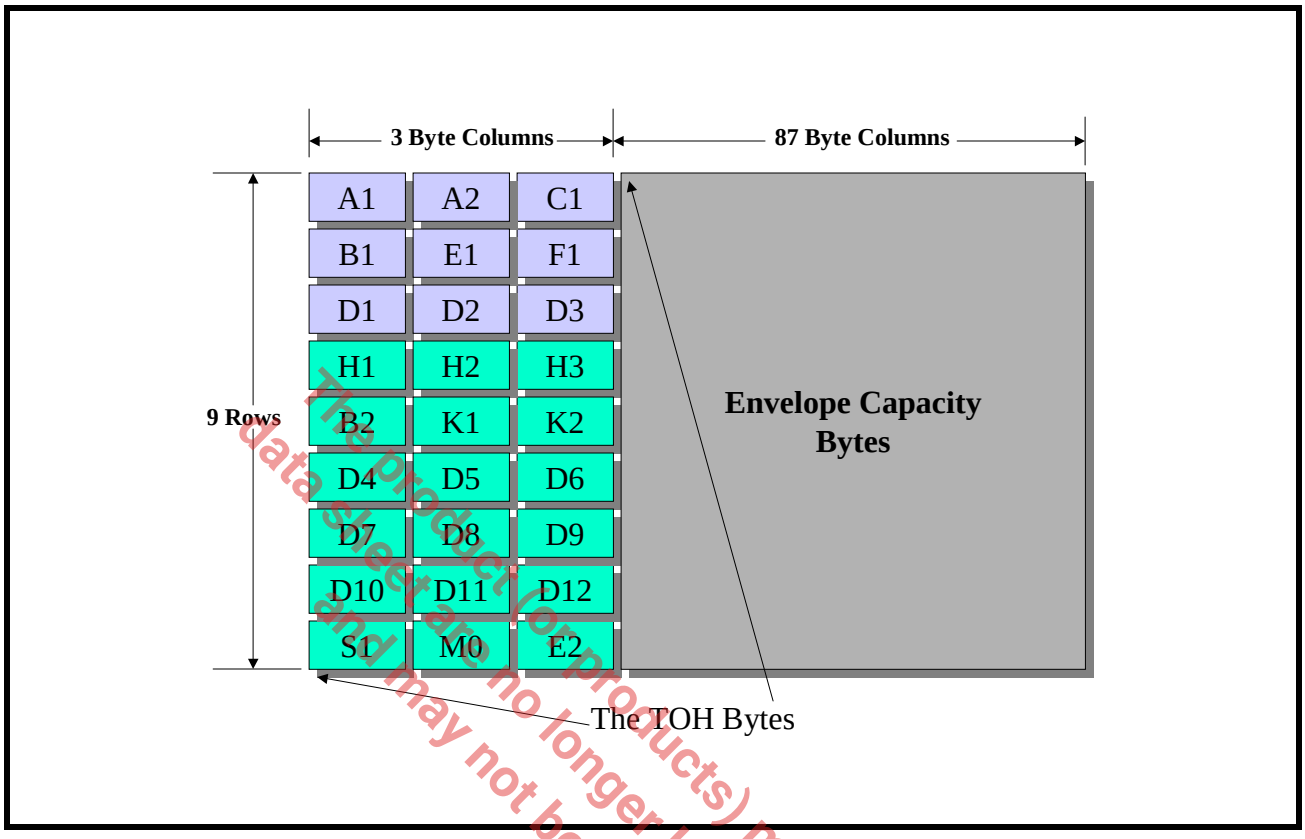
The Transport Overhead or TOH bytes occupy the very first three (3) byte columns within each STS-1 frame. Figure 41 presents another simple illustration of an STS-1 frame structure. However, in this case, both the TOH and the Envelope Capacity bytes are designated in this Figure.

FIGURE 41. A SIMPLE ILLUSTRATION OF THE STS-1 FRAME STRUCTURE WITH THE TOH AND THE ENVELOPE CAPACITY BYTES DESIGNATED



Since the TOH bytes occupy the first three byte columns of each STS-1 frame, and since each STS-1 frame consists of nine (9) rows, then we can state that the TOH (within each STS-1 frame) consists of 3 byte columns x 9 rows = 27 bytes. The byte format of the TOH is presented below in Figure 42.

FIGURE 42. THE BYTE-FORMAT OF THE TOH WITHIN AN STS-1 FRAME



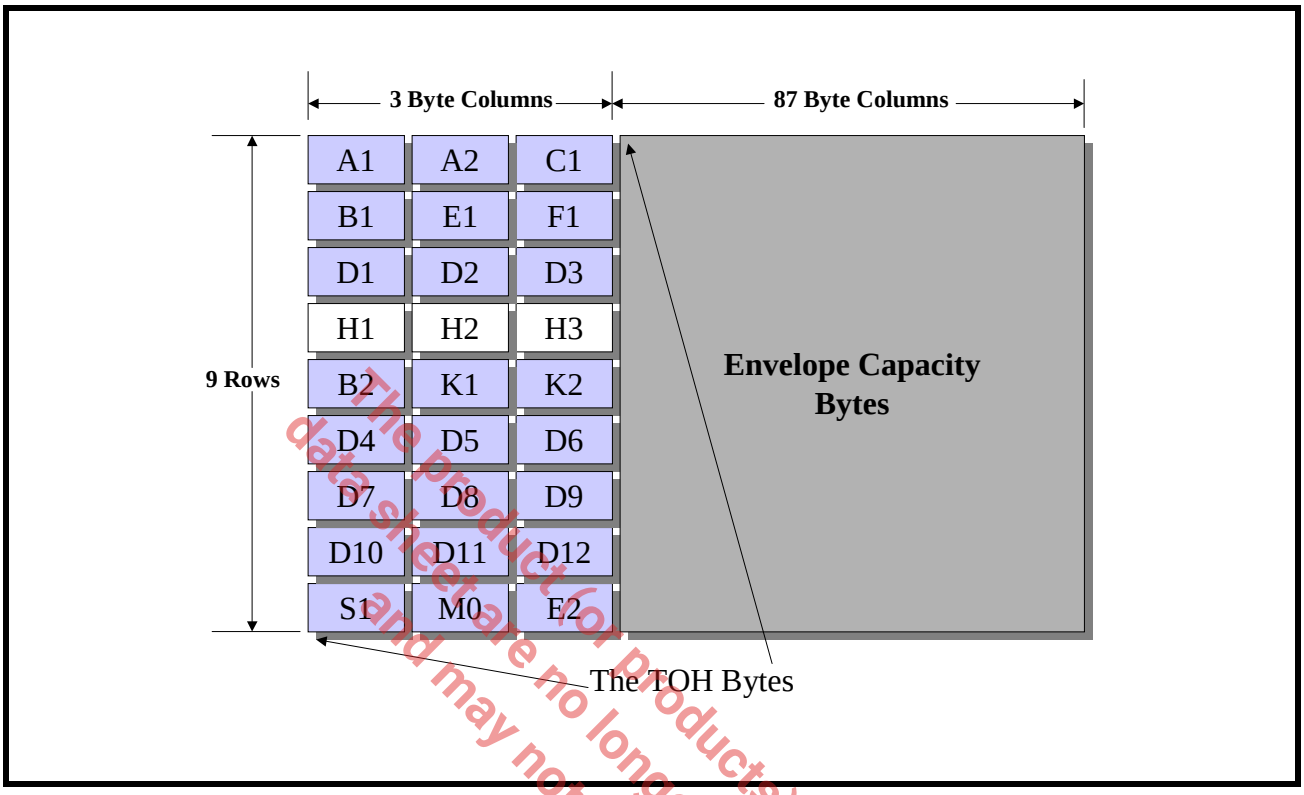
In general, the role/purpose of the TOH bytes is to fulfill the following functions.

- To support STS-1 Frame Synchronization
- To support Error Detection within the STS-1 frame
- To support the transmission of various alarm conditions such as RDI-L (Line - Remote Defect Indicator) and REI-L (Line - Remote Error Indicator)
- To support the Transmission and Reception of "Section Trace" Messages
- To support the Transmission and Reception of OAM&P Messages via the DCC Bytes (Data Communication Channel bytes - D1 through D12 byte)

The roles of most of the TOH bytes is beyond the scope of this Data Sheet and will not be discussed any further. However, there are a three TOH bytes that are important from the stand-point of this data sheet, and will discussed in considerable detail throughout this document. These are the H1 and H2 (e.g., the SPE Pointer) bytes and the H3 (e.g., the Pointer Action) byte.

Figure 43 presents an illustration of the Byte-Format of the TOH within an STS-1 Frame, with the H1, H2 and H3 bytes highlighted.

FIGURE 43. THE BYTE-FORMAT OF THE TOH WITHIN AN STS-1 FRAME



Although the role of the H1, H2 and H3 bytes will be discussed in much greater detail in “Section 8.3, Jitter/ Wander due to Pointer Adjustments” on page 70. For now, we will simply state that the role of these bytes is two-fold.

- To permit a given PTE (Path Terminating Equipment) that is receiving an STS-1 data to be able to locate the STS-1 SPE (Synchronous Payload Envelope) within the Envelope Capacity of this incoming STS-1 data stream and,
- To inform a given PTE whenever Pointer Adjustment and NDF (New Data Flag) events occur within the incoming STS-1 data-stream.

8.2.1.1.2 The Envelope Capacity Bytes within an STS-1 Frame

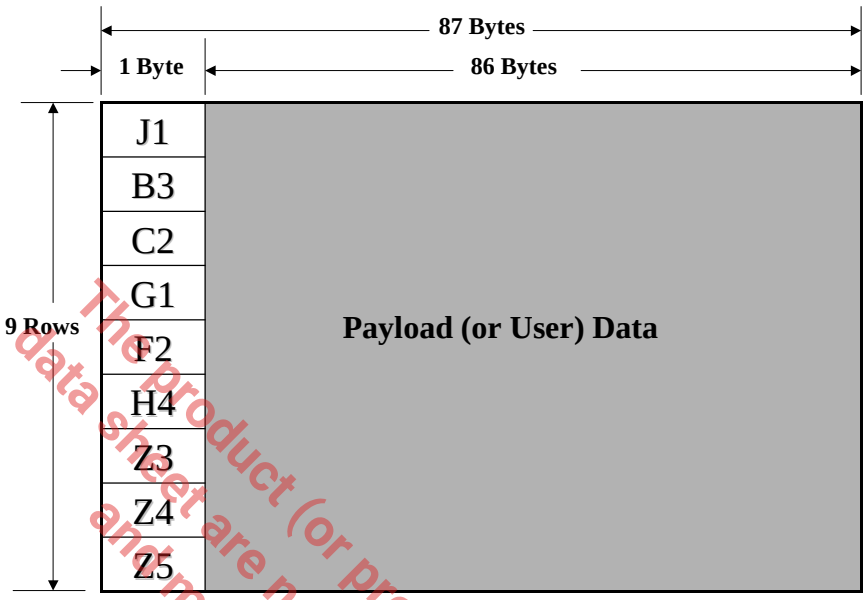
In general, the Envelope Capacity Bytes are any bytes (within an STS-1 frame) that exist outside of the TOH bytes. In short, the Envelope Capacity contains the STS-1 SPE (Synchronous Payload Envelope). In fact, every single byte that exists within the Envelope Capacity also exists within the STS-1 SPE. The only difference that exists between the "Envelope Capacity" as defined in Figure 42 and Figure 43 above and the STS-1 SPE is that the Envelope Capacity is aligned with the STS-1 framing boundaries and the TOH bytes; whereas the STS-1 SPE is NOT aligned with the STS-1 framing boundaries, nor the TOH bytes.

The STS-1 SPE is an "87 byte column x 9 row" data-structure (which is the exact same size as is the Envelope Capacity) that is permitted to "float" within the "Envelope Capacity". As a consequence, the STS-1 SPE (within an STS-1 data-stream) will typically straddle across an STS-1 frame boundary.

8.2.1.1.3 The Byte Structure of the STS-1 SPE

As mentioned above, the STS-1 SPE is an 87 byte column x 9 row structure. The very first column within the STS-1 SPE consists of some overhead bytes which are known as the "Path Overhead" (or POH) bytes. The remaining portions of the STS-1 SPE is available for "user" data. The Byte Structure of the STS-1 SPE is presented below in Figure 44.

FIGURE 44. ILLUSTRATION OF THE BYTE STRUCTURE OF THE STS-1 SPE



In general, the role/purpose of the POH bytes is to fulfill the following functions.

- To support error detection within the STS-1 SPE
- To support the transmission of various alarm conditions such as RDI-P (Path - Remote Defect Indicator) and REI-P (Path - Remote Error Indicator)
- To support the transmission and reception of "Path Trace" Messages

The role of the POH bytes is beyond the scope of this data sheet and will not be discussed any further.

8.2.1.2 Mapping DS3 data into an STS-1 SPE

Now that we have defined the STS-1 SPE, we can now describe how a DS3 signal is mapped into an STS-1 SPE. As mentioned above, the STS-1 SPE is basically an 87 byte column x 9 row structure of data. The very first byte column (e.g., in all 9 bytes) consists of the POH (Path Overhead) bytes. All of the remaining bytes within the STS-1 SPE is simply referred to as "user" or "payload" data because this is the portion of the STS-1 signal that is used to transport "user data" from one end of the SONET network to the other. Telcordia GR-253-CORE specifies the approach that one must use to asynchronously map DS3 data into an STS-1 SPE. In short, this approach is presented below in Figure 45.

FIGURE 45. AN ILLUSTRATION OF TELCORDIA GR-253-CORE'S RECOMMENDATION ON HOW MAP DS3 DATA INTO AN STS-1 SPE

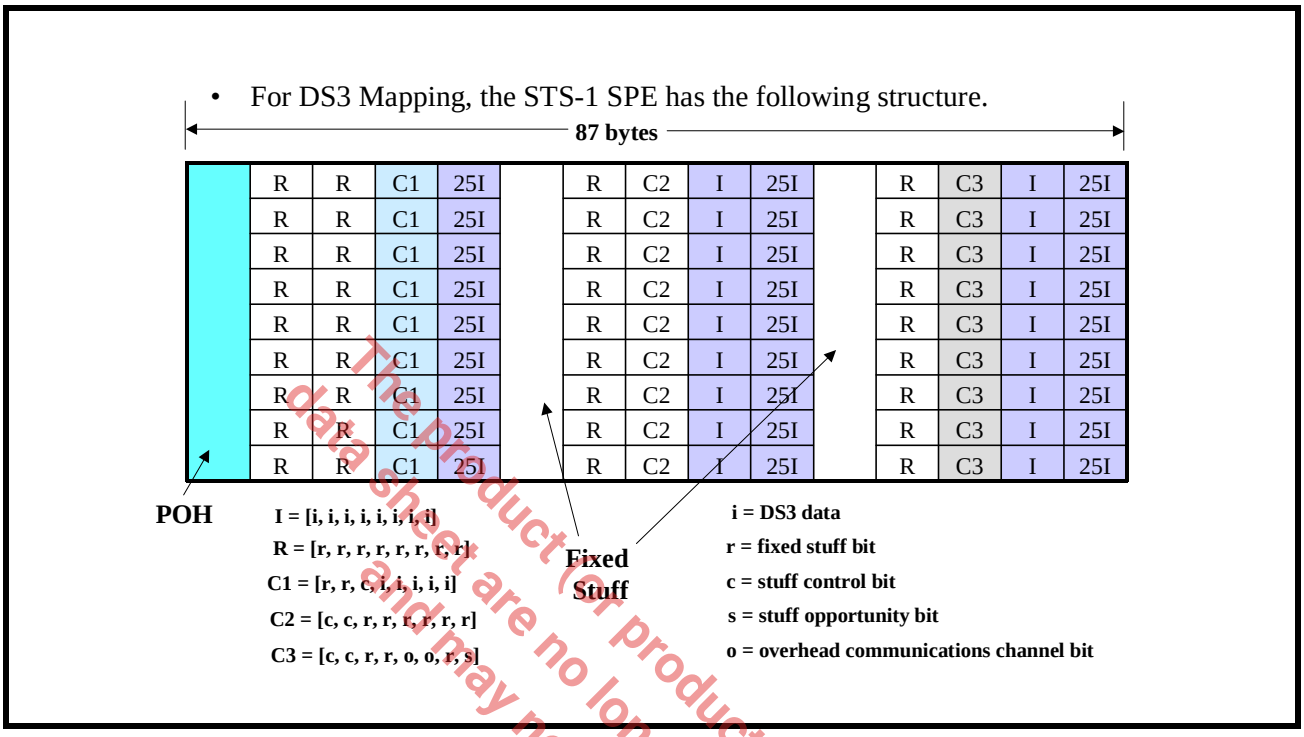


Figure 45 was copied directly out of Telcordia GR-253-CORE. However, this figure can be simplified and redrawn as depicted below in Figure 46.

FIGURE 46. A SIMPLIFIED "BIT-ORIENTED" VERSION OF TELCORDIA GR-253-CORE'S RECOMMENDATION ON HOW TO MAP DS3 DATA INTO AN STS-1 SPE

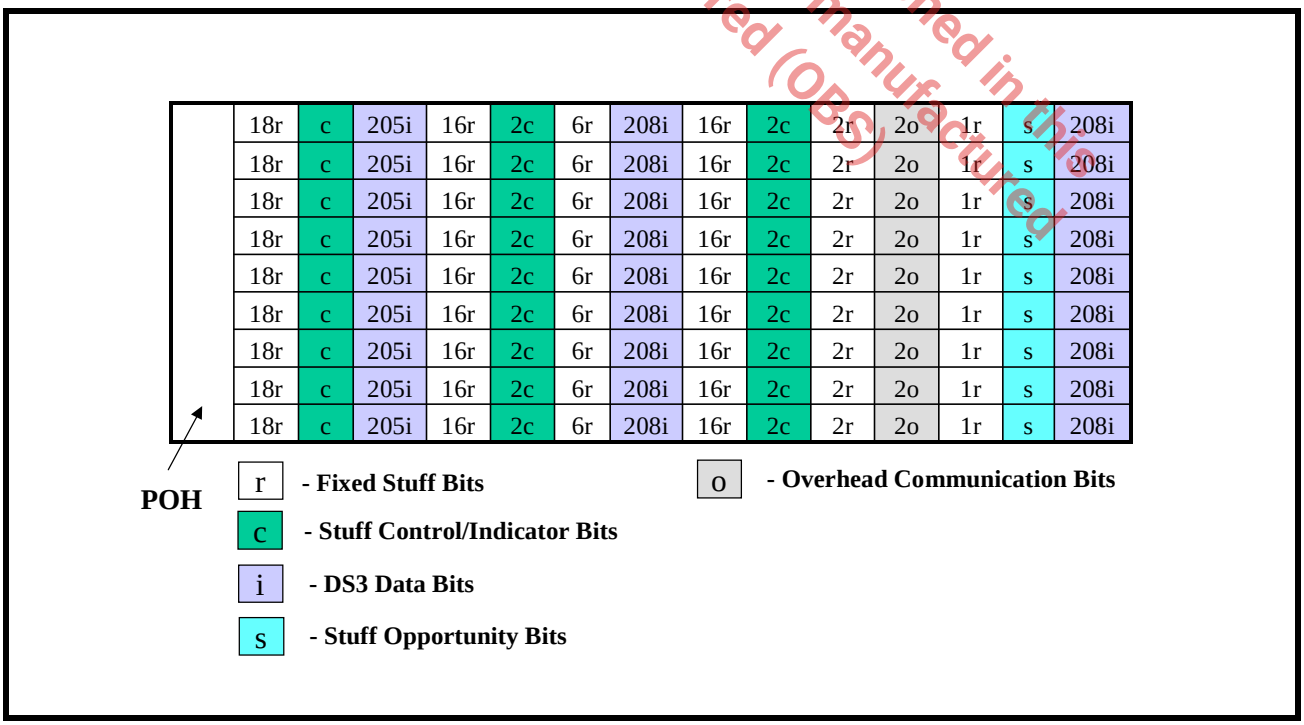


Figure 46 presents an alternative illustration of Telcordia GR-253-CORE's recommendation on how to asynchronously map DS3 data into an STS-1 SPE. In this case, the STS-1 SPE bit-format is expressed purely in the form of "bit-types" and "numbers of bits within each of these types of bits". If one studies this figure closely he/she will notice that this is the same "87 byte column x 9 row" structure that we have been talking about when defining the STS-1 SPE. However, in this figure, the "user-data" field is now defined and is said to consist of five (5) different types of bits. Each of these bit-types play a role when asynchronously mapping a DS3 signal into an STS-1 SPE. Each of these types of bits are listed and described below.

Fixed Stuff Bits

Fixed Stuff bits are simply "space-filler" bits that simply occupy space within the STS-1 SPE. These bit-fields have no functional role other than "space occupation". Telcordia GR-253-CORE does not define any particular value that these bits should be set to. Each of the 9 rows, within the STS-1 SPE will contain 59 of these "fixed stuff" bits.

DS3 Data Bits

The DS3 Data-Bits are (as its name implies) used to transport the DS3 data-bits within the STS-1 SPE. If the STS-1 SPE is transporting a framed DS3 data-stream, then these DS3 Data bits will carry both the "DS3 payload data" and the "DS3 overhead bits". Each of the 9 rows, within the STS-1 SPE will contain 621 of these "DS3 Data bits". This means that each STS-1 SPE contains 5,589 of these DS3 Data bit-fields.

Stuff Opportunity Bits

The "Stuff" Opportunity bits will function as either a "stuff" (or junk) bit, or it will carry a DS3 data-bit. The decision as to whether to have a "Stuff Opportunity" bit transport a "DS3 data-bit" or a "stuff" bit depends upon the "timing differences" between the DS3 data that is being mapped into the STS-1 SPE and the timing source that is driving the STS-1 circuitry within the PTE.

As will be described later on, these "Stuff Opportunity" Bits play a very important role in "frequency-justifying" the DS3 data that is being mapped into the STS-1 SPE. These "Stuff Opportunity" bits also play a critical role in inducing Intrinsic Jitter and Wander within the DS3 signal (as it is de-mapped by the remote PTE).

Each of the 9 rows, within the STS-1 SPE consists of one (1) Stuff Opportunity bit. Hence, there are a total of nine "Stuff Opportunity" bits within each STS-1 SPE.

Stuff Control/Indicator Bits

Each of the nine (9) rows within the STS-1 SPE contains five (5) Stuff Control/Indicator bits. The purpose of these "Stuff Control/Indicator" bits is to indicate (to the de-mapping PTE) whether the "Stuff Opportunity" bits (that resides in the same row) is a "Stuff" bit or is carrying a DS3 data bit.

If all five of these "Stuff Control/Indicator" bits, within a given row are set to "0", then this means that the corresponding "Stuff Opportunity" bit (e.g., the "Stuff Opportunity" bit within the same row) is carrying a DS3 data bit.

Conversely, if all five of these "Stuff Control/Indicator" bits, within a given row are set to "1" then this means that the corresponding "Stuff Opportunity" bit is carrying a "stuff" bit.

Overhead Communication Bits

Telcordia GR-253-CORE permits the user to use these two bits (for each row) as some sort of "Communications" bit. Some Mapper devices, such as the XRT94L43 12-Channel DS3/E3/STS-1 to STS-12/STM-1 Mapper and the XRT94L33 3-Channel DS3/E3/STS-1 to STS-3/STM-1 Mapper IC (both from Exar Corporation) do permit the user to have access to these bit-fields.

However, in general, these particular bits can also be thought of as "Fixed Stuff" bits, that mostly have a "space occupation" function.

8.2.2 DS3 Frequency Offsets and the Use of the "Stuff Opportunity" Bits

In order to fully convey the role that the "stuff-opportunity" bits play, when mapping DS3 data into SONET, we will present a detailed discussion of each of the following "Mapping DS3 into STS-1" scenarios.

- The Ideal Case (e.g., with no frequency offsets)
- The 44.736Mbps + 1 ppm Case

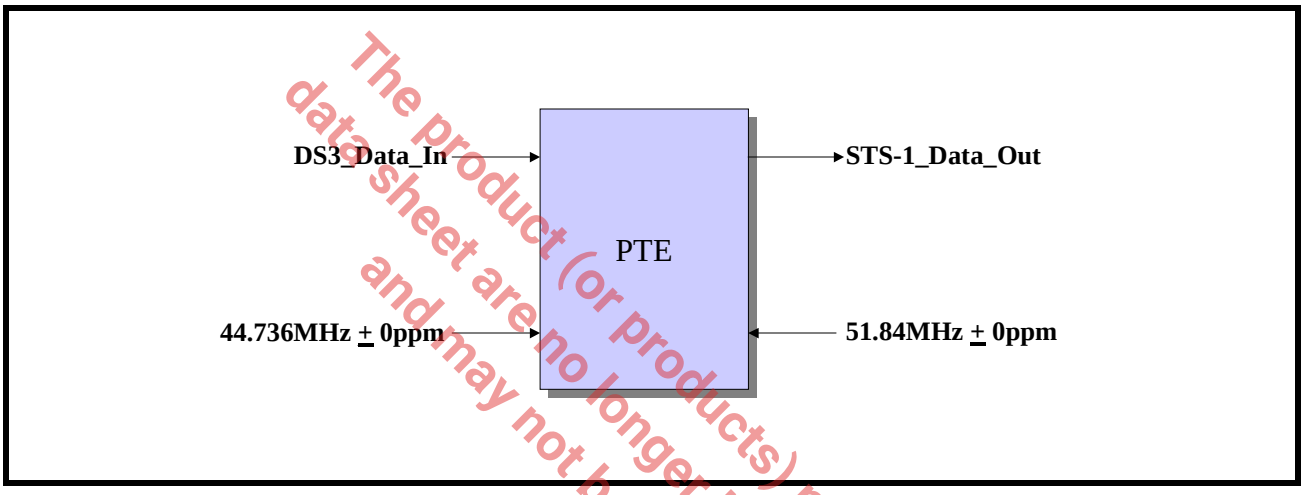
- The 44.736MHz - 1ppm Case

Throughout each of these cases, we will discuss how the resulting "bit-stuffing" (that was done when mapping the DS3 signal into SONET) affects the amount of intrinsic jitter and wander that will be present in the DS3 signal, once it is ultimately de-mapped from SONET.

8.2.2.1 The Ideal Case for Mapping DS3 data into an STS-1 Signal (e.g., with no Frequency Offsets)

Let us assume that we are mapping a DS3 signal, which has a bit rate of exactly 44.736Mbps (with no frequency offset) into SONET. Further, let us assume that the SONET circuitry within the PTE is clocked at exactly 51.84MHz (also with no frequency offset), as depicted below.

FIGURE 47. A SIMPLE ILLUSTRATION OF A DS3 DATA-STREAM BEING MAPPED INTO AN STS-1 SPE, VIA A PTE



Given the above-mentioned assumptions, we can state the following:

- The DS3 data-stream has a bit-rate of exactly 44.736Mbps
- The PTE will create 8000 STS-1 SPE's per second
- In order to properly map a DS3 data-stream into an STS-1 data-stream, then each STS-1 SPE must carry (44.736Mbps/8000 =) 5592 DS3 data bits.

Is there a Problem?

According to Figure 46, each STS-1 SPE only contains 5589 bits that are specifically designated for "DS3 data bits". In this case, each STS-1 SPE appears to be three bits "short".

No there is a Simple Solution

No, earlier we mentioned that each STS-1 SPE consists of nine (9) "Stuff Opportunity" bits. Therefore, these three additional bits (for DS3 data) are obtained by using three of these "Stuff Opportunity" bits. As a consequence, three (3) of these nine (9) "Stuff Opportunity" bits, within each STS-1 SPE, will carry DS3 data-bits. The remaining six (6) "Stuff Opportunity" bits will typically function as "stuff" bits.

In summary, for the "Ideal Case"; where there is no frequency offset between the DS3 and the STS-1 bit-rates, once this DS3 data-stream has been mapped into the STS-1 data-stream, then each and every STS-1 SPE will have the following "Stuff Opportunity" bit utilization.

3 "Stuff Opportunity" bits will carry DS3 data bits.

6 "Stuff Opportunity" bits will function as "stuff" bits

In this case, this DS3 signal (which has now been mapped into STS-1) will be transported across the SONET network. As this STS-1 signal arrives at the "Destination PTE", this PTE will extract (or de-map) this DS3 data-stream from each incoming STS-1 SPE. Now since each and every STS-1 SPE contains exactly 5592 DS3 data bits; then the bit rate of this DS3 signal will be exactly 44.736Mbps (such as it was when it was mapped into SONET, at the "Source" PTE).

As a consequence, no "Mapping/De-Mapping" Jitter or Wander is induced in the "Ideal Case".

8.2.2.2 The 44.736Mbps + 1ppm Case

The "above example" was a very ideal case. In reality, there are going to be frequency offsets in both the DS3 and STS-1 signals. For instance Bellcore GR-499-CORE mandates that a DS3 signal have a bit rate of 44.736Mbps ± 20ppm. Hence, the bit-rate of a "Bellcore" compliant DS3 signal can vary from the exact correct frequency for DS3 by as much of 20ppm in either direction. Similarly, many SONET applications mandate that SONET equipment use at least a "Stratum 3" level clock as its timing source. This requirement mandates that an STS-1 signal must have a bit rate that is in the range of 51.84 ± 4.6ppm. To make matters worse, there are also provisions for SONET equipment to use (what is referred to as) a "SONET Minimum Clock" (SMC) as its timing source. In this case, an STS-1 signal can have a bit-rate in the range of 51.84Mbps ± 20ppm.

In order to convey the impact that frequency offsets (in either the DS3 or STS-1 signal) will impose on the bit-stuffing behavior, and the resulting bit-rate, intrinsic jitter and wander within the DS3 signal that is being transported across the SONET network; let us assume that a DS3 signal, with a bit-rate of 44.736Mbps + 1ppm is being mapped into an STS-1 signal with a bit-rate of 51.84Mbps + 0ppm. In this case, the following things will occur.

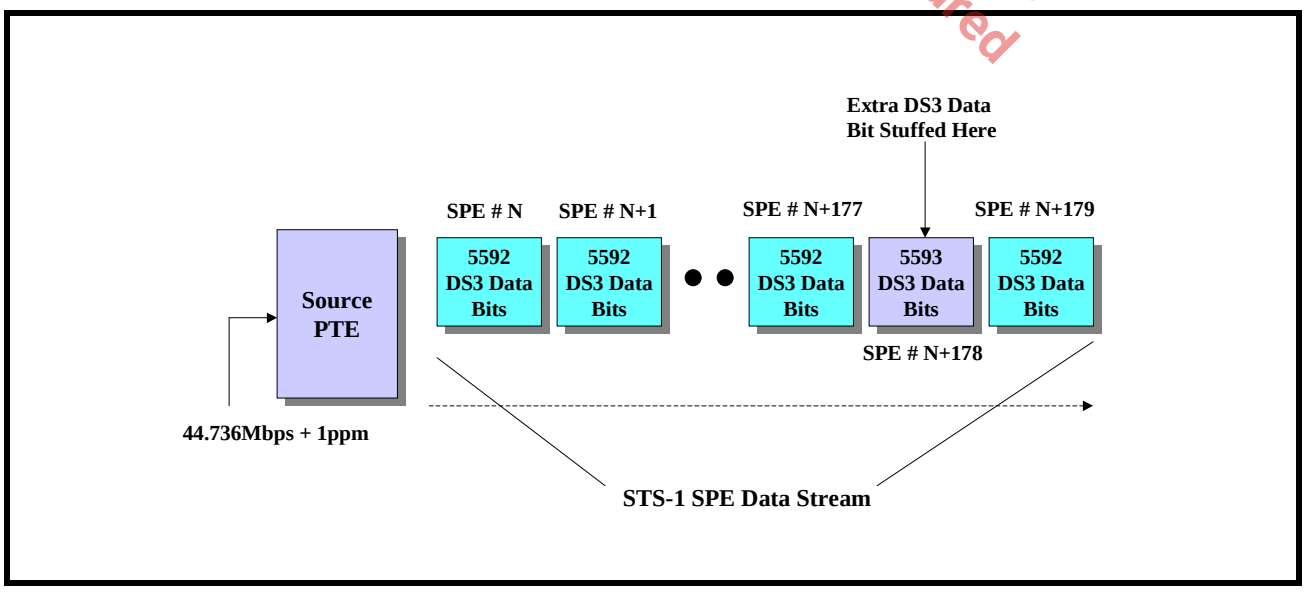
- In general, most of the STS-1 SPE's will each transport 5592 DS3 data bits.
- However, within a "one-second" period, a DS3 signal that has a bit-rate of 44.736Mbps + 1 ppm will deliver approximately 44.7 additional bits (over and above that of a DS3 signal with a bit-rate of 44.736Mbps + 0 ppm). This means that this particular signal will need to "negative-stuff" or map in an additional DS3 data bit every (1/44.736 =) 22.35ms. In other words, this additional DS3 data bit will need to be mapped into about one in every (22.35ms · 8000 =) 178.8 STS-1 SPEs in order to avoid dropping any DS3 data-bits.

What does this mean at the "Source" PTE?

All of this means that as the "Source" PTE maps this DS3 signal, with a data rate of 44.736Mbps + 1ppm into an STS-1 signal, most of the resulting "outbound" STS-1 SPEs will transport 5592 DS3 data bits (e.g., 3 Stuff Opportunity bits will be carrying DS3 data bits, the remaining 6 Stuff Opportunity bits are "stuff" bits, as in the "Ideal" case). However, in approximately one out of 178.8 "outbound" STS-1 SPEs, there will be a need to insert an additional DS3 data bit within this STS-1 SPE. Whenever this occurs, then (for these particular STS-1 SPEs) the SPE will be carrying 5593 DS3 data bits (e.g., 4 Stuff Opportunity bits will be carrying DS3 data bits, the remaining 5 Stuff Opportunity bits are "stuff" bits).

Figure 48 presents an illustration of the STS-1 SPE traffic that will be generated by the "Source" PTE, during this condition.

FIGURE 48. AN ILLUSTRATION OF THE STS-1 SPE TRAFFIC THAT WILL BE GENERATED BY THE "SOURCE" PTE, WHEN MAPPING IN A DS3 SIGNAL THAT HAS A BIT RATE OF 44.736MBPS + 1PPM, INTO AN STS-1 SIGNAL



What does this mean at the "Destination" PTE?

In this case, this DS3 signal (which has now been mapped into an STS-1 data-stream) will be transported across the SONET network. As this STS-1 signal arrives at the "Destination" PTE, this PTE will extract (or de-map) this DS3 data from each incoming STS-1 SPE. Now, in this case most (e.g., 177/178.8) of the incoming STS-1 SPEs will contain 5592 DS3 data-bits. Therefore, the nominal data rate of the DS3 signal being de-mapped from SONET will be 44.736Mbps. However, in approximately 1 out of every 178 incoming STS-1 SPEs, the SPE will carry 5593 DS3 data-bits. This means that (during these times) the data rate of the de-mapped DS3 signal will have an instantaneous frequency that is greater than 44.736Mbps. These "excursion" of the de-mapped DS3 data-rate, from the nominal DS3 frequency can be viewed as occurrences of "mapping/de-mapping" jitter. Since each of these "bit-stuffing" events involve the insertion of one DS3 data bit, we can say that the amplitude of this "mapping/de-mapping" jitter is approximately 1UI-pp. From this point on, we will be referring to this type of jitter (e.g., that which is induced by the mapping and de-mapping process) as "de-mapping" jitter.

Since this occurrence of "de-mapping" jitter is periodic and occurs once every 22.35ms, we can state that this jitter has a frequency of 44.7Hz.

8.2.2.3 The 44.736Mbps - 1ppm Case

In this case, let us assume that a DS3 signal, with a bit-rate of 44.736Mbps - 1ppm is being mapped into an STS-1 signal with a bit-rate of 51.84Mbps + 0ppm. In this case, the following this will occur.

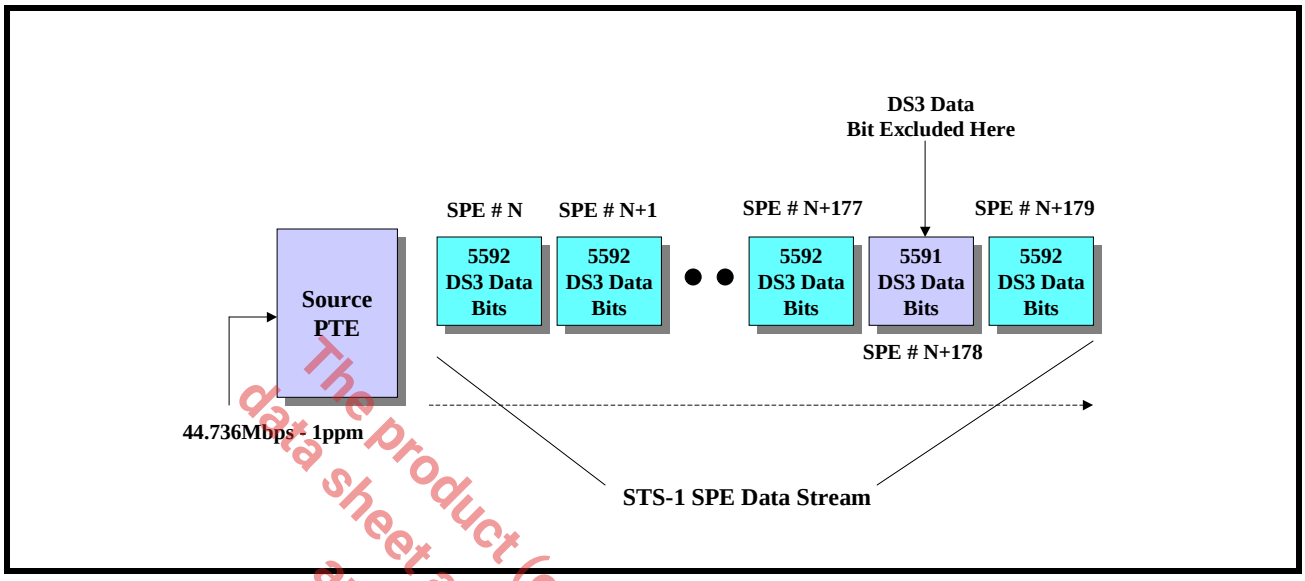
- In general, most of the STS-1 SPEs will each transport 5592 DS3 data bits.
- However, within a "one-second" period a DS3 signal that has a bit-rate of 44.736Mbps - 1ppm will deliver approximately 45 too few bits below that of a DS3 signal with a bit-rate of 44.736Mbps + 0ppm. This means that this particular signal will need to "positive-stuff" or exclude a DS3 data bit from mapping every (1/44.736) = 22.35ms. In other words, we will need to avoid mapping this DS3 data-bit about one in every (22.35ms*8000) = 178.8 STS-1 SPEs.

What does this mean at the "Source" PTE?

All of this means that as the "Source" PTE maps this DS3 signal, with a data rate of 44.736Mbps - 1ppm into an STS-1 signal, most of the resulting "outbound" STS-1 SPEs will transport 5592 DS3 data bits (e.g., 3 Stuff Opportunity bits will be carrying DS3 data bits, the remaining 6 Stuff Opportunity bits are "stuff" bits). However, in approximately one out of 178.8 "outbound" STS-1 SPEs, there will be a need for a "positive-stuffing" event. Whenever these "positive-stuffing" events occur then (for these particular STS-1 SPEs) the SPE will carry only 5591 DS3 data bits (e.g., in this case, only 2 Stuff Opportunity bits will be carrying DS3 data-bits, and the remaining 7 Stuff Opportunity bits are "stuff" bits).

Figure 49 presents an illustration of the STS-1 SPE traffic that will be generated by the "Source" PTE, during this condition.

FIGURE 49. AN ILLUSTRATION OF THE STS-1 SPE TRAFFIC THAT WILL BE GENERATED BY THE SOURCE PTE, WHEN MAPPING A DS3 SIGNAL THAT HAS A BIT RATE OF 44.736MBPS - 1PPM, INTO AN STS-1 SIGNAL



What does this mean at the Destination PTE?

In this case, this DS3 signal (which has now been mapped into an STS-1 data-stream) will be transported across the SONET network. As this STS-1 signal arrives at the "Destination" PTE, this PTE will extract (or de-map) this DS3 data from each incoming STS-1 SPE. Now, in this case, most (e.g., 177/178.8) of the incoming STS-1 SPEs will contain 5592 DS3 data-bits. Therefore, the nominal data rate of the DS3 signal being de-mapped from SONET will be 44.736Mbps. However, in approximately 1 out of every 178 incoming STS-1 SPEs, the SPE will carry only 5591 DS3 data bits. This means that (during these times) the data rate of the de-mapped DS3 signal will have an instantaneous frequency that is less than 44.736Mbps. These "excursions" of the de-mapped DS3 data-rate, from the nominal DS3 frequency can be viewed as occurrences of mapping/de-mapping jitter with an amplitude of approximately 1UI-pp.

Since this occurrence of "de-mapping" jitter is periodic and occurs once every 22.35ms, we can state that this jitter has a frequency of 44.7Hz.

We talked about De-Mapping Jitter, What about De-Mapping Wander?

The Telcordia and Bellcore specifications define "Wander" as "Jitter with a frequency of less than 10Hz". Based upon this definition, the DS3 signal (that is being transported by SONET) will cease to contain jitter and will now contain "Wander", whenever the frequency offset of the DS3 signal being mapped into SONET is less than 0.2ppm.

8.3 Jitter/Wander due to Pointer Adjustments

In the previous section, we described how a DS3 signal is asynchronously-mapped into SONET, and we also defined "Mapping/De-mapping" jitter. In this section, we will describe how occurrences within the SONET network will induce jitter/wander within the DS3 signal that is being transported across the SONET network.

In order to accomplish this, we will discuss the following topics in detail.

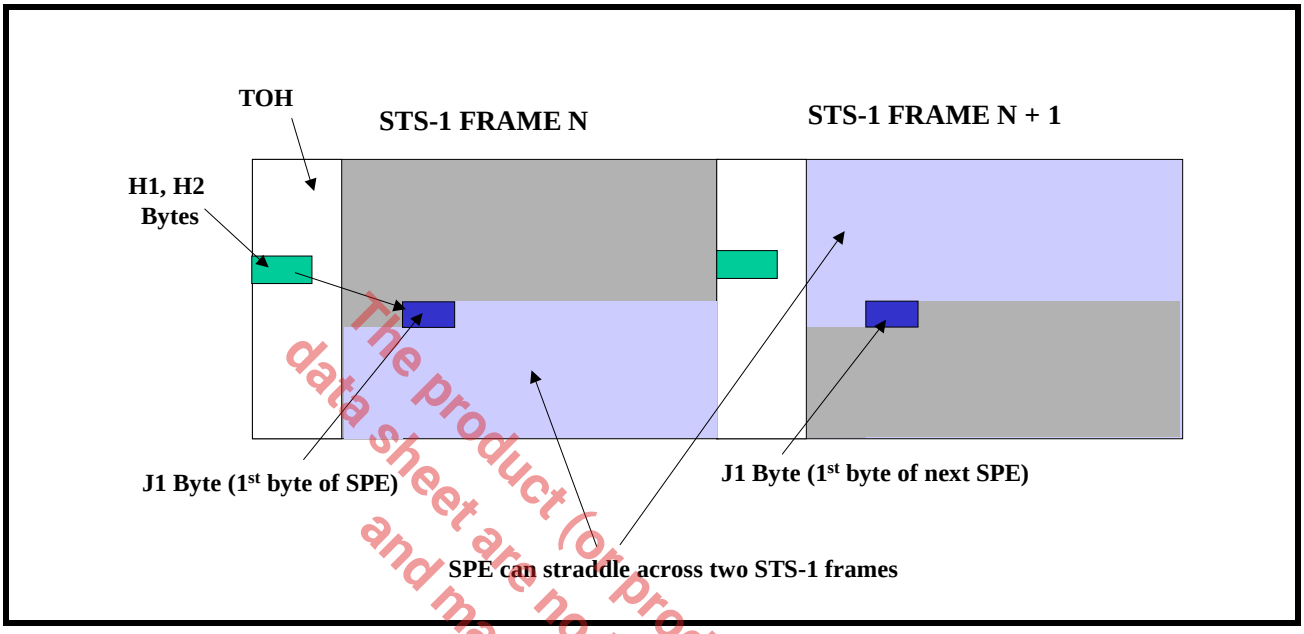
- The concept of an STS-1 SPE pointer
- The concept of Pointer Adjustments
- The causes of Pointer Adjustments
- How Pointer Adjustments induce jitter/wander within a DS3 signal being transported by that SONET network.

8.3.1 The Concept of an STS-1 SPE Pointer

As mentioned earlier, the STS-1 SPE is not aligned to the STS-1 frame boundaries and is permitted to "float" within the Envelope Capacity. As a consequence, the STS-1 SPE will often times "straddle" across two

consecutive STS-1 frames. Figure 50 presents an illustration of an STS-1 SPE straddling across two consecutive STS-1 frames.

FIGURE 50. AN ILLUSTRATION OF AN STS-1 SPE STRADDLING ACROSS TWO CONSECUTIVE STS-1 FRAMES



A PTE that is receiving and terminating an STS-1 data-stream will perform the following tasks.

- It will acquire and maintain STS-1 frame synchronization with the incoming STS-1 data-stream.
- Once the PTE has acquired STS-1 frame synchronization, then it will locate the J1 byte (e.g., the very byte within the very next STS-1 SPE) within the Envelope Capacity by reading out the contents of the H1 and H2 bytes.

The H1 and H2 bytes are referred to (in the SONET standards) as the SPE Pointer Bytes. When these two bytes are concatenated together in order to form a 16-bit word (with the H1 byte functioning as the "Most Significant Byte") then the contents of the "lower" 10 bit-fields (within this 16-bit word) reflects the location of the J1 byte within the Envelope Capacity of the incoming STS-1 data-stream. Figure 51 presents an illustration of the bit format of the H1 and H2 bytes, and indicates which bit-fields are used to reflect the location of the J1 byte.

FIGURE 51. THE BIT-FORMAT OF THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE 10 BITS, REFLECTING THE LOCATION OF THE J1 BYTE, DESIGNATED

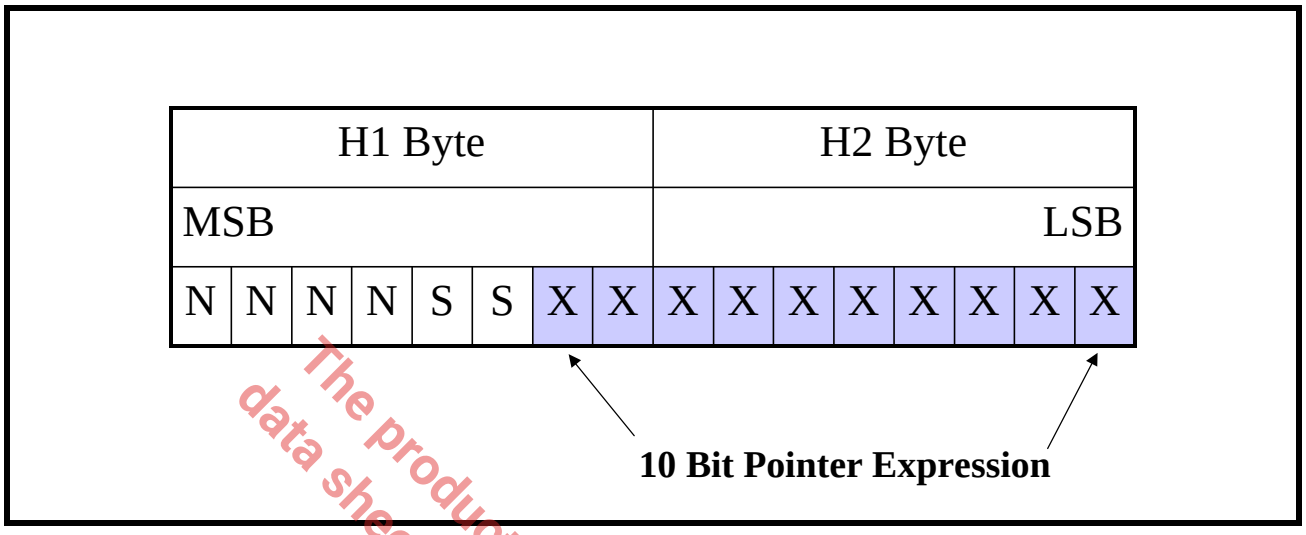
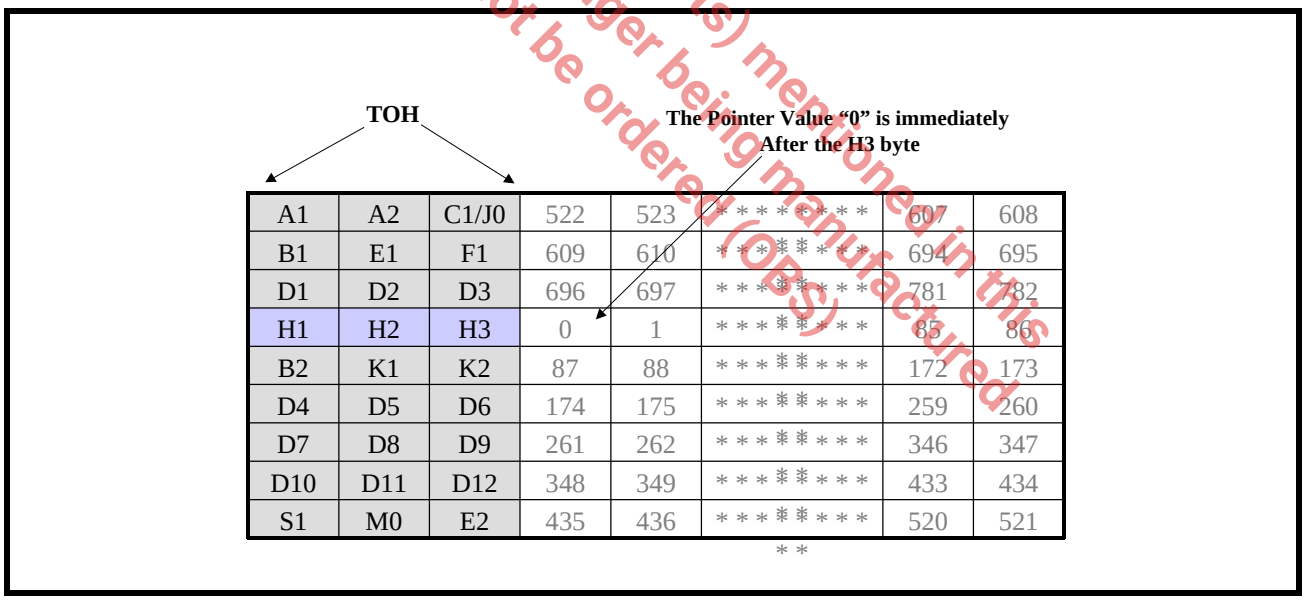


Figure 52 relates the contents within these 10 bits (within the H1 and H2 bytes) to the location of the J1 byte (e.g., the very first byte of the STS-1 SPE) within the Envelope Capacity.

FIGURE 52. THE RELATIONSHIP BETWEEN THE CONTENTS OF THE "POINTER BITS" (E.G., THE 10-BIT EXPRESSION WITHIN THE H1 AND H2 BYTES) AND THE LOCATION OF THE J1 BYTE WITHIN THE ENVELOPE CAPACITY OF AN STS-1 FRAME



A1	A2	C1/J0	522	523	* * * * * * * * *	607	608
B1	E1	F1	609	610	* * * * * * * * *	694	695
D1	D2	D3	696	697	* * * * * * * * *	781	782
H1	H2	H3	0	1	* * * * * * * * *	85	86
B2	K1	K2	87	88	* * * * * * * * *	172	173
D4	D5	D6	174	175	* * * * * * * * *	259	260
D7	D8	D9	261	262	* * * * * * * * *	346	347
D10	D11	D12	348	349	* * * * * * * * *	433	434
S1	M0	E2	435	436	* * * * * * * * *	520	521

NOTES:

1. *If the content of the "Pointer Bits" is "0x00" then the J1 byte is located immediately after the H3 byte, within the Envelope Capacity.*
2. *If the contents of the 10-bit expression exceed the value of 0x30F (or 782, in decimal format) then it does not contain a valid pointer value.*

8.3.2 Pointer Adjustments within the SONET Network

The word SONET stands for "Synchronous Optical NETwork. This name implies that the entire SONET network is synchronized to a single clock source. However, because the SONET (and SDH) Networks can

span thousands of miles, traverse many different pieces of equipments, and even cross International boundaries; in practice, the SONET/SDH network is NOT synchronized to a single clock source.

In practice, the SONET/SDH network can be thought of as being divided into numerous "Synchronization Islands". Each of these "Synchronization Islands" will consist of numerous pieces of SONET Terminal Equipment. Each of these pieces of SONET Terminal Equipment will all be synchronized to a single Stratum-1 clock source which is the most accurate clock source within the Synchronization Island. Typically a "Synchronization Island" will consist of a single "Timing Master" equipment along with multiple "Timing Slave" pieces of equipment. This "Timing Master" equipment will be directly connected to the Stratum-1 clock source and will have the responsibility of distributing a very accurate clock signal (that has been derived from the Stratum 1 clock source) to each of the "Timing Slave" pieces of equipment within the "Synchronization Island". The purpose of this is to permit each of the "Timing Slave" pieces of equipment to be "synchronized" with the "Timing Master" equipment, as well as the Stratum 1 Clock source. Typically this "clock distribution" is performed in the form of a BITS (Building Integrated Timing Supply) clock, in which a very precise clock signal is provided to the other pieces of equipment via a T1 or E1 line signal.

Many of these "Synchronization Islands" will use a Stratum-1" clock source that is derived from GPS pulses that are received from Satellites that operate at Geo-synchronous orbit. Other "Synchronization Islands" will use a Stratum-1" clock source that is derived from a very precise local atomic clock. As a consequence, different "Synchronization Islands" will use different Stratum 1 clock sources. The up-shot of having these "Synchronization Islands" that use different "Stratum-1 clock" sources, is that the Stratum 1 Clock frequencies, between these "Synchronization Islands" are likely to be slightly different from each other. These "frequency-differences" within Stratum 1 clock sources will result in "clock-domain changes" as a SONET signal (that is traversing the SONET network) passes from one "Synchronization Island" to another.

The following section will describe how these "frequency differences" will cause a phenomenon called "pointer adjustments" to occur in the SONET Network.

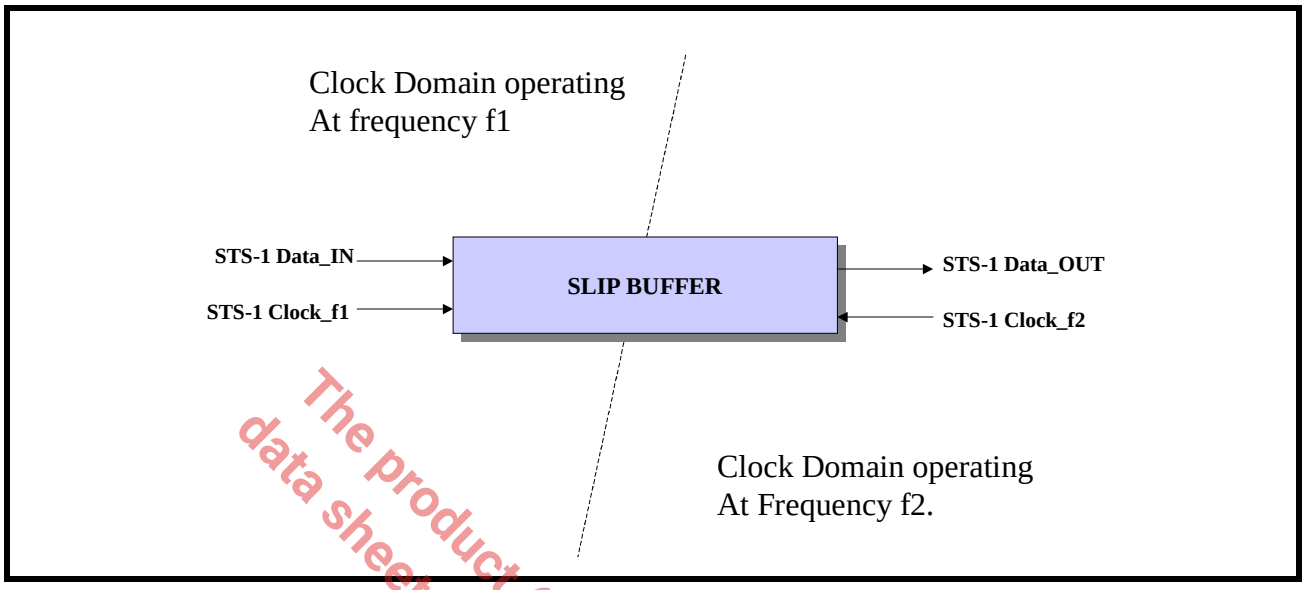
8.3.3 Causes of Pointer Adjustments

The best way to discuss how pointer adjustment events occur is to consider an STS-1 signal, which is driven by a timing reference of frequency f1; and that this STS-1 signal is being routed to a network equipment (that resides within a different "Synchronization Island") and processes STS-1 data at a frequency of f2.

NOTE: *Clearly, both frequencies f1 and f2 are at the STS-1 rate (e.g., 51.84MHz). However, these two frequencies are likely to be slightly different from each other.*

Now, since the STS-1 signal (which is of frequency f1) is being routed to the network element (which is operating at frequency f2), the typical design approach for handling "clock-domain" differences is to route this STS-1 signal through a "Slip Buffer" as illustrated below.

FIGURE 53. AN ILLUSTRATION OF AN STS-1 SIGNAL BEING PROCESSED VIA A SLIP BUFFER



In the "Slip Buffer, the "input" STS-1 data (labeled "STS-1 Data_IN") is latched into the FIFO, upon a given edge of the corresponding "STS-1 Clock_f1" input clock signal. The STS-1 Data (labeled "STS-1 Data_OUT") is clocked out of the Slip Buffer upon a given edge of the "STS-1 Clock_f2" input clock signal.

The behavior of the data, passing through the "Slip Buffer" is now described for each possible relationship between frequencies f1 and f2.

If f1 = f2

If both frequencies, f1 and f2 are exactly equal, then the STS-1 data will be "clocked" into the "Slip Buffer" at exactly the same rate that it is "clocked out". In this case, the "Slip Buffer" will neither fill-up nor become depleted. As a consequence, no pointer-adjustments will occur in this STS-1 data stream. In other words, the STS-1 SPE will remain at a constant location (or offset) within each STS-1 envelope capacity for the duration that this STS-1 signal is supporting this particular service.

If f1 < f2

If frequency f1 is less than f2, then this means that the STS-1 data is being "clocked out" of the "Slip Buffer" at a faster rate than it is being clocked in. In this case, the "Slip Buffer" will eventually become depleted. Whenever this occurs, a typical strategy is to "stuff" (or insert) a "dummy byte" into the data stream. The purpose of stuffing this "dummy byte" is to compensate for the frequency differences between f1 and f2, and attempt to keep the "Slip Buffer, at a somewhat constant fill level.

NOTE: *This "dummy byte" does not carry any valuable information (not for the user, nor for the system).*

Since this "dummy byte" carries no useful information, it is important that the "Receiving PTE" be notified anytime this "dummy byte" stuffing occurs. This way, the Receiving Terminal can "know" not to treat this "dummy byte" as user data.

Byte-Stuffing and Pointer Incrementing in a SONET Network

Whenever this "byte-stuffing" occurs then the following other things occur within the STS-1 data stream.

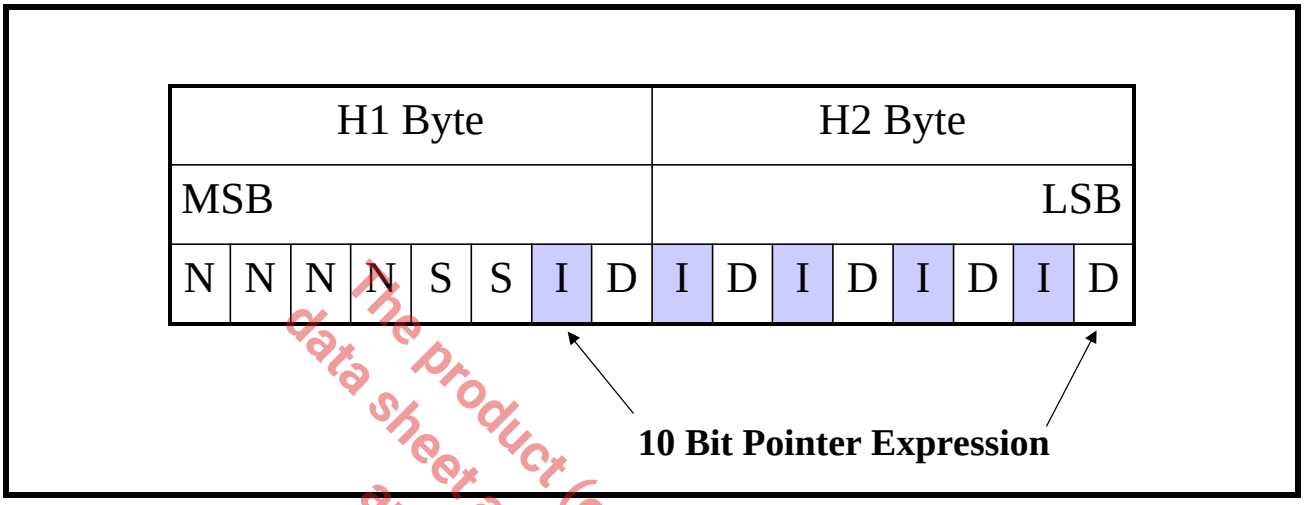
During the STS-1 frame that contains the "Byte-Stuffing" event

a. The "stuff-byte" will be inserted into the byte position immediately after the H3 byte. This insertion of the "dummy byte" immediately after the H3 byte position will cause the J1 byte (and in-turn, the rest of the SPE) to be "byte-shifted" away from the H3 byte. As a consequence, the offset between the H3 byte position and the STS-1 SPE will now have been increased by 1 byte.

b. The "Transmitting" Network Equipment will notify the remote terminal of this byte-stuffing event, by inverting certain bits within the "pointer word" (within the H1 and H2 bytes) that are referred to as "I" bits.

Figure 54 presents an illustration of the bit-format within the 16-bit word (consist of the H1 and H2 bytes) with the "I" bits designated.

FIGURE 54. AN ILLUSTRATION OF THE BIT FORMAT WITHIN THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE "I" BITS DESIGNATED



NOTE: *At this time the "I" bits are inverted in order to denote that an "incrementing" pointer adjustment event is currently occurring.*

During the STS-1 frame that follows the "Byte-Stuffing" event

The "I" bits (within the "pointer-word") will be set back to their normal value; and the contents of the H1 and H2 bytes will be incremented by "1".

If f1 > f2

If frequency f1 is greater than f2, then this means that the STS-1 data is being clocked into the "Slip Buffer" at a faster rate than is being clocked out. In this case, the "Slip Buffer" will start to fill up. Whenever this occurs, a typical strategy is to delete (e.g., negative-stuff) a byte from the Slip Buffer. The purpose of this "negative-stuffing" is to compensate for the frequency differences between f1 and f2; and to attempt to keep the "Slip Buffer" at a somewhat constant fill-level.

NOTE: *This byte, which is being "un-stuffed" does carry valuable information for the user (e.g., this byte is typically a payload byte). Therefore, whenever this negative stuffing occurs, two things must happen.*

a. The "negative-stuffed" byte must not be simply discarded. In other words, it must somehow also be transmitted to the remote PTE with the remainder of the SPE data.

b. The remote PTE must be notified of the occurrence of these "negative-stuffing" events. Further, the remote PTE must know where to obtain this "negative-stuffed" byte.

Negative-Stuffing and Pointer-Decrementing in a SONET Network

Whenever this "byte negative-stuffing" occurs then the following other things occur within the STS-1 data-stream.

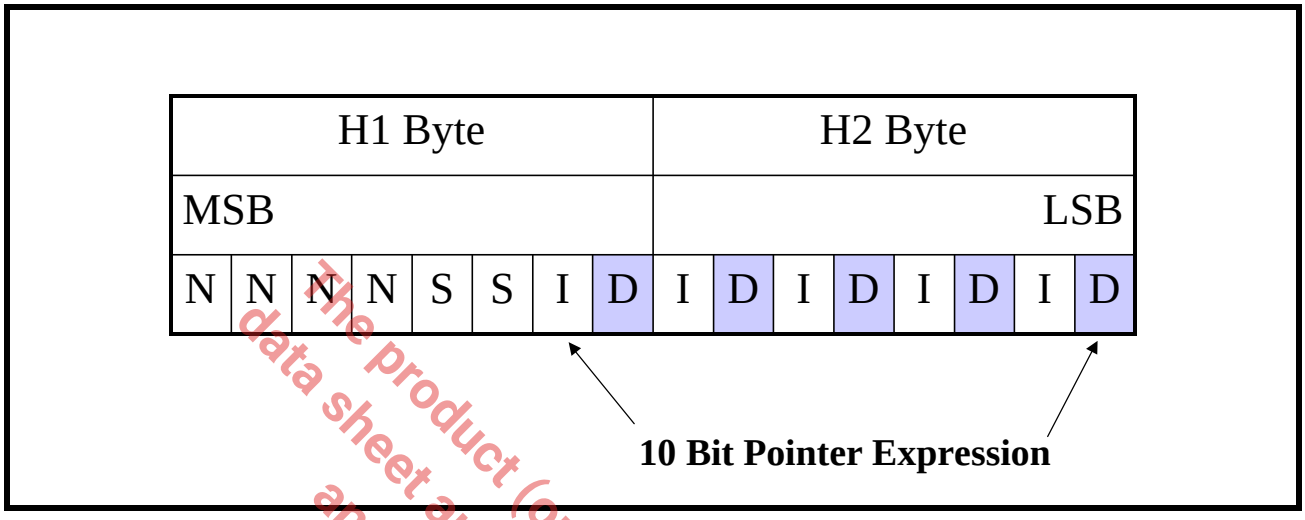
During the STS-1 frame that contains the "Negative Byte-Stuffing" Event

a. The "Negative-Stuffed" byte will be inserted into the H3 byte position. Whenever an SPE data byte is inserted into the H3 byte position (which is ordinarily an unused byte), the number of bytes that will exist between the H3 byte and the J1 byte within the very next SPE will be reduced by 1 byte. As a consequence, in this case, the J1 byte (and in-turn, the rest of the SPE) will now be "byte-shifted" towards the H3 byte position.

b. The "Transmitting" Network Element will notify the remote terminal of this "negative-stuff" event by inverting certain bits within the "pointer word" (within the H1 and H2 bytes) that are referred to as "D" bits.

Figure 55 presents an illustration of the bit format within the 16-bit word (consisting of the H1 and H2 bytes) with the "D" bits designated.

FIGURE 55. AN ILLUSTRATION OF THE BIT-FORMAT WITHIN THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE "D" BITS DESIGNATED



NOTE: *At this time the "D" bits are inverted in order to denote that a "decrementing" pointer adjustment event is currently occurring.*

During the STS-1 frame that follows the "Negative Byte-Stuffing" Event

The "D" bits (within the pointer-word) will be set back to their normal value; and the contents of the H1 and H2 bytes will be decremented by one.

8.3.4 Why are we talking about Pointer Adjustments?

The overall SONET network consists of numerous "Synchronization Islands". As a consequence, whenever a SONET signal is being transmitted from one "Synchronization Island" to another; that SONET signal will undergo a "clock domain" change as it traverses the network. This clock domain change will result in periodic pointer-adjustments occurring within this SONET signal. Depending upon the direction of this "clock-domain" shift that the SONET signal experiences, there will either be periodic "incrementing" pointer-adjustment events or periodic "decrementing" pointer-adjustment events within this SONET signal.

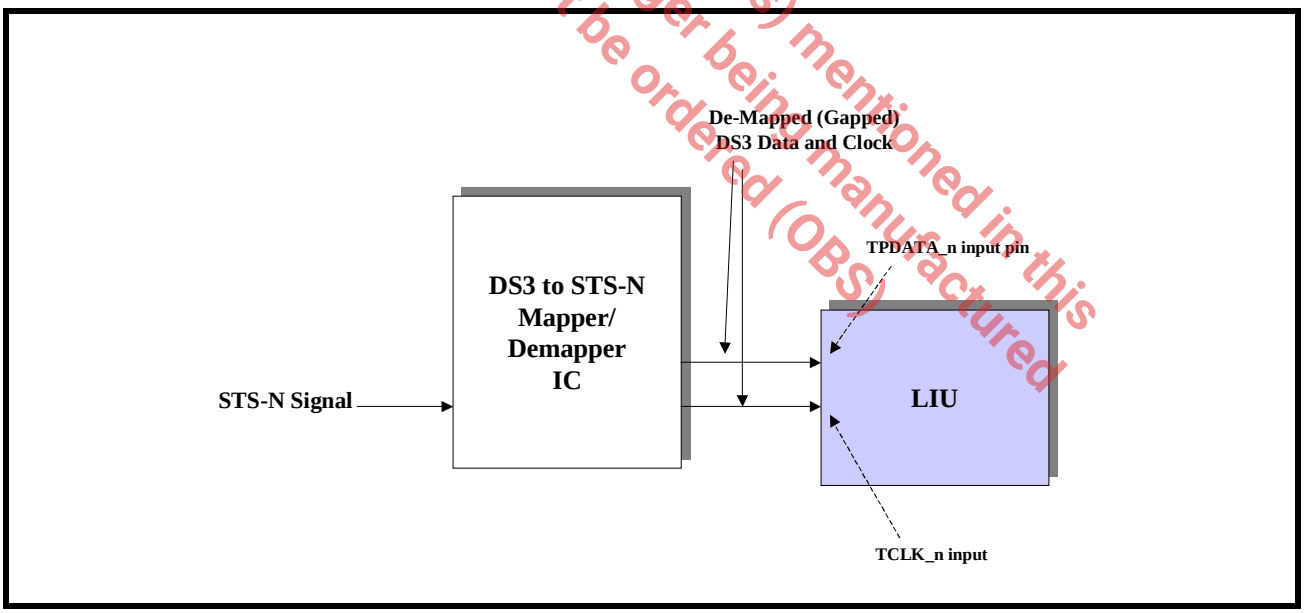
Regardless of whether a given SONET signal is experiencing incrementing or decrementing pointer adjustment events, each pointer adjustment event will result in an abrupt 8-bit shift in the position of the SPE within the STS-1 data-stream. If this STS-1 signal is transporting an "asynchronously-mapped" DS3 signal; then this 8-bit shift in the location of the SPE (within the STS-1 signal) will result in approximately 8UIpp of jitter within the asynchronously-mapped DS3 signal, as it is de-mapped from SONET. In “Section 8.5, A Review of the Category I Intrinsic Jitter Requirements (per Telcordia GR-253-CORE) for DS3 applications” on page 78 we will discuss the "Category I Intrinsic Jitter Requirements (for DS3 Applications) per Telcordia GR-253-CORE. However, for now we will simply state that this 8UIpp of intrinsic jitter far exceeds these "intrinsic jitter" requirements.

In summary, pointer-adjustments events are a "fact of life" within the SONET/SDH network. Further, pointer-adjustment events, within a SONET signal that is transporting an asynchronously-mapped DS3 signal, will impose a significant impact on the Intrinsic Jitter and Wander within that DS3 signal as it is de-mapped from SONET.

8.4 Clock Gapping Jitter

In most applications (in which the LIU will be used in a SONET De-Sync Application) the user will typically interface the LIU to a Mapper Device in the manner as presented below in Figure 56.

FIGURE 56. ILLUSTRATION OF THE TYPICAL APPLICATIONS FOR THE LIU IN A SONET DE-SYNC APPLICATION



In this application, the Mapper IC will have the responsibility of receiving an STS-N signal (from the SONET Network) and performing all of the following operations on this STS-N signal.

- Byte-de-interleaving this incoming STS-N signal into N STS-1 signals
- Terminating each of these STS-1 signals
- Extracting (or de-mapping) the DS3 signal(s) from the SPEs within each of these terminated STS-1 signals.

In this application, these Mapper devices can be thought of as multi-channel devices. For example, an STS-3 Mapper can be viewed as a 3-Channel DS3/STS-1 to STS-3 Mapper IC. Similarly, an STS-12 Mapper can be

viewed as a 12-Channel DS3/STS-1 to STS-12 Mapper IC. Continuing on with this line of thought, if a Mapper IC is configured to receive an STS-N signal, and (from this STS-N signal) de-map and output N DS3 signals (towards the DS3 facility), then it will typically do so in the following manner.

- In many cases, the Mapper IC will output this DS3 signal, using both a "Data-Signal" and a "Clock-Signal". In many cases, the Mapper IC will output the contents of an entire STS-1 data-stream via the Data-Signal.
- However, as the Mapper IC output this STS-1 data-stream, it will typically supply clock pulses (via the Clock-Signal output) coincident to whenever a DS3 bit is being output via the Data-Signal. In this case, the Mapper IC will NOT supply a clock pulse coincident to when a TOH, POH, or any "non-DS3 data-bit" is being output via the "Data-Signal".

Now, since the Mapper IC will output the entire STS-1 data stream (via the Data-Signal), the output Clock-Signal will be of the form such that it has a period of 19.3ns (e.g., a 51.84MHz clock signal). However, the Mapper IC will still generate approximately 44,736,000 clock pulses during any given one second period. Hence, the clock signal that is output from the Mapper IC will be a horribly gapped 44.736MHz clock signal. One can view such a clock signal as being a very-jittery 44.736MHz clock signal. This jitter that exists within the "Clock-Signal" is referred to as "Clock-Gapping" Jitter. A more detailed discussion on how the user must handle this type of jitter is presented in “Section 8.8.2, Recommendations on Pre-Processing the Gapped Clocks (from the Mapper/ASIC Device) prior to routing this DS3 Clock and Data-Signals to the Transmit Inputs of the LIU” on page 89.

8.5 A Review of the Category I Intrinsic Jitter Requirements (per Telcordia GR-253-CORE) for DS3 applications

The "Category I Intrinsic Jitter Requirements" per Telcordia GR-253-CORE (for DS3 applications) mandates that the user perform a large series of tests against certain specified "Scenarios". These "Scenarios" and their corresponding requirements is summarized in Table 19, below.

TABLE 19: SUMMARY OF "CATEGORY I INTRINSIC JITTER REQUIREMENT PER TELCORDIA GR-253-CORE, FOR DS3 APPLICATIONS

SCENARIO DESCRIPTION	SCENARIO NUMBER	TELCORDIA GR-253-CORE CATEGORY I INTRINSIC JITTER REQUIREMENTS	COMMENTS
DS3 De-Mapping Jitter		0.4UI-pp	Includes effects of De-Mapping and Clock Gapping Jitter
Single Pointer Adjustment	A1	0.3UI-pp + Ao	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.NOTE: Ao is the amount of intrinsic jitter that was measured during the "DS3 De-Mapping Jitter" phase of the Test.
Pointer Bursts	A2	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
Phase Transients	A3	1.2UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
87-3 Pattern	A4	1.0UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
87-3 Add	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
87-3 Cancel	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
Continuous Pattern	A4	1.0UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.

TABLE 19: SUMMARY OF "CATEGORY I INTRINSIC JITTER REQUIREMENT PER TELCORDIA GR-253-CORE, FOR DS3 APPLICATIONS

SCENARIO DESCRIPTION	SCENARIO NUMBER	TELCORDIA GR-253-CORE CATEGORY I INTRINSIC JITTER REQUIREMENTS	COMMENTS
Continuous Add	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
Continuous Cancel	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.

NOTE: *All of these intrinsic jitter measurements are to be performed using a band-pass filter of 10Hz to 400kHz.*

Each of the scenarios presented in Table 19, are briefly described below.

8.5.1 DS3 De-Mapping Jitter

DS3 De-Mapping Jitter is the amount of Intrinsic Jitter that will be measured within the "Line" or "Facility-side" DS3 signal, (after it has been de-mapped from a SONET signal) without the occurrence of "Pointer Adjustments" within the SONET signal.

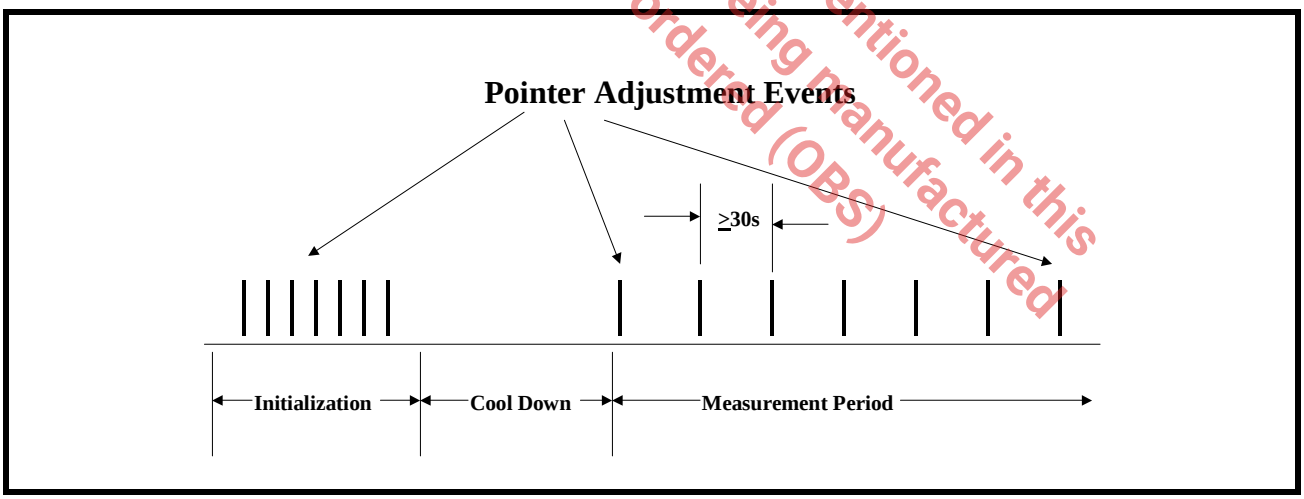
Telcordia GR-253-CORE requires that the "DS3 De-Mapping" Jitter be less than 0.4UI-pp, when measured over all possible combinations of DS3 and STS-1 frequency offsets.

8.5.2 Single Pointer Adjustment

Telcordia GR-253-CORE states that if each pointer adjustment (within a continuous stream of pointer adjustments) is separated from each other by a period of 30 seconds, or more; then they are sufficiently isolated to be considered "Single-Pointer Adjustments".

Figure 57 presents an illustration of the "Single Pointer Adjustment" Scenario.

FIGURE 57. ILLUSTRATION OF SINGLE POINTER ADJUSTMENT SCENARIO



Telcordia GR-253-CORE states that the Intrinsic Jitter that is measured (within the DS3 signal) that is ultimately de-mapped from a SONET signal that is experiencing "Single-Pointer Adjustment" events, must NOT exceed the value 0.3UI-pp + Ao.

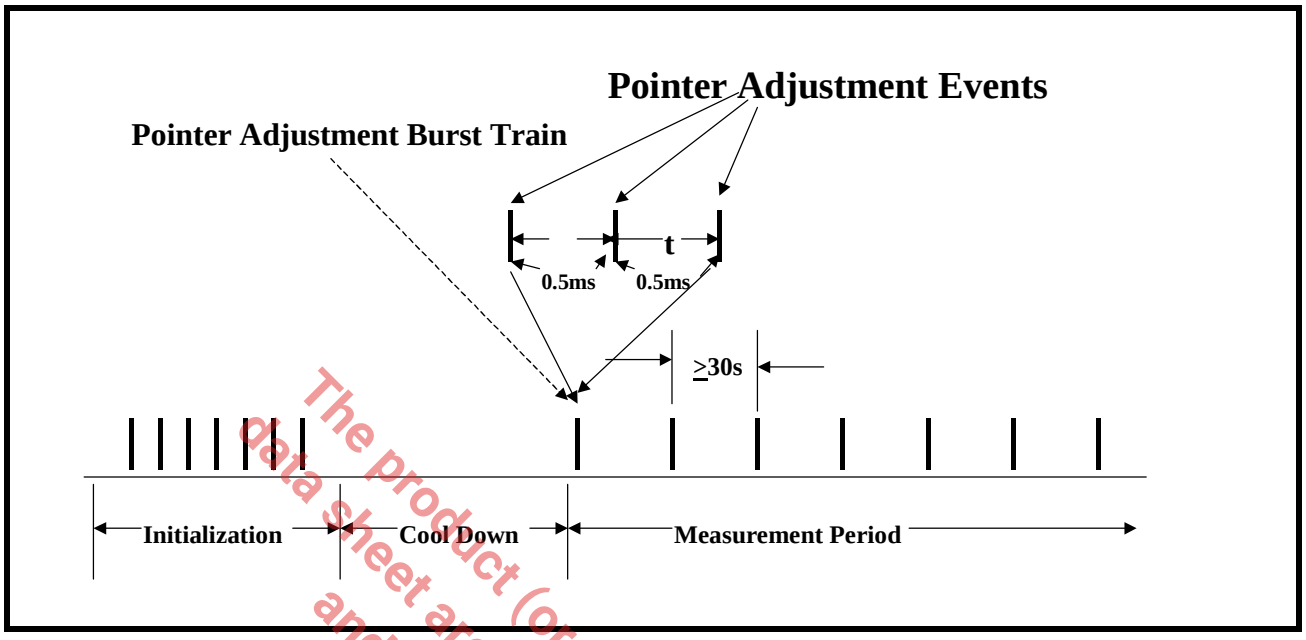
NOTES:

1. *Ao is the amount of Intrinsic Jitter that was measured during the "De-Mapping" Jitter portion of this test.*
2. *Testing must be performed for both Incrementing and Decrementing Pointer Adjustments.*

8.5.3 Pointer Burst

Figure 58 presents an illustration of the "Pointer Burst" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 58. ILLUSTRATION OF BURST OF POINTER ADJUSTMENT SCENARIO

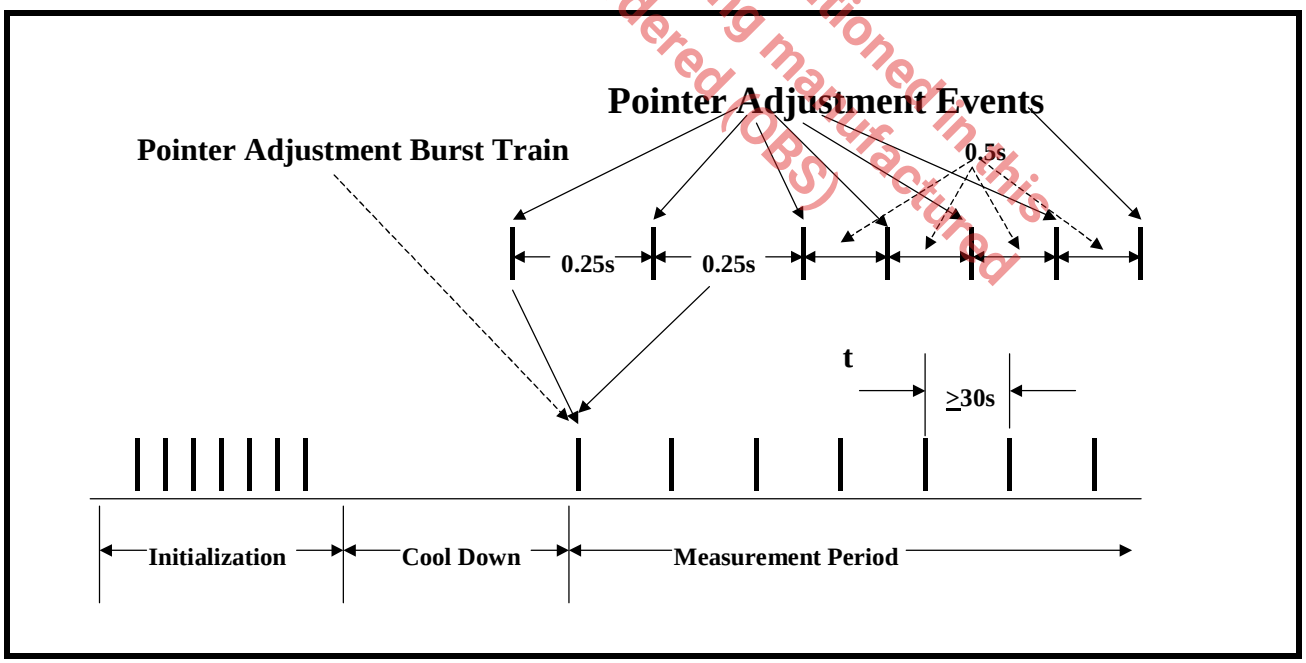


Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Burst of Pointer Adjustment" scenario, must NOT exceed 1.3UI-pp.

8.5.4 Phase Transients

Figure 59 presents an illustration of the "Phase Transients" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 59. ILLUSTRATION OF "PHASE-TRANSIENT" POINTER ADJUSTMENT SCENARIO

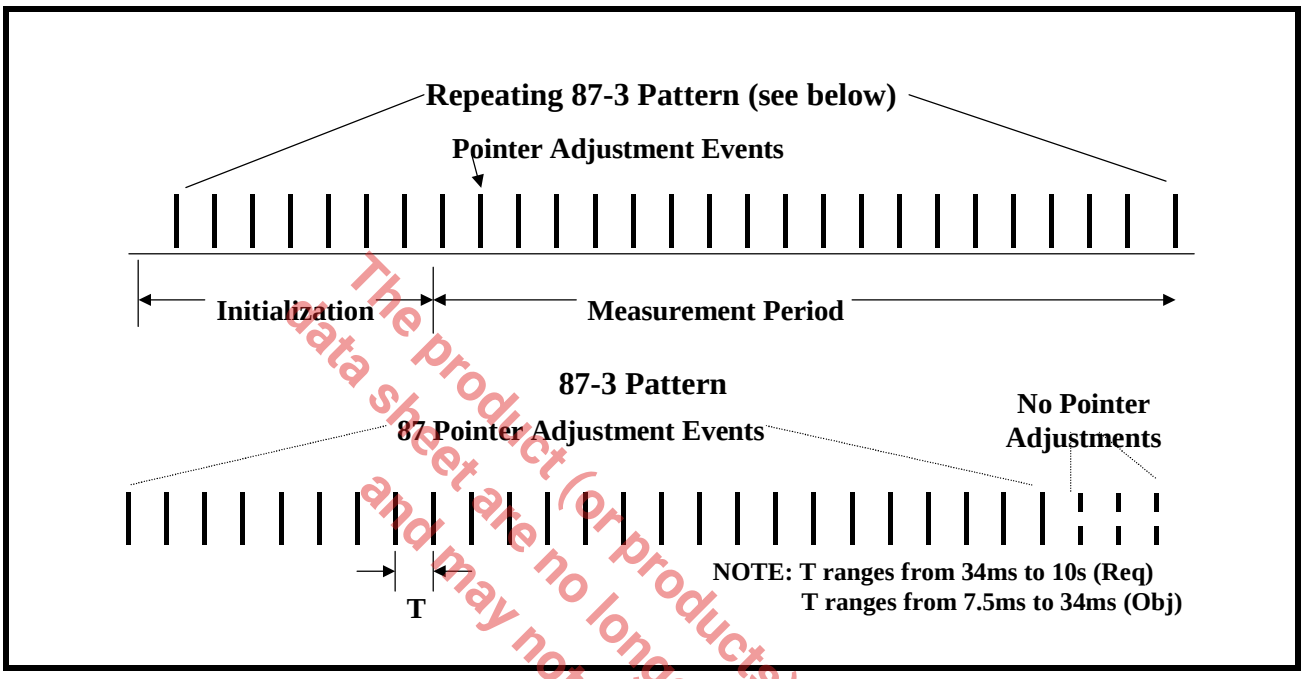


Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Phase Transient - Pointer Adjustment" scenario must NOT exceed 1.2UI-pp.

8.5.5 87-3 Pattern

Figure 60 presents an illustration of the "87-3 Continuous Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 60. AN ILLUSTRATION OF THE 87-3 CONTINUOUS POINTER ADJUSTMENT PATTERN



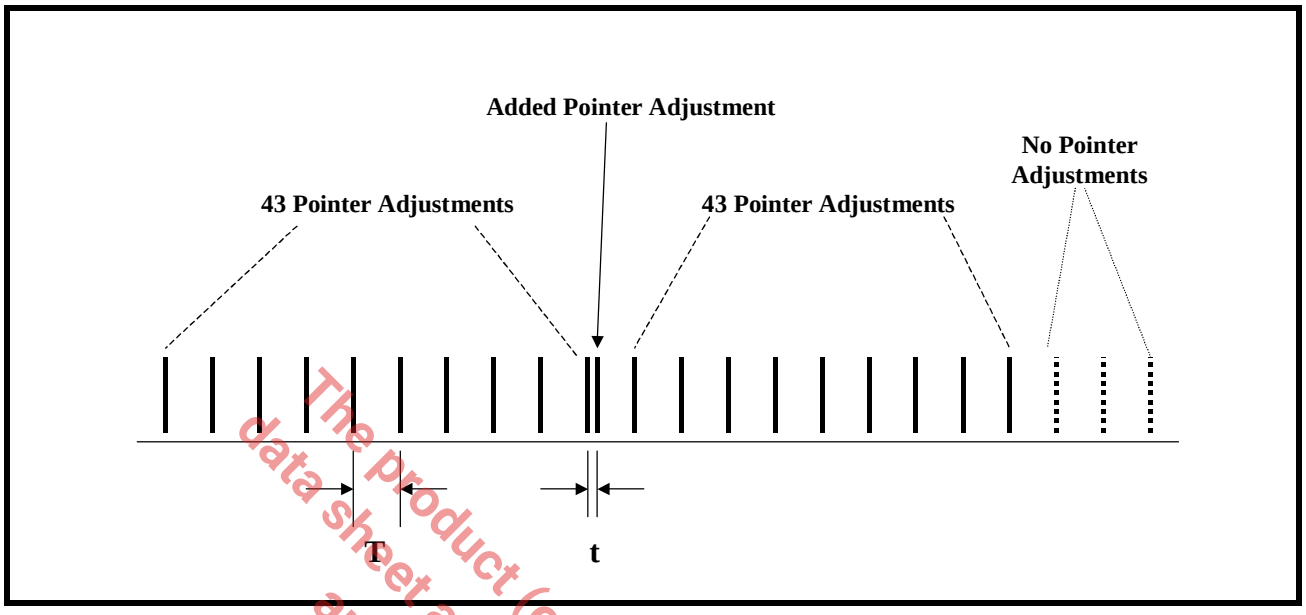
Telcordia GR-253-CORE defines an "87-3 Continuous" Pointer Adjustment pattern, as a repeating sequence of 90 pointer adjustment events. Within this 90 pointer adjustment event, 87 pointer adjustments are actually executed. The remaining 3 pointer adjustments are never executed. The spacing between individual pointer adjustment events (within this scenario) can range from 7.5ms to 10seconds.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "87-3 Continuous" pattern of Pointer Adjustments, must not exceed 1.0UI-pp.

8.5.6 87-3 Add

Figure 61 presents an illustration of the "87-3 Add Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 61. ILLUSTRATION OF THE 87-3 ADD POINTER ADJUSTMENT PATTERN



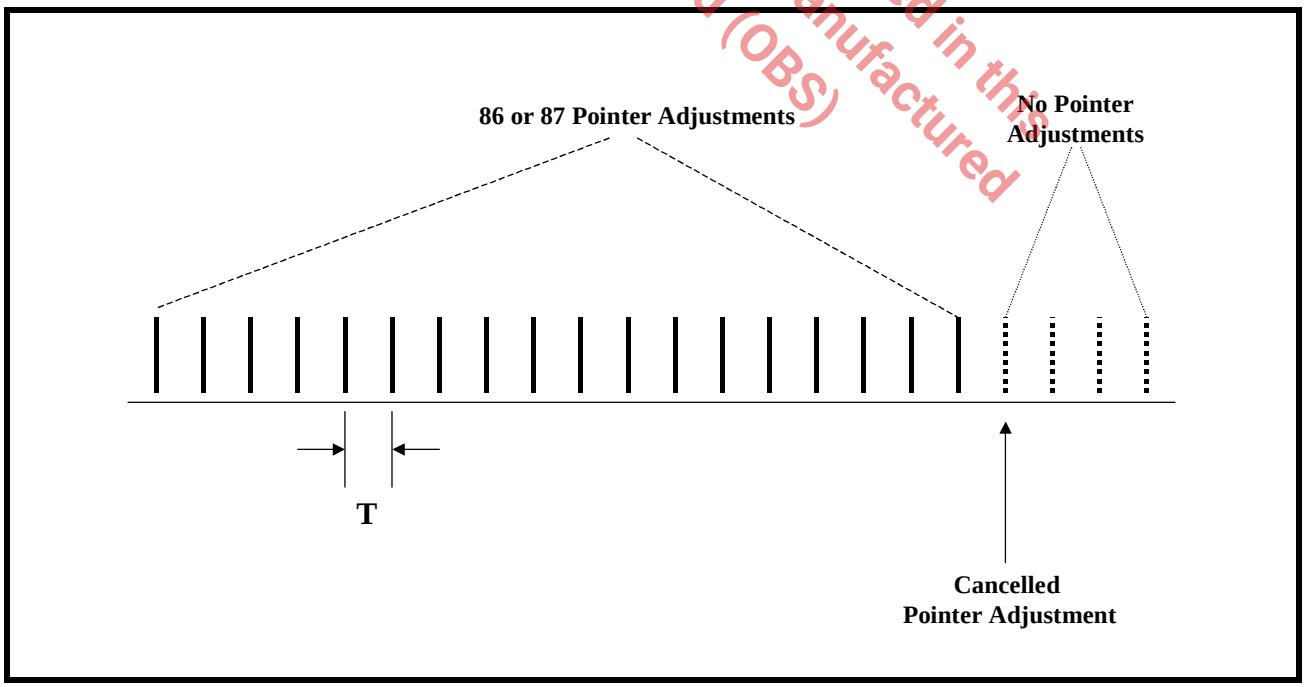
Telcordia GR-253-CORE defines an "87-3 Add" Pointer Adjustment, as the "87-3 Continuous" Pointer Adjustment pattern, with an additional pointer adjustment inserted, as shown above in Figure 61.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "87-3 Add" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

8.5.7 87-3 Cancel

Figure 62 presents an illustration of the 87-3 Cancel Pattern Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 62. ILLUSTRATION OF 87-3 CANCEL POINTER ADJUSTMENT SCENARIO



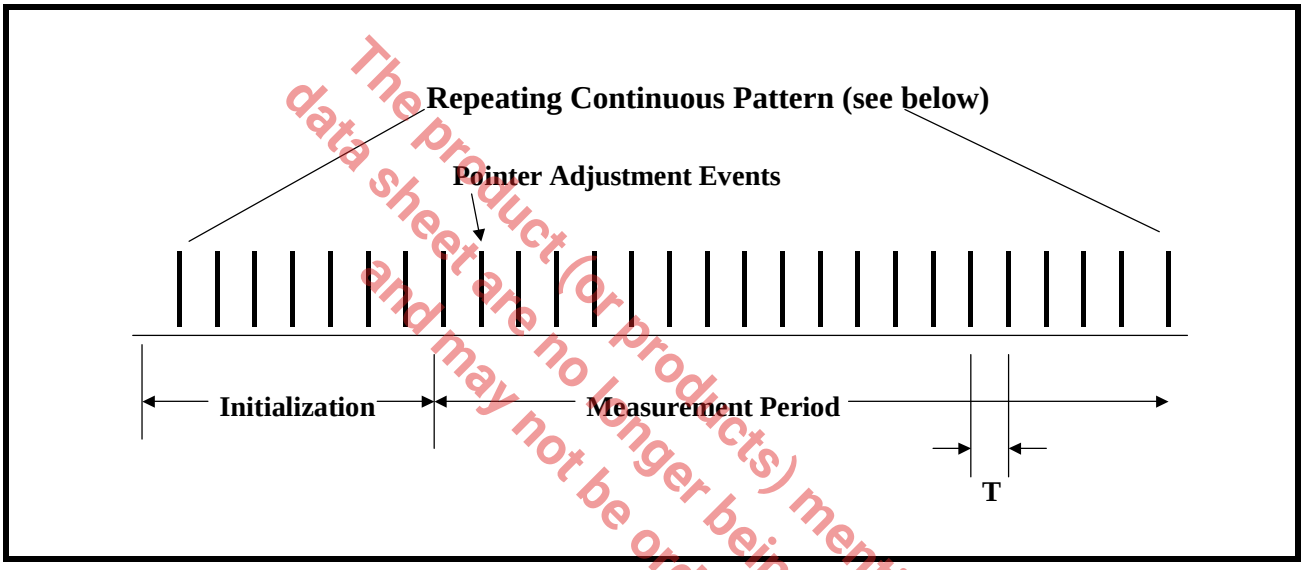
Telcordia GR-253-CORE defines an "87-3 Cancel" Pointer Adjustment, as the "87-3 Continuous" Pointer Adjustment pattern, with an additional pointer adjustment cancelled (or not executed), as shown above in Figure 62.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "87-3 Cancel" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

8.5.8 Continuous Pattern

Figure 63 presents an illustration of the "Continuous" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 63. ILLUSTRATION OF CONTINUOUS PERIODIC POINTER ADJUSTMENT SCENARIO

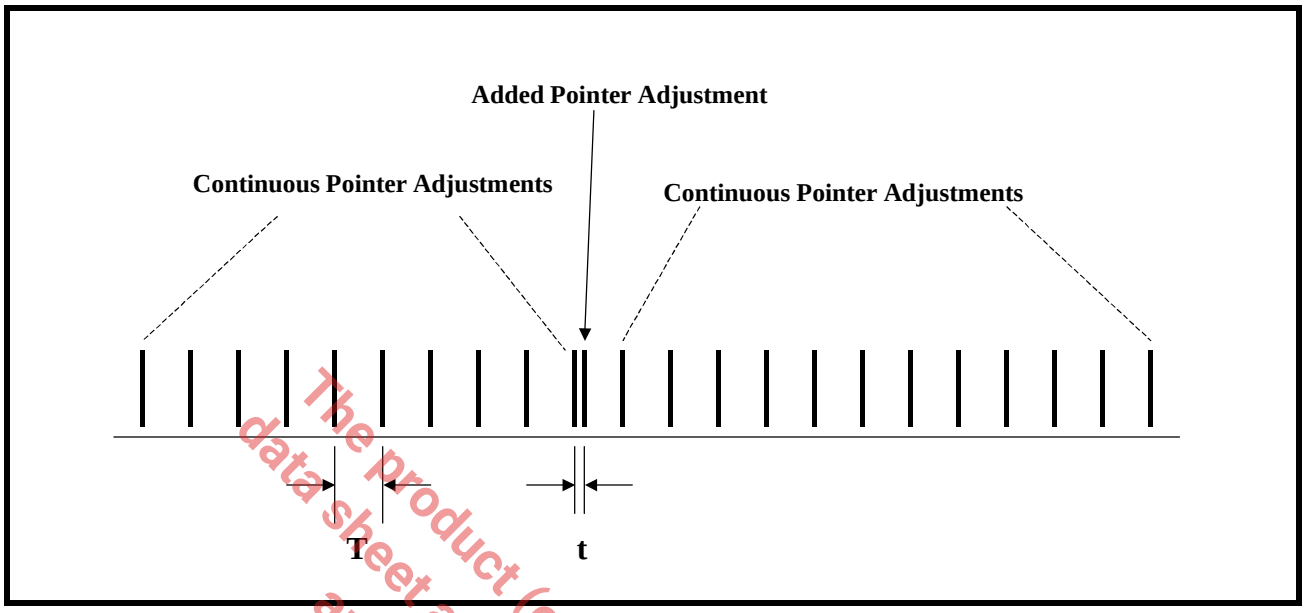


Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Continuous" pattern of Pointer Adjustments, must not exceed 1.0UI-pp. The spacing between individual pointer adjustments (within this scenario) can range from 7.5ms to 10s.

8.5.9 Continuous Add

Figure 64 presents an illustration of the "Continuous Add Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 64. ILLUSTRATION OF CONTINUOUS-ADD POINTER ADJUSTMENT SCENARIO



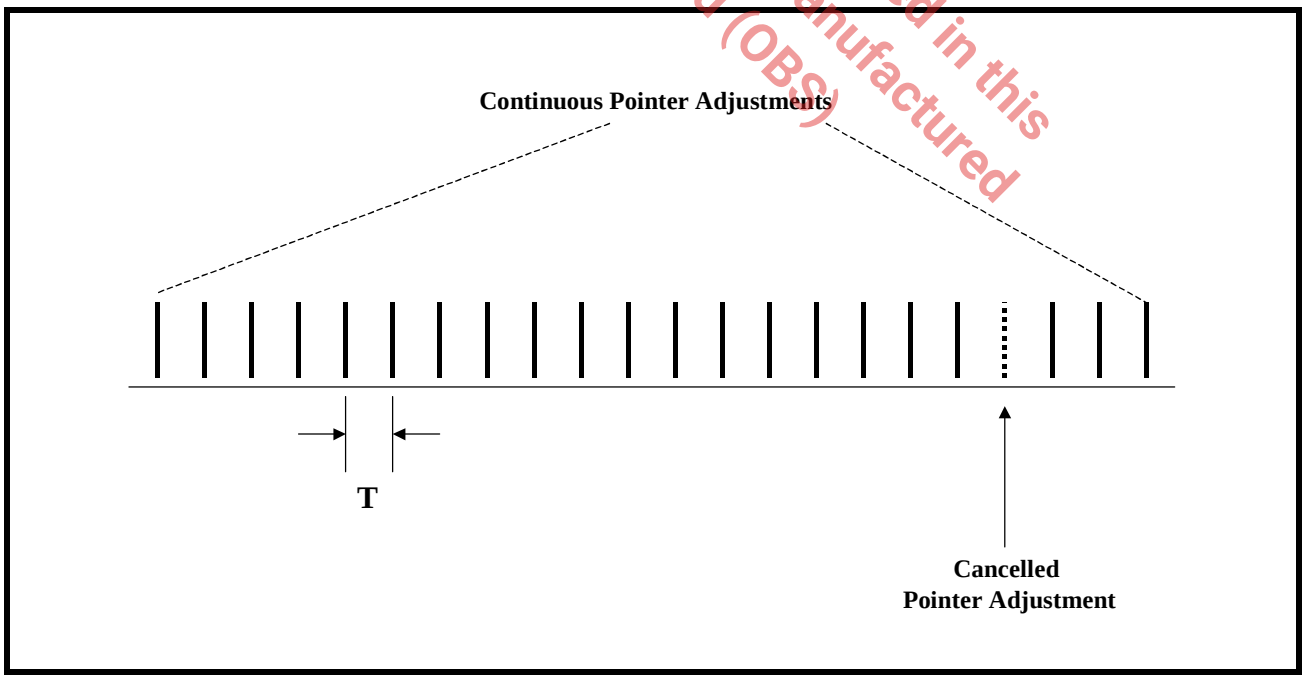
Telcordia GR-253-CORE defines an "Continuous Add" Pointer Adjustment, as the "Continuous" Pointer Adjustment pattern, with an additional pointer adjustment inserted, as shown above in Figure 64.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Continuous Add" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

8.5.10 Continuous Cancel

Figure 65 presents an illustration of the "Continuous Cancel Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 65. ILLUSTRATION OF CONTINUOUS-CANCEL POINTER ADJUSTMENT SCENARIO



Telcordia GR-253-CORE defines a "Continuous Cancel" Pointer Adjustment, as the "Continuous" Pointer Adjustment pattern, with an additional pointer adjustment cancelled (or not executed), as shown above in Figure 65.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Continuous Cancel" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

8.6 A Review of the DS3 Wander Requirements per ANSI T1.105.03b-1997.

To be provided in the next revision of this data sheet.

8.7 A Review of the Intrinsic Jitter and Wander Capabilities of the LIU in a typical system application

The Intrinsic Jitter and Wander Test results are summarized in this section.

8.7.1 Intrinsic Jitter Test results

The Intrinsic Jitter Test results for the LIU in DS3 being de-mapped from SONET is summarized below in Table 2.

TABLE 20: SUMMARY OF "CATEGORY I INTRINSIC JITTER TEST RESULTS" FOR SONET/DS3 APPLICATIONS

SCENARIO DESCRIPTION	SCENARIO NUMBER	LIU INTRINSIC JITTER TEST RESULTS	TELCORDIA GR-253-CORE CATEGORY I INTRINSIC JITTER REQUIREMENTS
DS3 De-Mapping Jitter		0.13UI-pp	0.4UI-pp
Single Pointer Adjustment	A1	0.201UI-pp	0.43UI-pp (e.g. 0.13UI-pp + 0.3UI-pp)
Pointer Bursts	A2	0.582UI-pp	1.3UI-pp
Phase Transients	A3	0.526UI-pp	1.2UI-pp
87-3 Pattern	A4	0.790UI-pp	1.0UI-pp
87-3 Add	A5	0.926UI-pp	1.3UI-pp
87-3 Cancel	A5	0.885UI-pp	1.3UI-pp
Continuous Pattern	A4	0.497UI-pp	1.0UI-pp
Continuous Add	A5	0.598UI-pp	1.3UI-pp
Continuous Cancel	A5	0.589UI-pp	1.3UI-pp

NOTES:

1. *A detailed test report on our Test Procedures and Test Results is available and can be obtained by contacting your Exar Sales Representative.*
2. *These test results were obtained via the LIUs mounted on our XRT94L43 12-Channel DS3/E3/STS-1 Mapper Evaluation Board.*
3. *These same results apply to SDH/AU-3 Mapping applications.*

8.7.2 Wander Measurement Test Results

Wander Measurement test results will be provided in the next revision of the LIU Data Sheet.

8.8 Designing with the LIU

In this section, we will discuss the following topics.

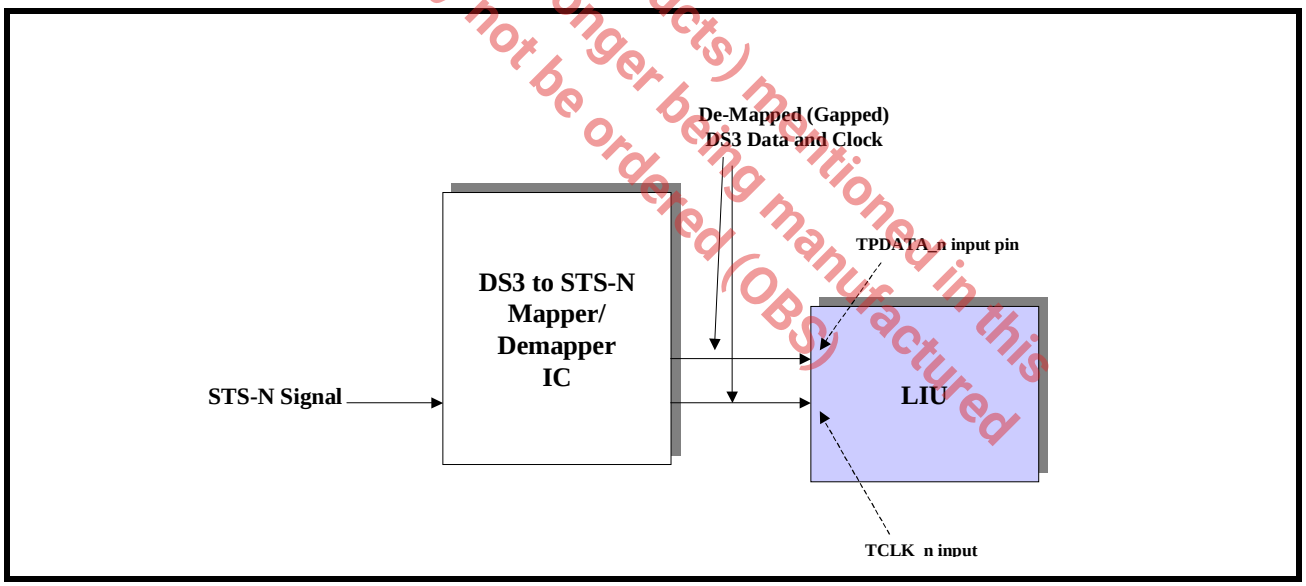
- How to design with and configure the LIU to permit a system to meet the above-mentioned Intrinsic Jitter and Wander requirements.
- How is the LIU able to meet the above-mentioned requirements?
- How does the LIU permits the user to comply with the SONET APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE)?
- How should one configure the LIU, if one needs to support "Daisy-Chain" Testing at the end Customer's site?

8.8.1 How to design and configure the LIU to permit a system to meet the above-mentioned Intrinsic Jitter and Wander requirements

As mentioned earlier, in most application (in which the LIU will be used in a SONET De-Sync Application) the user will typically interface the LIU to a Mapper device in the manner as presented below in Figure 66.

In this application, the Mapper has the responsibility of receiving a SONET STS-N/OC-N signal and extracting as many as N DS3 signals from this signal. As a given channel within the Mapper IC extracts out a given DS3 signal (from SONET) it will typically be applying a Clock and Data signal to the "Transmit Input" of the LIU IC. Figure 66 presents a simple illustration as to how one channel, within the LIU should be connected to the Mapper IC.

FIGURE 66. ILLUSTRATION OF THE LIU BEING CONNECTED TO A MAPPER IC FOR SONET DE-SYNC APPLICATIONS



As mentioned above, the Mapper IC will typically output a Clock and Data signal to the LIU. In many cases, the Mapper IC will output the contents of an entire STS-1 data-stream via the Data Signal to the LIU. However, the Mapper IC typically only supplies a clock pulse via the Clock Signal to the LIU coincident to whenever a DS3 bit is being output via the Data Signal. In this case, the Mapper IC would not supply a clock edge coincident to when a TOH, POH or any non-DS3 data-bit is being output via the Data-Signal.

Figure 66 indicates that the Data Signal from the Mapper device should be connected to the TPDATA_n input pin of the LIU IC and that the Clock Signal from the Mapper device should be connected to the TCLK_n input pin of the LIU IC.

In this application, the LIU has the following responsibilities.

- Using a particular clock edge within the "gapped" clock signal (from the Mapper IC) to sample and latch the value of each DS3 data-bit that is output from the Mapper IC.
- To (through the user of the Jitter Attenuator block) attenuate the jitter within this "DS3 data" and "clock signal" that is output from the Mapper IC.
- To convert this "smoothed" DS3 data and clock into industry-compliant DS3 pulses, and to output these pulses onto the line.

To configure the LIU to operate in the correct mode for this application, the user must execute the following configuration steps.

a. *Configure the LIU to operate in the DS3 Mode*

The user can configure a given channel (within the LIU) to operate in the DS3 Mode, by executing either of the following steps.

- **If the LIU has been configured to operate in the Host Mode**

The user can accomplish this by setting both Bits 2 (E3_n) and Bits 1 (STS-1/DS3*_n), within each of the "Channel Control Registers" to "0" as depicted below.

CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X06
CHANNEL 1 ADDRESS LOCATION = 0X0E
CHANNEL 2 ADDRESS LOCATION = 0X16

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		PRBS Enable Ch_n	RLB_n	LLB_n	E3_n	STS-1/$\overline{DS3}$_n	SR/$\overline{DR}$_n
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

- **If the LIU has been configured to operate in the Hardware Mode**

The user can accomplish this by pulling all of the following input pins "Low".

Pin 76 - E3_0

Pin 94 - E3_1

Pin 85 - E3_2

Pin 72 - STS-1/$\overline{DS3}$_0

Pin 98 - STS-1/$\overline{DS3}$_1

Pin 81 - STS-1/$\overline{DS3}$_2

b. *Configure the LIU to operate in the Single-Rail Mode*

Since the Mapper IC will typically output a single "Data Line" and a "Clock Line" for each DS3 signal that it demaps from the incoming STS-N signal, it is imperative to configure each channel within the LIU to operate in the Single Rail Mode.

The user can accomplish this by executing either of the following steps.

- **If the LIU has been configured to operate in the Host Mode**

The user can accomplish this by setting Bit 0 (SR/DR*), within the each of the "Channel Control" Registers to 1, as illustrated below.

CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X06

CHANNEL 1 ADDRESS LOCATION = 0X0E

CHANNEL 2 ADDRESS LOCATION = 0X16

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		PRBS Enable Ch_n	RLB_n	LLB_n	E3_n	STS-1/ DS3_n	SR/DR_n
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

- **If the LIU has been configured to operate in the Hardware Mode**

Then the user should tie pin 65 (SR/DR*) to "High".

c. *Configure each of the channels within the LIU to operate in the SONET De-Sync Mode*

The user can accomplish this by executing either of the following steps.

- **If the LIU has been configured to operate in the Host Mode.**

Then the user should set Bit D2 (JA0) to "0" and Bit D0 (JA1) to "1", within the Jitter Attenuator Control Register, as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - (CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time DisableCh_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

- **If the LIU has been configured to operate in the Hardware Mode**

Then the user should tie pin 44 (JA0) to a logic "HIGH" and pin 42 (JA1) to a logic "LOW".

Once the user accomplishes either of these steps, then the Jitter Attenuator (within the LIU) will be configured to operate with a very narrow bandwidth.

d. *Configure the Jitter Attenuator (within each of the channels) to operate in the Transmit Direction.*

The user can accomplish this by executing either the following steps.

- **If the LIU has been configured to operate in the Host Mode.**

Then the user should be Bit D1 (JATx/JARx*) to "1", within the Jitter Attenuator Control Register, as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time DisableCh_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

- **If the LIU has been configured to operate in the Hardware Mode.**

Then the user should tie pin 43 (JATx/JARx*) to "1".

e. *Enable the "SONET APS Recovery Time" Mode*

Finally, if the user intends to use the LIU in an Application that is required to reacquire proper SONET and DS3 traffic, prior within 50ms of an APS (Automatic Protection Switching) event (per Telcordia GR-253-CORE), then the user should set Bit 4 (SONET APS Recovery Time Disable), within the "Jitter Attenuator Control" Register, to "0" as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time DisableCh_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

NOTES:

1. *The ability to disable the "SONET APS Recovery Time" mode is only available if the LIU is operating in the Host Mode. If the LIU is operating in the "Hardware" Mode, then this "SONET APS Recovery Time Mode" feature will always be enabled.*
2. *The "SONET APS Recovery Time" mode will be discussed in greater detail in "Section 8.8.3, How does the LIU permit the user to comply with the SONET APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE)?" on page 93.*

8.8.2 Recommendations on Pre-Processing the Gapped Clocks (from the Mapper/ASIC Device) prior to routing this DS3 Clock and Data-Signals to the Transmit Inputs of the LIU

In order to minimize the effects of "Clock-Gapping" Jitter within the DS3 signal that is ultimately transmitted to the DS3 Line (or facility), we recommend that some "pre-processing" of the "Data-Signals" and "Clock-Signals" (which are output from the Mapper device) be implemented prior to routing these signals to the "Transmit Inputs" of the LIU.

8.8.2.1 SOME NOTES PRIOR TO STARTING THIS DISCUSSION:

Our simulation results indicate that Jitter Attenuator PLL (within the LIU LIU IC) will have no problem handling and processing the "Data-Signal" and "Clock-Signal" from a Mapper IC/ASIC if no pre-processing has been performed on these signals. In order words, our simulation results indicate that the Jitter Attenuator PLL (within the LIU IC) will have no problem handling the "worst-case" of 59 consecutive bits of no clock pulses in the "Clock-Signal (due to the Mapper IC processing the TOH bytes, an Incrementing Pointer-Adjustment-induced "stuffed-byte", the POH byte, and the two fixed-stuff bytes within the STS-1 SPE, etc), immediately followed be processing clusters of DS3 data-bits (as shown in Figure 46) and still comply with the "Category I Intrinsic Jitter Requirements per Telcordia GR-253-CORE for DS3 applications.

NOTE: *If this sort of "pre-processing" is already supported by the Mapper device that you are using, then no further action is required by the user.*

8.8.2.2 OUR PRE-PROCESSING RECOMMENDATIONS

For the time-being, we recommend that the customer implement the "pre-processing" of the DS3 "Data-Signal" and "Clock-Signal" as described below. Currently we are aware that some of the Mapper products on the Market do implement this exact "pre-processing" algorithm. However, if the customer is implementing their Mapper Design in an ASIC or FPGA solution, then we strongly recommend that the user implement the necessary logic design to realize the following recommendations.

Some time ago, we spent some time, studying (and then later testing our solution with) the PM5342 OC-3 to DS3 Mapper IC from PMC-Sierra. In particular, we wanted to understand the type of "DS3 Clock" and "Data" signal that this DS3 to OC-3 Mapper IC outputs.

During this effort, we learned the following.

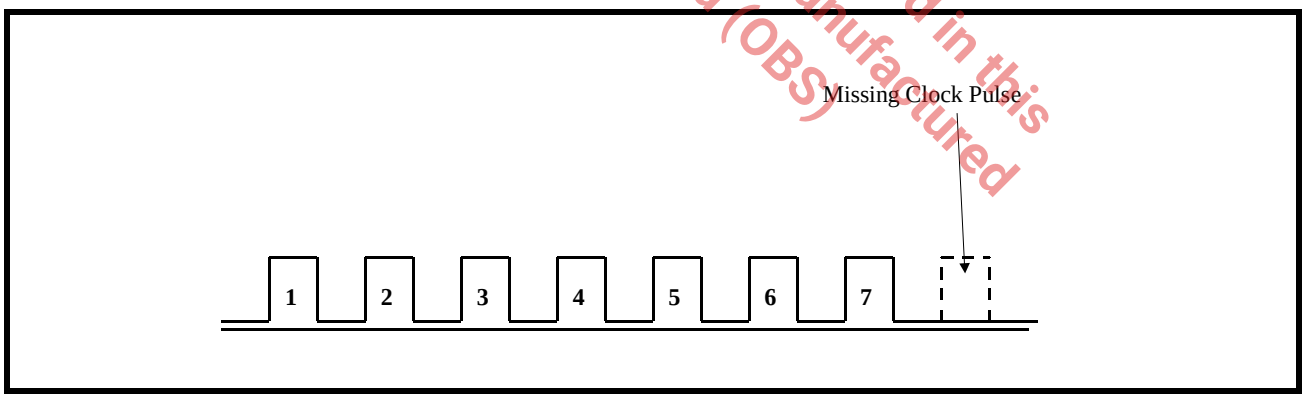
1. This "DS3 Clock" and "Data" signal, which is output from the Mapper IC consists of two major "repeating" patterns (which we will refer to as "MAJOR PATTERN A" and "MAJOR PATTERN B". The behavior of each of these patterns is presented below.

MAJOR PATTERN A

MAJOR PATTERN A consists of two "sub" or minor-patterns, (which we will refer to as "MINOR PATTERN P1 and P2).

MINOR PATTERN P1 consists of a string of seven (7) clock pulses, followed by a single gap (no clock pulse). An illustration of MINOR PATTERN P1 is presented below in Figure 67.

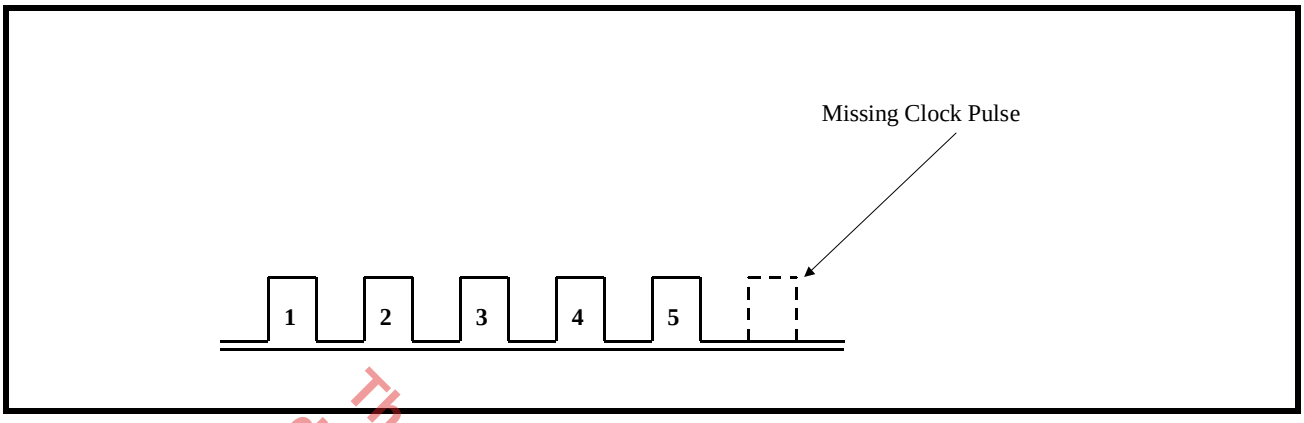
FIGURE 67. ILLUSTRATION OF MINOR PATTERN P1



It should be noted that each of these clock pulses has a period of approximately 19.3ns (or has an "instantaneously frequency of 51.84MHz).

MINOR Pattern P2 consists of string of five (5) clock pulses, which is also followed by a single gap (no clock pulse). An illustration of Pattern P2 is presented below in Figure 68.

FIGURE 68. ILLUSTRATION OF MINOR PATTERN P2



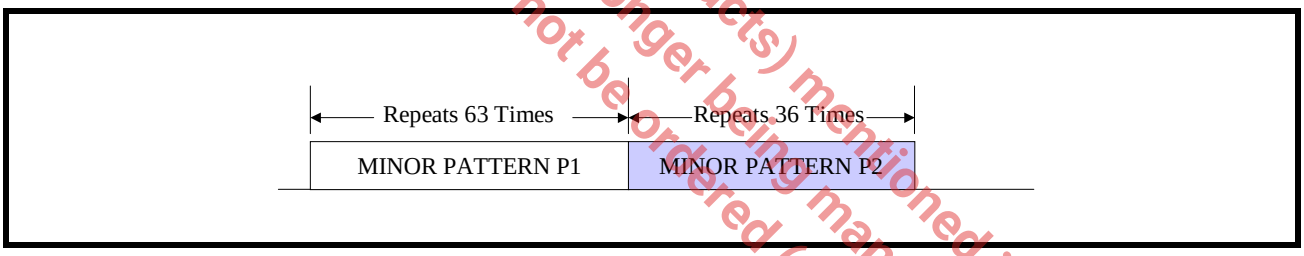
HOW MAJOR PATTERN A IS SYNTHESIZED

MAJOR PATTERN A is created (by the Mapper IC) by:

- Repeating MINOR PATTERN P1 (e.g., 7 clock pulses, followed by a gap) 63 times.
- Upon completion of the 63rd transmission of MINOR PATTERN P1, MINOR PATTERN P2 is transmitted repeatedly 36 times.

Figure 69 presents an illustration which depicts the procedure that is used to synthesize MAJOR PATTERN A

FIGURE 69. ILLUSTRATION OF PROCEDURE WHICH IS USED TO SYNTHESIZE MAJOR PATTERN A



Hence, MAJOR PATTERN A consists of "(63 x 7) + (36 x 5)" = 621 clock pulses. These 621 clock pulses were delivered over a period of "(63 x 8) + (36 x 6)" = 720 STS-1 (or 51.84MHz) clock periods.

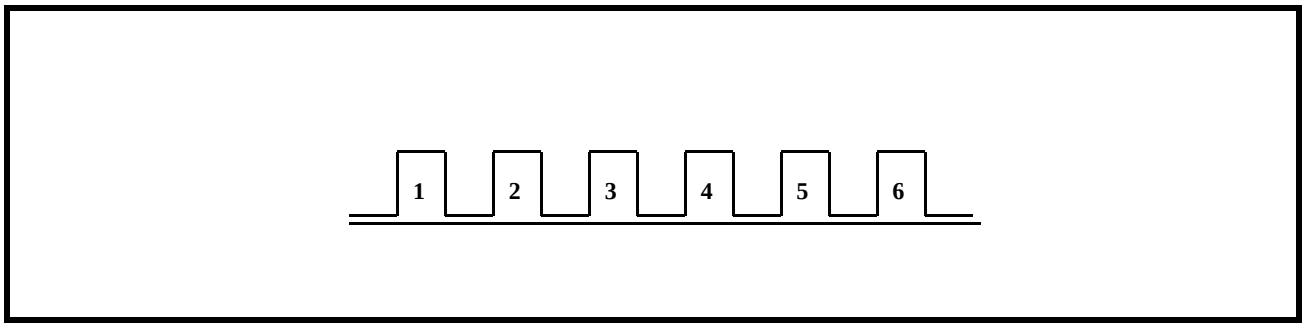
MAJOR PATTERN B

MAJOR PATTERN B consists of three sub or minor-patterns (which we will refer to as "MINOR PATTERNS P1, P2 and P3).

MINOR PATTERN P1, which is used to partially synthesize MAJOR PATTERN B, is exactly the same "MINOR PATTERN P1" as was presented above in Figure 39. Similarly, the MINOR PATTERN P2, which is also used to partially synthesize MAJOR PATTERN B, is exactly the same "MINOR PATTERN P2" as was presented in Figure 40.

MINOR PATTERN P3 (which has yet to be defined) consists of a string of six (6) clock pulses, which contains no gaps. An illustration of MINOR PATTERN P3 is presented below in Figure 70.

FIGURE 70. ILLUSTRATION OF MINOR PATTERN P3



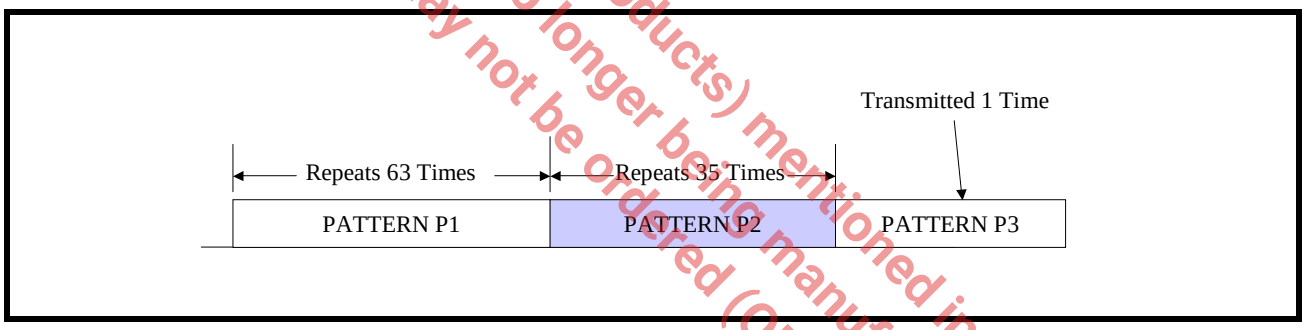
HOW MAJOR PATTERN B IS SYNTHESIZED

MAJOR PATTERN B is created (by the Mapper IC) by:

- Repeating MINOR PATTERN P1 (e.g., 7 clock pulses, followed by a gap) 63 times.
- Upon completion of the 63rd transmission of MINOR PATTERN P1, MINOR PATTERN P2 is transmitted repeatedly 36 times.
- pon completion of the 35th transmission of MINOR PATTERN P2, MINOR PATTERN P3 is transmitted once.

Figure 71 presents an illustration which depicts the procedure that is used to synthesize MAJOR PATTERN B.

FIGURE 71. ILLUSTRATION OF PROCEDURE WHICH IS USED TO SYNTHESIZE PATTERN B



Hence, MAJOR PATTERN B consists of "(63 x 7) + (35 x 5)" + 6 = 622 clock pulses.

These 622 clock pulses were delivered over a period of "(63 x 8) + (35 x 6) + 6 = 720 STS-1 (or 51.84MHz) clock periods.

PUTTING THE PATTERNS TOGETHER

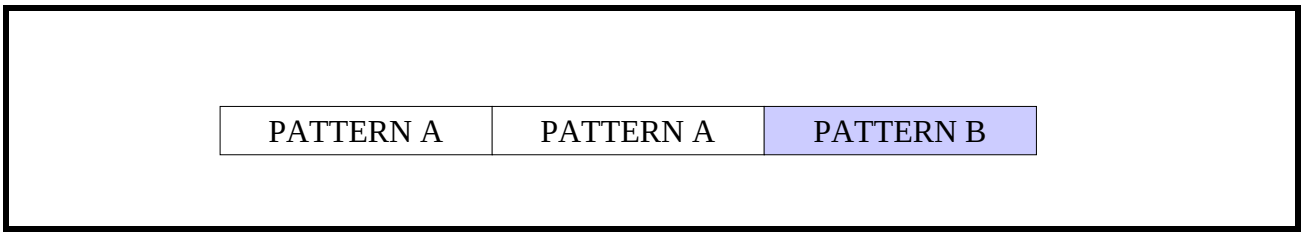
Finally, the DS3 to OC-N Mapper IC clock output is reproduced by doing the following.

- MAJOR PATTERN A is transmitted two times (repeatedly).
- After the second transmission of MAJOR PATTERN A, MAJOR PATTERN B is transmitted once.
- Then the whole process repeats.

Throughout the remainder of this document, we will refer to this particular pattern as the "SUPER PATTERN".

Figure 72 presents an illustration of this "SUPER PATTERN" which is output via the Mapper IC.

FIGURE 72. ILLUSTRATION OF THE SUPER PATTERN WHICH IS OUTPUT VIA THE "OC-N TO DS3" MAPPER IC



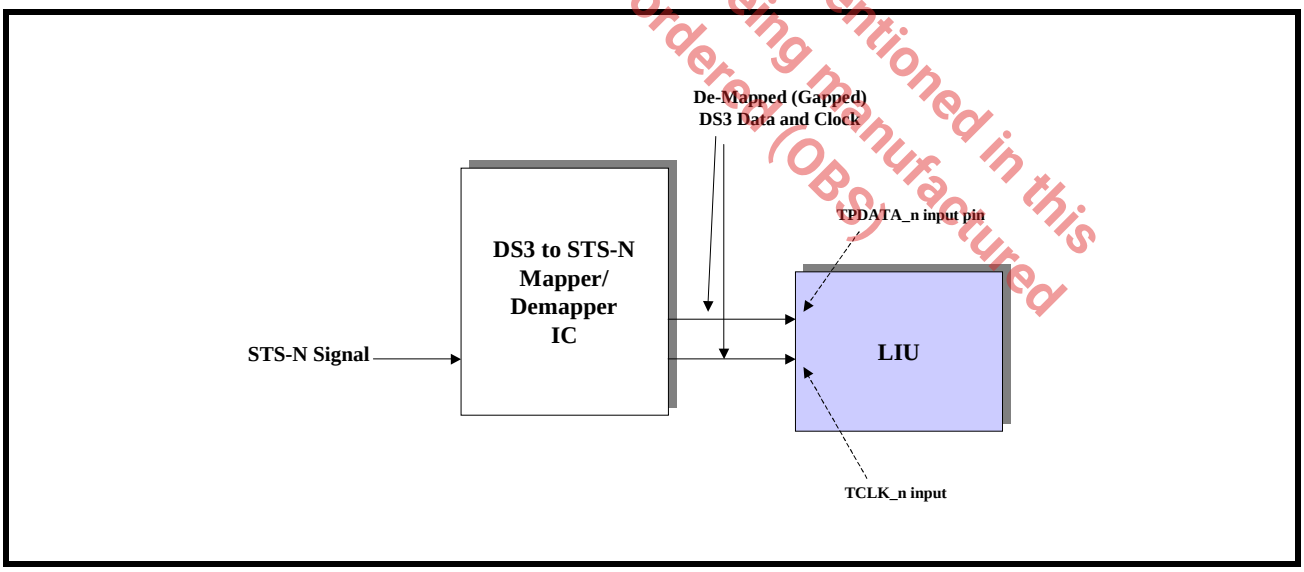
CROSS-CHECKING OUR DATA

- Each SUPER PATTERN consists of (621 + 621 + 622) = 1864 clock pulses.
- The total amount of time, which is required for the "DS3 to OC-N Mapper" IC to transmit this SUPER PATTERN is (720 + 720 + 720) = 2160 "STS-1" clock periods.
- This amount to a period of (2160/51.84MHz) = 41,667ns.
- In a period of 41, 667ns, the LIU (when configured to operate in the DS3 Mode), will output a total (41,667ns x 44,736,000) = 1864 uniformly spaced DS3 clock pulses.
- Hence, the number of clock pulses match.

APPLYING THE SUPER PATTERN TO THE LIU

Whenever the LIU is configured to operate in a "SONET De-Sync" application, the device will accept a continuous string of the above-defined SUPER PATTERN, via the TCLK input pin (along with the corresponding data). The channel within the LIU (which will be configured to operate in the "DS3" Mode) will output a DS3 line signal (to the DS3 facility) that complies with the "Category I Intrinsic Jitter Requirements - per Telcordia GR-253-CORE (for DS3 applications). This scheme is illustrated below in Figure 73.

FIGURE 73. SIMPLE ILLUSTRATION OF THE LIU BEING USED IN A SONET DE-SYNCHRONIZER" APPLICATION



8.8.3 How does the LIU permit the user to comply with the SONET APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE)?

Telcordia GR-253-CORE, Section 5.3.3.3 mandates that the "APS Completion" (or Recovery) time be 50ms or less. Many of our customers interpret this particular requirement as follows.

"From the instant that an APS is initiated on a high-speed SONET signal, all lower-speed SONET traffic (which is being transported via this "high-speed" SONET signal) must be fully restored within 50ms. Similarly, if the "high-speed" SONET signal is transporting some PDH signals (such as DS1 or DS3, etc.), then those entities

that are responsible for acquiring and maintaining DS1 or DS3 frame synchronization (with these DS1 or DS3 data-streams that have been de-mapped from SONET) must have re-acquired DS1 or DS3 frame synchronization within 50ms" after APS has been initiated."

The LIU was designed such that the DS3 signals that it receives from a SONET Mapper device and processes will comply with the Category I Intrinsic Jitter requirements per Telcordia GR-253-CORE.

Reference 1 documents some APS Recovery Time testing, which was performed to verify that the Jitter Attenuator blocks (within the LIU) device that permit it to comply with the Category I Intrinsic Jitter Requirements (for DS3 Applications) per Telcordia GR-253-CORE, do not cause it to fail to comply with the "APS Completion Time" requirements per Section 5.3.3.3 of Telcordia GR-253-CORE. However, Table 3 presents a summary of some APS Recovery Time requirements that were documented within this test report.

Table 3,

TABLE 21: MEASURED APS RECOVERY TIME AS A FUNCTION OF DS3 PPM OFFSET

DS3 PPM OFFSET (PER W&G ANT-20SE)	MEASURED APS RECOVERY TIME (PER LOGIC ANALYZER)
-99 ppm	1.25ms
-40ppm	1.54ms
-30 ppm	1.34ms
-20 ppm	1.49ms
-10 ppm	1.30ms
0 ppm	1.89ms
+10 ppm	1.21ms
+20 ppm	1.64ms
+30 ppm	1.32ms
+40 ppm	1.25ms
+99 ppm	1.35ms

NOTE: *The APS Completion (or Recovery) time requirement is 50ms.*

Configuring the LIU to be able to comply with the SONET APS Recovery Time Requirements of 50ms

Quite simply, the user can configure a given Jitter Attenuator block (associated with a given channel) to (1) comply with the "APS Completion Time" requirements per Telcordia GR-253-CORE, and (2) also comply with the "Category I Intrinsic Jitter Requirements per Telcordia GR-253-CORE (for DS3 applications) by making sure that Bit 4 (SONET APS Recovery Time Disable Ch_n), within the Jitter Attenuator Control Register is set to "0" as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time Disable Ch_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

NOTE: *The user can only disable the "SONET APS Recovery Time Mode" if the LIU is operating in the Host Mode. If the user is operating the LIU in the Hardware Mode, then the user will have NO ability to disable the "SONET APS Recovery Time Mode" feature.*

8.8.4 How should one configure the LIU, if one needs to support "Daisy-Chain" Testing at the end Customer's site?

Daisy-Chain testing is emerging as a new requirements that many of our customers are imposing on our SONET Mapper and LIU products. Many System Designer/Manufacturers are finding out that whenever their end-customers that are evaluating and testing out their systems (in order to determine if they wish to move forward and start purchasing this equipment in volume) are routinely demanding that they be able to test out these systems with a single piece of test equipment. This means that the end-customer would like to take a single piece of DS3 or STS-1 test equipment and (with this test equipment) snake the DS3 or STS-1 traffic (that this test equipment will generate) through many or (preferably all) channels within the system. For example, we have had request from our customers that (on a system that supports OC-192) our silicon be able to support this DS3 or STS-1 traffic snaking through the 192 DS3 or STS-1 ports within this system.

After extensive testing, we have determined that the best approach to complying with test "Daisy-Chain" Testing requirements, is to configure the Jitter Attenuator blocks (within each of the Channels within the LIU) into the "32-Bit" Mode. The user can configure the Jitter Attenuator block (within a given channel of the LIU) to operate in this mode by settings in the table below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time Disable Ch_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	0

REFERENCES

1. TEST REPORT - AUTOMATIC PROTECTION SWITCHING (APS) RECOVERY TIME TESTING WITH THE XRT94L43 DS3/E3/STS-1 TO STS-12 MAPPER IC - Revision C Silicon

9.0 ELECTRICAL CHARACTERISTICS

TABLE 22: ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
V_{DD}	Supply Voltage	-0.5	6.0	V	Note 1
V_{IN}	Input Voltage at any Pin	-0.5	5.5	V	Note 1
I_{IN}	Input current at any pin		100	mA	Note 1
S_{TEMP}	Storage Temperature	-65	150	^0C	Note 1
A_{TEMP}	Ambient Operating Temperature	-40	85	^0C	linear airflow 0 ft./min
Theta JA	Thermal Resistance		23	$^0C/W$	linear air flow 0ft/min (See Note 3 below)
M_{LEVL}	Exposure to Moisture	4		level	EIA/JEDEC JESD22-A112-A
ESD	ESD Rating	2000		V	Note 2

NOTES:

1. *Exposure to or operating near the Min or Max values for extended period may cause permanent failure and impair reliability of the device.*
2. *ESD testing method is per MIL-STD-883D,M-3015.7*
3. *With Linear Air flow of 200 ft/min, reduce Theta JA by 20%, Theta JC is unchanged.*

TABLE 23: DC ELECTRICAL CHARACTERISTICS:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DV_{DD}	Digital Supply Voltage	3.135	3.3	3.465	V
AV_{DD}	Analog Supply Voltage	3.135	3.3	3.465	V
I_{CC}	Supply current requirements		725	850	mA
P_{DD}	Power Dissipation		2.64	2.93	W
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0		5.5	V
V_{OL}	Output Low Voltage, I_{OUT} = - 4mA			0.4	V
V_{OH}	Output High Voltage, I_{OUT} = 4 mA	2.4			V
I_L	Input Leakage Current[1]			±10	µA
C_I	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

NOTES:

1. *Not applicable for pins with pull-up or pull-down resistors.*
2. *The Digital inputs are TTL 5V compliant.*

APPENDIX A

TABLE 24: TRANSFORMER RECOMMENDATIONS

PARAMETER	VALUE
Turns Ratio	1:1
Primary Inductance	40 µH
Isolation Voltage	1500 Vrms
Leakage Inductance	0.6 µH

TABLE 25: TRANSFORMER DETAILS

PART NUMBER	VENDOR	INSULATION	PACKAGE TYPE
PE-68629	PULSE	3000 V	Large Thru-hole
PE-65966	PULSE	1500 V	Small Thru-hole
PE-65967	PULSE	1500 V	SMT
T 3001	PULSE	1500 V	SMT
TG01-0406NS	HALO	1500 V	SMT
TTI 7601-SM	TransPower	1500 V	SMT

TRANSFORMER VENDOR INFORMATION

Pulse
Corporate Office
12220 World Trade Drive
San Diego, CA 92128
Tel: (858)-674-8100
FAX: (858)-674-8262

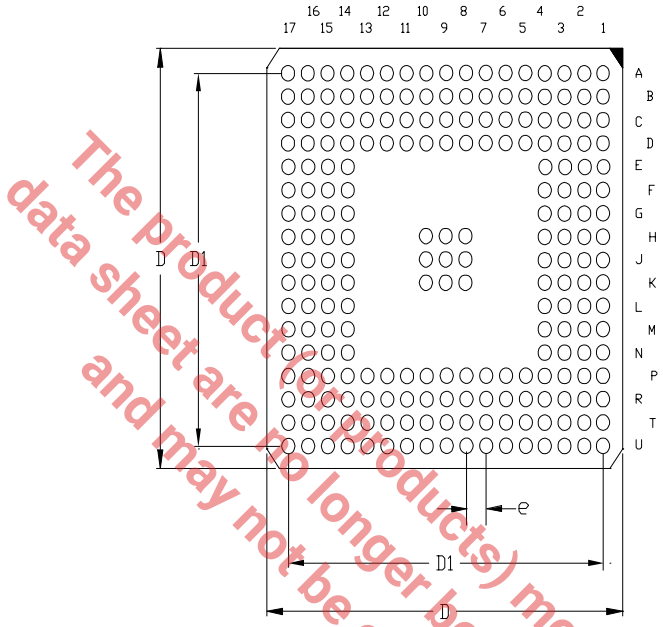
Europe
1 & 2 Huxley Road
The Surrey Research Park
Guildford, Surrey GU2 5RE
United Kingdom
Tel: 44-1483-401700
FAX: 44-1483-401701

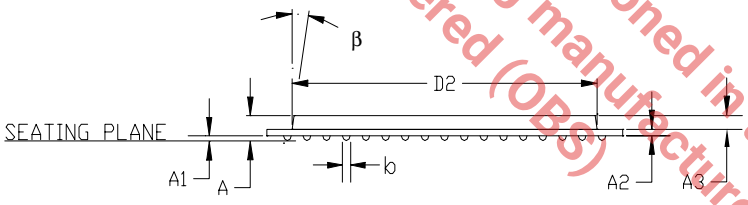
Asia
150 Kampong Ampat
#07-01/02
KA Centre
Singapore 368324
Tel: 65-287-8998
Website: http://www.pulseeng.com
Halo Electronics
Corporate Office
P.O. Box 5826
Redwood City, CA 94063
Tel: (650)568-5800
FAX: (650)568-6165
Email: info@haloelectronics.com
Website: http://www.haloelectronics.com
Transpower Technologies, Inc.
Corporate Office
Park Center West Building
9805 Double R Blvd, Suite # 100
Reno, NV 89511
(800)500-5930 or (775)852-0140
Email: info@trans-power.com
Website: http://www.trans-power.com

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75R06DIB	217 Lead BGA (23 x 23 mm)	- 40°C to + 85°C

PACKAGE DIMENSIONS - 23 X 23 MM 217 LEAD BGA PACKAGE





Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.067	0.098	1.70	2.50
A1	0.016	0.028	0.40	0.70
A2	0.012	0.024	0.30	0.60
A3	0.039	0.047	1.00	1.20
D	0.898	0.913	22.80	23.20
D1	0.800 BSC		20.32 BSC	
D2	0.780	0.795	19.80	20.20
b	0.024	0.035	0.60	0.90
e	0.050 BSC		1.27 BSC	
β	10°	20°	10°	20°

REVISIONS

REVISION	DATE	COMMENTS
P1.0.0	07/15/04	First release of the preliminary datasheet.
.0.0	12/15/04	Release to production. Added data for power supply current and power dissapation.

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Datasheet December 2004.