



MxL86289C

Ethernet PHY

8-Port 2.5 Gigabit Ethernet PHY

MxL86289C

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Ending Validity Date: 2024-12-26 or with the official document release

Preliminary Data Sheet

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Revision 1.2, 2024-05-10

Reference ID 620910

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Revision History

| Current: | Revision 1.2, 2024-05-10 |
|------------------|---|
| Previous: | Revision 1.1, 2023-09-13 |
| Page | Major changes since previous revision |
| 15 | Section 1.1 Features: <ul style="list-style-type: none"> Added USXGMII PHY compliant references. Added 1588 Time Stamp feature list. |
| 22 | Table 3 Abbreviations for Buffer Type: Updated table. |
| 25 | Table 5 USXGMII Interface Signals: Updated URESREF pin type. |
| 31 | Table 10 LED and Debug Interface Signals: Added notes in TDI , TMS and TDO . |
| 36 | Table 11 Miscellaneous Signals: <ul style="list-style-type: none"> Updated description of CLK. Removed HW_UTXD. Removed HW_URXD. |
| 46 | Section 3.2 MDIO Slave Interface: Added MDIO slave section. |
| 49 | Section 3.5.1 Supported Flash Memory Devices: Added section. |
| 53 | Section 3.6.7 RJ45 Tab Up or Tab Down Configuration: Updated description and figure. |
| 57 | Figure 10 LED Connection Options to Ground or Power Supply: Updated figure. |
| 58 | Figure 11 Connection of a Dual Color LED and Configuring Pin Strap Value: Updated figure. |
| 58 | Figure 12 Connection of a Single Color LED and Configuring Pin Strap Value: Updated figure. |
| 59 | Section 3.8.3 LED Brightness Control: Updated description and figure. |
| 60 | Section 3.9.1 PTP Configuration: Added section. |
| 61 | Section 3.10.1 PPS Configuration: Added section. |
| 62 | Section 3.11 Synchronous Ethernet: Updated description. |
| 62 | Section 3.11.1 SyncE Configuration: Added section. |
| 65 | Section 3.14.6 Low-Power State: Updated persistent MDIO register list. |
| 71 | Section 3.15 Firmware Upgrade: Updated description. |
| 77 | Table 26 Register Access Type: Updated table. |
| 78 | Table 27 Registers Overview- Standard Management Registers: Updated reset values of STD_AN_ADV and STD_AN_LPA . |
| 86 | Section 5.1 Standard Management Registers: Updated reset value of Auto-Negotiation Advertisement (Register 0.4) |
| 88 | Section 5.1 Standard Management Registers: Updated reset value of Auto-Negotiation Link Partner Ability (Register 0.5) |
| 101 | Table 28 Registers Overview- PHY-specific Management Registers: Updated reset values of PHY_STAT1 . |
| 102 | Section 5.2 PHY-specific Management Registers: Updated reset value of Physical Layer Status 1 (Register 0.17) and description of FW_MEM . |
| 103 | Section 5.2 PHY-specific Management Registers: Updated description of TXADJ in Physical Layer Control 1 (Register 0.19) . |
| 105 | Section 5.2 PHY-specific Management Registers: Updated description of SDETP in Physical Layer Control 2 (Register 0.20) . |

Revision History

| | |
|------------------|---|
| Current: | Revision 1.2, 2024-05-10 |
| Previous: | Revision 1.1, 2023-09-13 |
| 107 | Section 5.2 PHY-specific Management Registers: Updated description of SEL in Error Counter (Register 0.21) . |
| 114 | Section 5.2 PHY-specific Management Registers: Removed INV , LED3EN , LED2EN , LED3DA and LED2DA in LED Control Register (Register 0.27) . |
| 115 | Section 5.2 PHY-specific Management Registers: Updated Test-Packet Generator Control (Register 0.28) . <ul style="list-style-type: none"> Removed CHSEL. Updated descriptions of IPGL, TYPE and SIZE. |
| 117 | Section 5.2 PHY-specific Management Registers: Updated description of DATA in Test-Packet Generator Data (Register 0.29) . |
| 122 | Table 30 Registers Overview- Standard PMAPMD Registers: Updated reset values of PMA_MGBT_FAST_RETRAIN_STA_CTRL . |
| 138 | Section 6.1 Standard PMAPMD Registers for MMD=0x01: Corrected RMGBT_LRM_ABILITY and RMGBT_CX4_ABILITY type in PMA/PMD Extended Ability (Register 1.11) . |
| 161 | Section 6.1 Standard PMAPMD Registers for MMD=0x01: Updated reset value of MULTIGBASE-T Skew Delay 2 (Register 1.147) |
| 180 | Section 6.2 Standard PCS Registers: Updated description of PCS2G5_PAT_TEST_AB in BASE-R and 10GBASE-T PCS Status 1 (Register 3.32) . |
| 183 | Table 32 Registers Overview- Standard Auto-Negotiation Registers: Updated reset values of ANEG_ADV and ANEG_LP_BP_AB . |
| 194 | Section 6.3 Standard Auto-Negotiation Registers for MMD=0x07: Updated reset value of ANEG Adv. for GPHY (Register 7.16) |
| 195 | Section 6.3 Standard Auto-Negotiation Registers for MMD=0x07: Updated reset value of AN Link Partner Base Page Ability (Register 7.19) |
| 212 | Section 6.4 Vendor Specific 1 Device Registers: Removed Configuration for LED Pin 2 (Register 30.3). |
| 212 | Table 33 Registers Overview- Vendor Specific 1 Device Registers: Updated reset values of VSPEC1_PM_CTRL . |
| 217 | Section 6.4 Vendor Specific 1 Device Registers: Added PHY Transmit Amplitude Control Register (Register 30.8) . |
| 219 | Section 6.4 Vendor Specific 1 Device Registers: Removed MACSEC_CAP in NBASE-T Downshift Status Register (Register 30.11) . |
| 220 | Section 6.4 Vendor Specific 1 Device Registers: Updated Packet Manager Control (Register 30.12) . <ul style="list-style-type: none"> Updated register reset value. Changed PD field to SI. Updated description of USXGMII_REACH. Added PTP_EN, PRE_EMP_EN and PCH_EN. Removed MAC_FREQ_TUNE. Updated description of PM_EN. |
| 222 | Section 6.4 Vendor Specific 1 Device Registers: Updated description of Temperature Code (Register 30.14) . |

Revision History

Current: Revision 1.2, 2024-05-10

Previous: Revision 1.1, 2023-09-13

| | |
|------------|---|
| 223 | Section 6.4 Vendor Specific 1 Device Registers: Updated description of VSPEC1 Interrupt Mask Register (Register 30.17) . <ul style="list-style-type: none"> Removed MCI. Removed PM_LPI. |
| 224 | Section 6.4 Vendor Specific 1 Device Registers: Updated description of VSPEC1 Interrupt Status Register (Register 30.18) . <ul style="list-style-type: none"> Removed MCI. Removed PM_LPI. |
| 237 | Table 35 Absolute Maximum Ratings: Updated Absolute Junction Temperature minimum value and its description. |
| 240 | Table 37 Typical Power Consumption: Updated table. |
| 240 | Table 38 Maximum Power Consumption: Updated maximum power. |
| 241 | Table 39 Maximum Current Per Rail: Updated table. |
| 242 | Section 7.6.1 Digital Interfaces: Added HRSTN. |
| 243 | Table 42 Temperature Sensor Characteristics: Updated description of Temperature Range. |
| 244 | Section 7.7.1 Power Up Sequence: Updated description, figure and table. |
| 246 | Section 7.7.3 Power Supply Rail Requirements: Updated description and table. |
| 250 | Table 47 QSPI Interface Timing Parameters: Updated table. |
| 255 | Table 54 Electrical Characteristics for Common-Mode Rejection and Termination Circuitry: Updated table. |
| 258 | Table 57 JEDEC Thermal Resistance Package Parameter - Compact 2-R Model Network: Added table. |
| 260 | Table 58 Product and Package Naming: Updated table. |

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Table of Contents

| | | |
|----------|---|----|
| | Table of Contents | 7 |
| | List of Figures | 10 |
| | List of Tables | 11 |
| | Preface | 13 |
| 1 | Product Overview | 14 |
| 1.1 | Features | 15 |
| 1.2 | Block Diagram | 18 |
| 2 | External Signals | 19 |
| 2.1 | Logic Symbol | 19 |
| 2.2 | External Signal Description | 20 |
| 2.2.1 | Ball Diagram | 20 |
| 2.2.2 | Abbreviations | 22 |
| 2.2.3 | Input/Output Signals | 23 |
| 2.2.3.1 | Ethernet Twisted Pair Interface | 23 |
| 2.2.3.2 | USXGMII Interface | 25 |
| 2.2.3.3 | MDIO Interface | 26 |
| 2.2.3.4 | QSPI Interface | 27 |
| 2.2.3.5 | I ² C Interface | 29 |
| 2.2.3.6 | Reset Interface | 30 |
| 2.2.3.7 | LED/UART/JTAG Interface | 31 |
| 2.2.3.8 | Miscellaneous Signals | 36 |
| 2.2.3.9 | Power Supply for GPHY | 38 |
| 2.2.3.10 | Power Supply for USXGMII | 40 |
| 2.2.3.11 | Power Supply for TPI (AFE) | 41 |
| 2.2.3.12 | Ground | 42 |
| 3 | Functional Description | 43 |
| 3.1 | Power Supply, Clock, and Reset | 43 |
| 3.1.1 | Power Supply | 43 |
| 3.1.2 | Clock | 43 |
| 3.1.3 | Reset Generation | 43 |
| 3.1.4 | Power-On Sequence | 43 |
| 3.1.5 | Configuration by Pin Strapping | 44 |
| 3.2 | MDIO Slave Interface | 46 |
| 3.3 | Configuration via MDIO Management Interface | 47 |
| 3.4 | I ² C Master Interface | 48 |
| 3.5 | Quad Serial Peripheral Interface | 49 |
| 3.5.1 | Supported Flash Memory Devices | 49 |
| 3.6 | Ethernet PHY Interface | 51 |
| 3.6.1 | Twisted Pair Interface | 51 |
| 3.6.2 | Transformerless Ethernet | 51 |
| 3.6.3 | Auto-Negotiation | 52 |
| 3.6.4 | Auto-Downspeed | 52 |
| 3.6.5 | Polarity Reversal Correction | 52 |
| 3.6.6 | Auto-Crossover Correction | 52 |
| 3.6.7 | RJ45 Tab Up or Tab Down Configuration | 53 |
| 3.6.8 | Wake-on-LAN | 55 |

Table of Contents

| | | |
|----------|---|------------|
| 3.7 | Ethernet SerDes Interface | 56 |
| 3.7.1 | Ethernet SerDes Interface Configuration at Power On | 56 |
| 3.8 | LED Interface | 57 |
| 3.8.1 | LED | 57 |
| 3.8.2 | LED Configuration | 57 |
| 3.8.3 | LED Brightness Control | 59 |
| 3.9 | Precision Time Protocol | 60 |
| 3.9.1 | PTP Configuration | 60 |
| 3.10 | Pulse Per Second | 61 |
| 3.10.1 | PPS Configuration | 61 |
| 3.11 | Synchronous Ethernet | 62 |
| 3.11.1 | SyncE Configuration | 62 |
| 3.12 | Smart-AZ | 62 |
| 3.13 | Preemption | 63 |
| 3.14 | Power Management | 64 |
| 3.14.1 | Power States | 64 |
| 3.14.2 | RESET PWRUP | 64 |
| 3.14.3 | POWER DOWN State | 64 |
| 3.14.4 | SCAN (ANEG) State | 65 |
| 3.14.5 | PING (ANEG) State | 65 |
| 3.14.6 | Low-Power State | 65 |
| 3.14.7 | NORMAL State | 69 |
| 3.14.8 | Low Power IDLE State - Energy-Efficient Ethernet | 70 |
| 3.15 | Firmware Upgrade | 71 |
| 4 | MDIO and MMD Register Interface Description | 72 |
| 4.1 | MDIO-specific Terminology | 72 |
| 4.2 | Register Naming and Numbering | 73 |
| 4.2.1 | Register Numbering | 73 |
| 4.2.2 | Register Naming | 73 |
| 4.2.3 | Examples | 73 |
| 4.3 | MMD Devices Present in MxL86289C | 74 |
| 4.4 | Responsibilities of the STA | 75 |
| 4.5 | MDIO Access Protocols to Read / Write Registers | 76 |
| 5 | MDIO Registers Detailed Description | 77 |
| 5.1 | Standard Management Registers | 78 |
| 5.1.1 | Standard Management Register Descriptions | 79 |
| 5.2 | PHY-specific Management Registers | 101 |
| 5.2.1 | PHY-specific Management Register Descriptions | 102 |
| 6 | MMD Registers Detailed Description | 121 |
| 6.1 | Standard PMAPMD Registers for MMD=0x01 | 122 |
| 6.1.1 | PMAPMD Register Descriptions | 124 |
| 6.2 | Standard PCS Registers | 163 |
| 6.2.1 | PCS Register Descriptions | 164 |
| 6.3 | Standard Auto-Negotiation Registers for MMD=0x07 | 183 |
| 6.3.1 | ANEG Register Descriptions | 184 |
| 6.4 | Vendor Specific 1 Device Registers | 212 |
| 6.4.1 | VSPEC1 Register Descriptions | 213 |
| 6.5 | Vendor Specific 2 Device Registers | 229 |
| 6.5.1 | VSPEC2 Register Descriptions | 230 |
| 7 | Electrical Characteristics | 237 |

Table of Contents

| | | |
|----------|--|------------|
| 7.1 | Absolute Maximum Ratings | 237 |
| 7.2 | Operating Range | 239 |
| 7.3 | Typical Power Consumption | 240 |
| 7.4 | Maximum Thermal Design Power | 240 |
| 7.5 | Maximum Current | 240 |
| 7.6 | DC Characteristics | 242 |
| 7.6.1 | Digital Interfaces | 242 |
| 7.6.2 | Twisted Pair Interface | 242 |
| 7.6.3 | Built-in Temperature Sensor | 243 |
| 7.7 | AC Characteristics | 244 |
| 7.7.1 | Power Up Sequence | 244 |
| 7.7.2 | Input Clock | 246 |
| 7.7.3 | Power Supply Rail Requirements | 246 |
| 7.7.3.1 | V _P AC and DC Power Supply Recommendations | 247 |
| 7.7.3.2 | V _{PH} AC and DC Power Supply Recommendations | 248 |
| 7.7.4 | MDIO Slave Interface | 249 |
| 7.7.5 | Quad Serial Peripheral Interface (QSPI) | 250 |
| 7.7.6 | I ² C Interface | 251 |
| 7.7.7 | JTAG Interface | 252 |
| 7.7.8 | USXGMII Interface Characteristics | 253 |
| 7.7.8.1 | USXGMII Transmit Characteristics | 253 |
| 7.7.8.2 | USXGMII Receive Characteristics | 253 |
| 7.7.9 | Crystal Specification | 254 |
| 7.8 | External Circuitry | 255 |
| 7.8.1 | Twisted-Pair Common-Mode Rejection and Termination Circuitry | 255 |
| 7.8.2 | Transformer (Magnetics) | 256 |
| 7.8.3 | RJ45 Plug | 257 |
| 8 | Package Outline | 258 |
| 9 | Product Ordering Information | 260 |
| | Literature References | 261 |
| | Standards References | 261 |
| | Terminology | 262 |

List of Figures

| | | |
|-----------|---|-----|
| Figure 1 | MxL86289C Block Diagram | 18 |
| Figure 2 | MxL86289C External Signal Overview | 19 |
| Figure 3 | Ball Diagram for PG-FCLBGA-256 (Top View). | 21 |
| Figure 4 | MDIO Slave | 46 |
| Figure 5 | MDIO Access Timing | 47 |
| Figure 6 | Twisted-Pair Interface of MxL86289C Including Transformer and RJ45 Plug | 51 |
| Figure 7 | External Circuitry for the Transformerless Ethernet Application | 51 |
| Figure 8 | RJ45 Tab Up or Tab Down Configuration. | 54 |
| Figure 9 | WoL Application Block Diagram | 55 |
| Figure 10 | LED Connection Options to Ground or Power Supply | 57 |
| Figure 11 | Connection of a Dual Color LED and Configuring Pin Strap Value | 58 |
| Figure 12 | Connection of a Single Color LED and Configuring Pin Strap Value | 58 |
| Figure 13 | LED Brightness Control by Controlling LED Output Enable/Disable | 59 |
| Figure 14 | State Diagram for Power Down State Management. | 64 |
| Figure 15 | Low Power Sequence. | 66 |
| Figure 16 | EEE Low Power Idle Sequence | 70 |
| Figure 17 | Input/Output Waveform for AC Tests | 244 |
| Figure 18 | Timing Diagram for the Reset Sequence | 245 |
| Figure 19 | DC and AC Characteristics for V_P Supply. | 247 |
| Figure 20 | DC and AC Characteristics for V_{PH} Supply. | 248 |
| Figure 21 | Timing Diagram for the MDIO Slave Interface | 249 |
| Figure 22 | QSPI Master Interface Timing | 250 |
| Figure 23 | I ² C Timing. | 251 |
| Figure 24 | Test Interface Timing | 252 |
| Figure 25 | Twisted Pair Common-Mode Rejection and Termination Circuitry. | 255 |
| Figure 26 | Schematic of an Ethernet Transformer Device. | 256 |
| Figure 27 | PG-FCLBGA-256 13 mm x 13 mm Package Outline | 259 |

List of Tables

| | | |
|----------|--|-----|
| Table 1 | Ball Diagram Color Codes | 20 |
| Table 2 | Abbreviations for Pin Type | 22 |
| Table 3 | Abbreviations for Buffer Type | 22 |
| Table 4 | Ethernet Twisted Pair Interface Signals | 23 |
| Table 5 | USXGMII Interface Signals | 25 |
| Table 6 | MDIO Management Interface Signals | 26 |
| Table 7 | QSPI Management Interface Signals | 27 |
| Table 8 | I ² C Management Interface Signals | 29 |
| Table 9 | Reset Signals | 30 |
| Table 10 | LED and Debug Interface Signals | 31 |
| Table 11 | Miscellaneous Signals | 36 |
| Table 12 | Power Supply Pins for GPHY | 38 |
| Table 13 | Power Supply Pins for USXGMII | 40 |
| Table 14 | Power Supply Pins for TPI (AFE) | 41 |
| Table 15 | Ground Pins | 42 |
| Table 16 | Pin Names Used for Pin Strapping | 44 |
| Table 17 | Pin Strapping Configuration Description | 44 |
| Table 18 | MDIO Ready Timing | 47 |
| Table 19 | Supported Flash Memory Devices | 49 |
| Table 20 | Flash command and timing | 50 |
| Table 21 | Supported Twisted Pair Mappings on a Cat 5 or Better Cable | 53 |
| Table 22 | Programming Sequence for the Wake-on-LAN Functionality | 55 |
| Table 23 | Ethernet SerDes Interface Feature List | 56 |
| Table 24 | Low Power State Entry and Exit Sequence | 67 |
| Table 25 | MDIO/MMD Devices Present in MxL86289C | 74 |
| Table 26 | Register Access Type | 77 |
| Table 27 | Registers Overview- Standard Management Registers | 78 |
| Table 28 | Registers Overview- PHY-specific Management Registers | 101 |
| Table 29 | Register Access Type | 121 |
| Table 30 | Registers Overview- Standard PMAPMD Registers | 122 |
| Table 31 | Registers Overview- Standard PCS Registers | 163 |
| Table 32 | Registers Overview- Standard Auto-Negotiation Registers | 183 |
| Table 33 | Registers Overview- Vendor Specific 1 Device Registers | 212 |
| Table 34 | Registers Overview- Vendor Specific 2 Device Registers | 229 |
| Table 35 | Absolute Maximum Ratings | 237 |
| Table 36 | Operating Range | 239 |
| Table 37 | Typical Power Consumption | 240 |
| Table 38 | Maximum Power Consumption | 240 |
| Table 39 | Maximum Current Per Rail | 241 |
| Table 40 | DC Characteristics of the GPIO Interfaces (VDDP = 3.3 V) | 242 |
| Table 41 | DC Characteristics of the GPIO Interfaces (VDDP = 1.8 V) | 242 |
| Table 42 | Temperature Sensor Characteristics | 243 |
| Table 43 | Power Supply Timings | 245 |
| Table 44 | AC Characteristics of Input Clock on XTAL1 Pin | 246 |
| Table 45 | AC Characteristics of the Power Supply | 246 |
| Table 46 | Timing Characteristics of the MDIO Slave Interface | 249 |
| Table 47 | QSPI Interface Timing Parameters | 250 |
| Table 48 | I ² C Timing | 251 |
| Table 49 | Test Interface Clock | 252 |

List of Tables

| | | |
|----------|--|-----|
| Table 50 | JTAG Timing | 252 |
| Table 51 | Transmit Characteristics of the USXGMII | 253 |
| Table 52 | Receive Characteristics of the USXGMII | 253 |
| Table 53 | Specification of the Crystal | 254 |
| Table 54 | Electrical Characteristics for Common-Mode Rejection and Termination Circuitry | 255 |
| Table 55 | Electrical Characteristics for Supported Transformers (Magnetics) | 256 |
| Table 56 | Electrical Characteristics for Supported RJ45 Plugs | 257 |
| Table 57 | JEDEC Thermal Resistance Package Parameter - Compact 2-R Model Network | 258 |
| Table 58 | Product and Package Naming | 260 |

Preface

This Preliminary Data Sheet describes the features and system architecture of the Ethernet PHY MxL86289C, which is an 8-Port 2.5 Gigabit Ethernet PHY.

Document Conventions

In the interest of brevity, this document uses short names to represent full product names.

MxL86289C Ethernet PHY MxL86289C

Document Information

This document's identifying information is:

Document Reference (Citation) Name

Ethernet PHY MxL86289C Preliminary Data Sheet Revision 1.2

File Name

620910_MxL86289C_Prel_DS_Rev1.2.pdf

Organization of this Document

- **Chapter 1, Product Overview**
This chapter provides an overview of the MxL86289C.
- **Chapter 2, External Signals**
This chapter provides a pinout of the MxL86289C device package.
- **Chapter 3, Functional Description**
This chapter provides the functional description for the MxL86289C.
- **Chapter 4, MDIO and MMD Register Interface Description**
This chapter describes the MDIO and MMD registers available to support the MxL86289C feature set.
- **Chapter 5, MDIO Registers Detailed Description**
This chapter describes the fields and reset values of the MDIO registers.
- **Chapter 6, MMD Registers Detailed Description**
This chapter describes the fields and reset values of the MMD registers.
- **Chapter 7, Electrical Characteristics**
This chapter provides the electrical characteristics for the MxL86289C.
- **Chapter 8, Package Outline**
This chapter provides a package outline for the MxL86289C.
- **Chapter 9, Product Ordering Information**
This chapter provides the product ordering details for the MxL86289C.
- **Standards References**

1 Product Overview

The MxL86289C device is a low power multi-port Ethernet PHY transceiver integrated circuit with two 10G Ethernet SerDes interfaces. The MxL86289C has eight integrated Ethernet BASE-T PHYs which support four data rates: 2500, 1000, 100, and 10 Mbps.

On the Ethernet Twisted Pair Interface (TPI), the MxL86289C is compliant with the standards from IEEE 802.3 referenced in [3]:

- 2.5GBASE-T (IEEE 802.3 Clause 126, NBASE-T)
- 1000BASE-T (IEEE 802.3 Clause 40)
- 100BASE-TX (IEEE 802.3 Clause 25)
- 10BASE-Te (IEEE 802.3 Clause 14)

This interface supports the Energy-Efficient Ethernet (EEE) feature to reduce idle mode power consumption. Power saving at the system level is also possible with the wake-on-LAN feature. A low-EMI line driver with integrated termination facilitates the PCB design.

With reference to the Open System Interconnection (OSI) model, the MxL86289C implements eight layer 1 physical media access devices, and each is connected to a layer 2 MAC using a SerDes data interface, and an MDIO management interface.

The MxL86289C provides two Ethernet SerDes data interfaces to connect to a MAC processor with multi-port (4 x 2.5G) USXGMII interface using an MDIO slave interface for management.

The MxL86289C supports the Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE).

The MxL86289C supports a standard MDIO management interface as defined in IEEE 802.3 Clause 22 and Clause 45 [3]. The MDIO serial interface is operable with a clock running up to 25 MHz. It allows a management entity (the external chip implementing the MAC) to access standard MDIO/MMD registers to control the MxL86289C's behavior, or to read the link status. The MxL86289C is also configurable via pin strapping.

The MxL86289C is capable of driving up to 16 LEDs (two per BASE-T port). Each LED is independently programmable to indicate the link speed and traffic activities. Several indication schemes are selectable.

External supplies of 0.8 V, 1.2 V, 1.8 V, and 3.3 V are required to power the MxL86289C device.

The MxL86289C uses a ball grid array package (type BGA 16 x16 matrix, size 13 mm x 13 mm).

1.1 Features

This section provides an overview of the features supported by the MxL86289C.

Communication Interfaces

- The eight Ethernet BASE-T interfaces support:
 - Ethernet modes and standards
2.5GBASE-T (IEEE 802.3, NBASE-T), 1000BASE-T (IEEE 802.3), 100BASE-TX (IEEE 802.3), and 10BASE-T_e (IEEE 802.3)
 - Ethernet twisted pair copper cable of category Cat5 or higher
 - Low EMI voltage mode line driver with integrated termination resistors
 - Transformerless Ethernet for backplane applications
 - Auto-Negotiation (ANEG) with extended next page support
 - Auto-MDIX and polarity correction
 - Auto-Downspeed (ADS)
 - 100BASE-TX EEE, 1000BASE-T EEE, 2.5GBASE-T EEE, and power down mode
 - Cable diagnostics: cable open/short detection and cable length estimation
 - Wake-on-LAN (WoL)
 - Precision Time Stamping (PTS), implementing standard IEEE 1588v2
 - Jumbo frames of up to 10 kB
- Two Ethernet SerDes interfaces, where each interface supports:
 - 10G-USXGMII
 - The PHY complies with all of the required features specified in the Cisco USXGMII Multiport Copper PHY Specification [8] and Cisco USXGMII Single-port Copper PHY Specification [9]
 - Back channel equalization, auto-negotiation, Forward Error Correction (FEC)
 - Clock and Data Recovery (CDR), no clock forwarding required
 - Clause 37 auto-negotiation
 - Packet Control Header (PCH) over Preamble
- The management interface supports the communication between the Station Manager (STA, per IEEE 802.3) and the MxL86289C using:
 - A Management Data Input/Output (MDIO) slave interface providing access to the standard registers in the MMD
 - An MDIO interface clock of up to 25 MHz
 - 3 MDIO message frame types as described in IEEE 802.3: Clause 22, Clause 22 Extended, and Clause 45 [3]
- The Quad SPI master interface connecting to serial external Quad-SPI flash memory supports:
 - Programmable interface clock: maximum 101 MHz
 - Internal firmware code access from external Quad-SPI flash memory
 - Write access to the Quad-SPI flash memory
 - Different Quad-SPI flash memory sizes up to 512 MB
 - Secure firmware upgrade of the flash memory
- One instance of the I²C master interface controlling external devices supports these speed modes:
 - Standard mode (<100 Kbps)
 - Fast mode (<400 Kbps)
 - Fast mode plus (<1000 Kbps)
 - High speed mode (<3.4 Mbps)
- The JTAG interface supports:
 - Boundary scan
 - Test and debug interface
 - Shared pins with GPIO functions
- The LED interface supports:
 - Programmable LED

- Up to two LEDs per BASE-T port
- Single and dual color LEDs
- Connection of LED to ground or 3.3 V
- Several LED indication schemes (link/activity, duplex/collision, and link speed)
- Configuration of LED indication via MDIO registers
- Control of LED brightness via software driver API
- Alternative configuration of LED pins as GPIO for custom indication
- Supports two external interrupts:
 - Configurable as output to an external controller
 - Configurable as input from external device(s)
 - Configurable edge, level, and polarity

Flash and Flashless Mode

- In flash mode, an external QSPI memory device is required to store the firmware
- In flashless mode, the firmware is downloaded from a host MAC SoC via the MDIO interface:
 - Broadcast firmware download support
 - Secure firmware download

Clocking, Timing, and Time Stamping Features

- The input reference clock options are:
 - 25 MHz crystal operation
 - 25 MHz direct from an external oscillator
 - An external CML/LVPECL reference clock operating at 50 MHz or 156.25 MHz
- SyncE, implementing standard ITU-T G.8262/Y.1362
- PTP, according to standard IEEE 1588v2
- Four general purpose clock pins GPC0, GPC1, GPC2, and GPC3 shared with GPIO for several usage options, configurable by API:
 - To input or output the Synchronous Ethernet reference clock SyncE: 2.048 MHz, 1.544 MHz
 - To input or output the precise time stamping signals (PTP)
 - To output the pulse per second signal (PPS)

1588 Time Stamp

- Ethernet packet time stamping as IEEE 1588 (v1 and v2) and IEEE 802.1AS-REV
- PTP over Ethernet and PTP over UDP over IPv4/IPv6
- It is possible to adjust time and frequency of the system reference time.
- Auxiliary time stamp snapshot for the time synchronization with other chips via the GPIO type signal
- 1 pulse per second (PPS) output programmable for start, stop, pulse width, and interval
- 1-step time stamping in Tx direction
- 2-step time stamp (16-entries in FIFO per Ethernet port) in Tx direction

Synchronous Ethernet (SyncE)

- Synchronous Ethernet according to ITU-T G.8262/Y.1362.
- Supports EEC-1 (2.048 MHz), EEC-2 (1.544 MHz), and 8 kHz reference clock input.
- Supports regeneration of these reference clocks as output.

Preemption

- Recognize preemption packet types defined in IEEE 802.3br.
- Forwarding of preemption packets
- PCH support of preemption packets

Other Features

- Temperature Sensor (warning, interrupt, reset and auto-downspeed)

Power Supply

- 3.3 V, 1.8 V, 1.2 V, and 0.8 V external power sources

1.2 Block Diagram

Figure 1 shows the block diagram of the MxL86289C. The main interfaces are:

- Data interface to SoC/MAC processor, using USXGMII
- Slave control interface driven by a SoC/MAC processor, using MDIO slave
- Master control interface using I²C master
- Interrupt signal MDINT allowing the MxL86289C to notify the SoC/MAC processor about a change of status
- LED control
- Twisted pair interfaces (TPI)
- Master Quad Serial Peripheral Interface (QSPI) interface

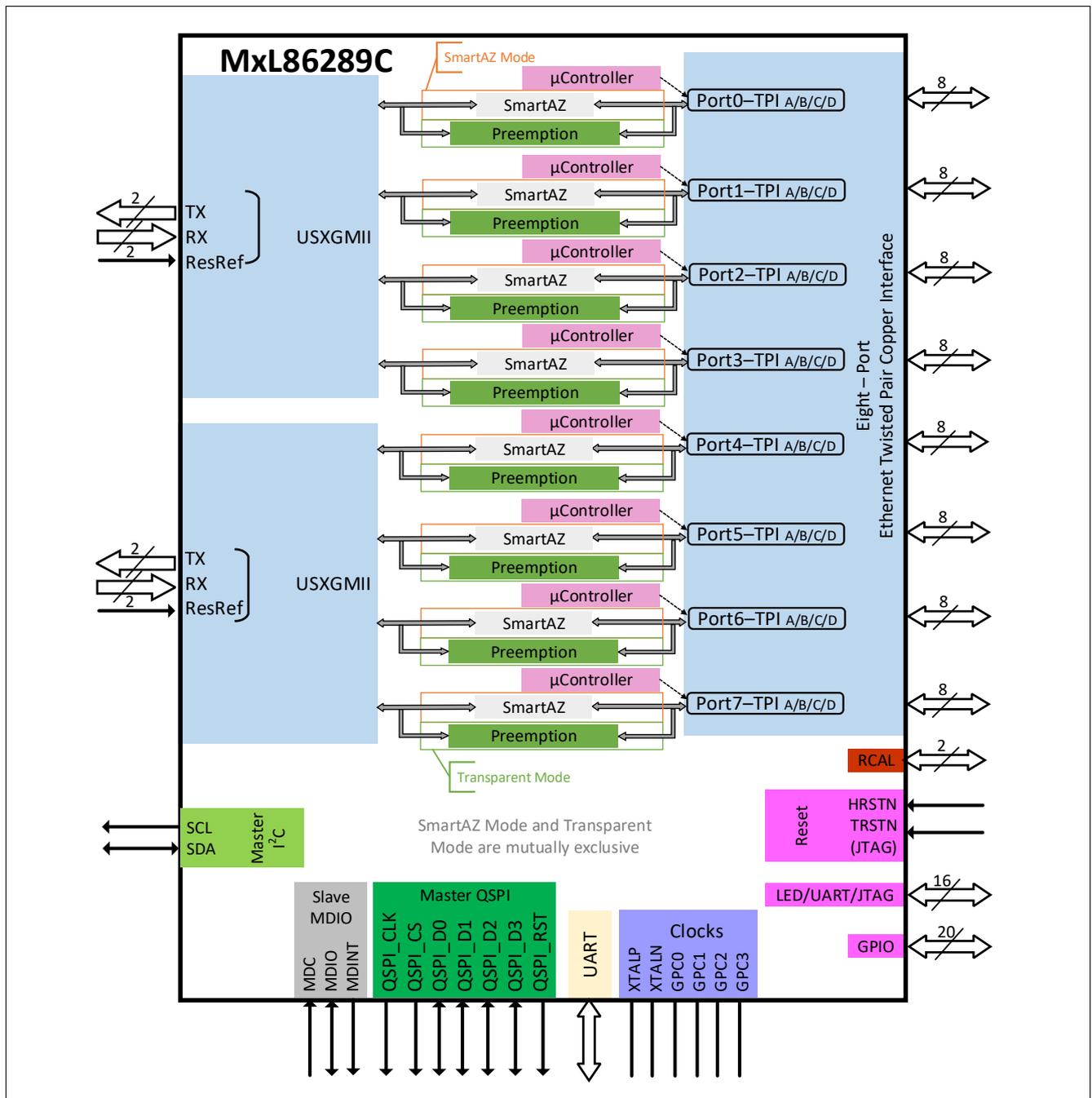


Figure 1 MxL86289C Block Diagram

2 External Signals

This chapter describes the signal mapping to the package.

2.1 Logic Symbol

Figure 2 gives an overview of the device's external interfaces.

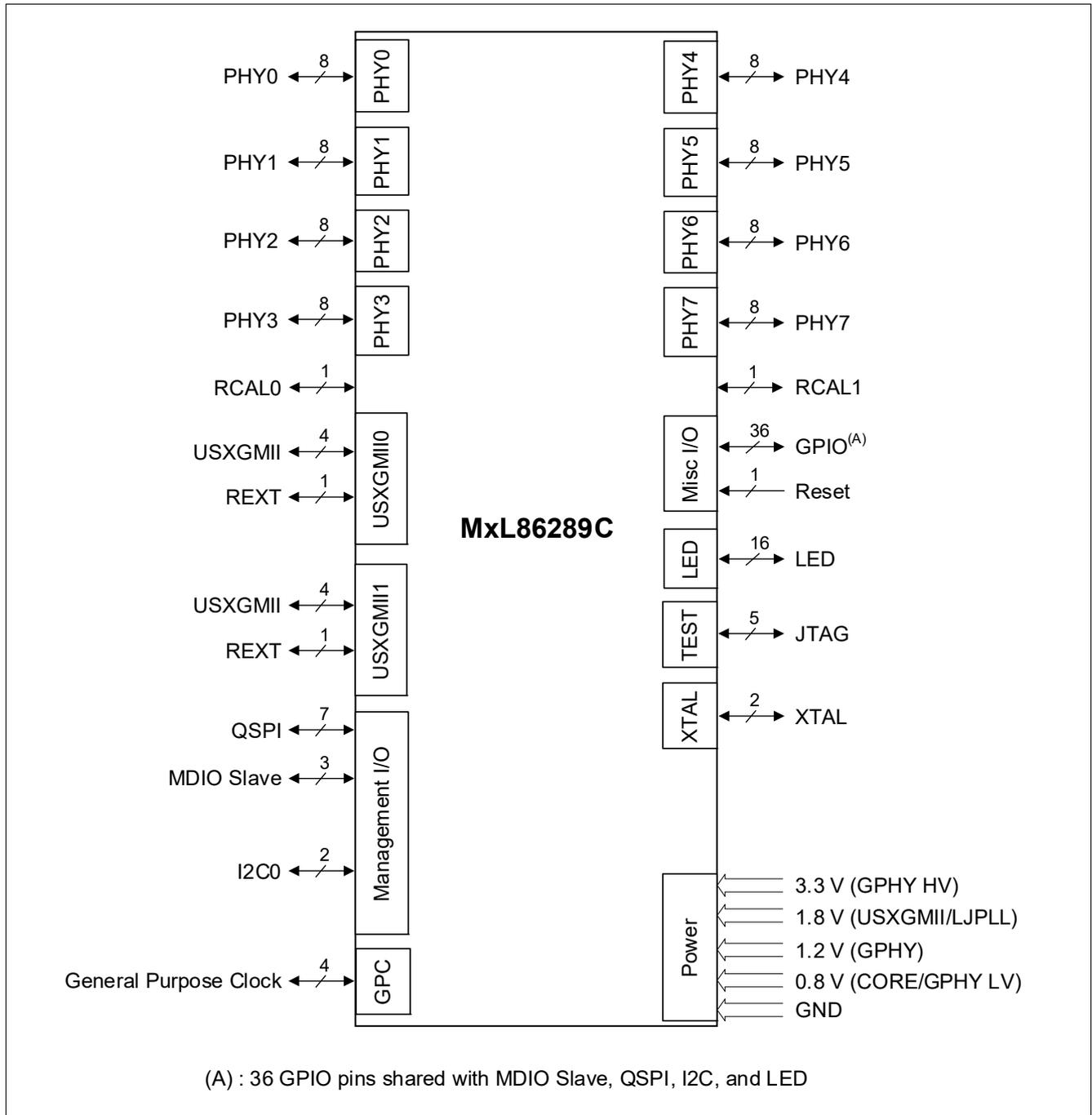


Figure 2 MxL86289C External Signal Overview

2.2 External Signal Description

This section provides the ball diagram, abbreviations for pin types and buffer types, and the table of input and output signals.

2.2.1 Ball Diagram

Figure 3 shows the ball diagram. **Table 1** lists the ball diagram color codes.

Table 1 Ball Diagram Color Codes

| Color | Description |
|-------------|--------------------------------|
| Red | Power |
| Light Red | USXGMII Power |
| Orange | MDIO, I ² C Signals |
| Grey | Ground |
| Blue | TPI-related Signals |
| Pink | QSPI, Reset Signals |
| Yellow | USXGMI Signals |
| Light Green | Clock, GPIO Signals |
| Light Blue | LED, JTAG Signals |

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|------------|------------|--------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|----------------|---------------|---------------|----------|----------|------------|---|
| A | TPVS SA_0 | TPBP _3 | TPAP _3 | TPDP _2 | TPCP _2 | TPBP _2 | TPAP _2 | TPDP _1 | TPCP _1 | TPBP _1 | TPAP _1 | TPDP _0 | TPCP _0 | TPBP _0 | TPAP _0 | TPVS SA_0 | A |
| B | TPCP _3 | TPBN _3 | TPAN _3 | TPDN _2 | TPCN _2 | TPBN _2 | TPAN _2 | TPDN _1 | TPCN _1 | TPBN _1 | TPAN _1 | TPDN _0 | TPCN _0 | TPBN _0 | TPAN _0 | URES REF_0 | B |
| C | TPDP _3 | TPCN _3 | TPVS SA_0 | TPVS SA_0 | VDD A3V3 _3 | TPVS SA_0 | VDD A3V3 _2 | TPVS SA_0 | VDD A3V3 _1 | TPVS SA_0 | VDD A3V3 _0 | TPVS SA_0 | TPVS SA_0 | UVSS | UVSS | URX M_0 | C |
| D | TPVS SA_0 | TPDN _3 | VDD3 V3PA D0 | TPVS SA_0 | TPVS SA_0 | RCA L_0 | VDD A1V8 _0 | VDD A1V8 _0 | VDD A1V2 CDB0 | VDD A1V2 CDB0 | TPVS SA_0 | VDD3 V3PA D1 | VA0V 8_0 | VA0V 8_0 | URXP _0 | UVSS | D |
| E | PHYL ED1_0 | TPVS SA_0 | VDD3 V3PA D0 | TPVS SA_0 | TPVS SA_0 | VDD A0V8 _0 | TPVS SA_0 | VDD A0V8 _0 | TPVS SA_0 | TPVS SA_0 | VDD A0V8 _0 | VSSD | VPHA 1V8_0 | UVSS | UTXM _0 | UTXP _0 | E |
| F | PHYL ED1_1 | PHYL ED2_1 | PHYL ED2_0 | VDD D0V8 _COR | VSSD | VDD D0V8 REF | GPC0 | GPC2 | VSS_XO | VSS_XO | F |
| G | PHYL ED1_2 | PHYL ED2_2 | HRSTN | VDD D0V8 _COR | VSSD | VDD D0V8 _COR | VSSD | VDD D0V8 _COR | VSSD | VDD D0V8 _COR | VDD D0V8 POST | VSS_XO | GPC1 | VSSD | XTAL2 | XTAL1 | G |
| H | PHYL ED1_3 | PHYL ED2_3 | GPIO1 | VSSD | VDD D0V8 _COR | VSSD | VDD D0V8 _COR | VSSD | VDD D0V8 _COR | VSSD | VDD A1V8 PORXO | VCC1 V8_O TP | VDDP _PAD | QSPI_D3 | QSPI_RST | QSPI_CS | H |
| J | PHYL ED1_4 | PHYL ED2_4 | GPIO2 | VSSD | VDD D0V8 _COR | VSSD | VDD D0V8 _COR | VSSD | VDD D0V8 _COR | VSSD | VDD A1V8 _PLL | VSSD | GPC3 | QSPI_D1 | QSPI_D2 | QSPI_CLK | J |
| K | PHYL ED1_5 | PHYL ED2_5 | GPIO3 | VDD D0V8 _COR | VSSD | VDD A1V8 _PVT | VDD A1V8 DA_0 | QSPI_D0 | MDIO _S | MDC _S | K |
| L | PHYL ED1_6 | PHYL ED2_6 | PHYL ED2_7 | VDD D0V8 _COR | VSSD | I2C_S CL_0 | VSSD | MDINT | GPIO0 | VSSD | L |
| M | PHYL ED1_7 | TRSTN | VSSD | TPVS SA_1 | TPVS SA_1 | VDD A0V8 _1 | TPVS SA_1 | VDD A0V8 _1 | TPVS SA_1 | TPVS SA_1 | VDD A0V8 _1 | VSSD | VPHA 1V8_1 | UVSS | UTXM _1 | UTXP _1 | M |
| N | TPVS SA_1 | TPAP _4 | VDD3 V3PA D0 | TPVS SA_1 | TPVS SA_1 | RCA L_1 | VDD A1V8 _1 | VDD A1V8 _1 | VDD A1V2 CDB1 | VDD A1V2 CDB1 | TPVS SA_1 | VDD3 V3PA D1 | VA0V 8_1 | VA0V 8_1 | URXP _1 | UVSS | N |
| P | TPAN _4 | TPBP _4 | TPVS SA_1 | TPVS SA_1 | VDD A3V3 _4 | TPVS SA_1 | VDD A3V3 _5 | TPVS SA_1 | VDD A3V3 _6 | TPVS SA_1 | VDD A3V3 _7 | TPVS SA_1 | TPVS SA_1 | UVSS | UVSS | URX M_1 | P |
| R | TPBN _4 | TPCP _4 | TPDP _4 | TPAP _5 | TPBP _5 | TPCP _5 | TPDP _5 | TPAP _6 | TPBP _6 | TPCP _6 | TPDP _6 | TPAP _7 | TPBP _7 | TPCP _7 | TPDP _7 | URES REF_1 | R |
| T | TPVS SA_1 | TPCN _4 | TPDN _4 | TPAN _5 | TPBN _5 | TPCN _5 | TPDN _5 | TPAN _6 | TPBN _6 | TPCN _6 | TPDN _6 | TPAN _7 | TPBN _7 | TPCN _7 | TPDN _7 | TPVS SA_1 | T |

Figure 3 Ball Diagram for PG-FCLBGA-256 (Top View)

2.2.2 Abbreviations

Table 2 and **Table 3** summarize the abbreviations used in the signal tables.

Table 2 Abbreviations for Pin Type

| Abbreviations | Description |
|---------------|--|
| I | Input-only, digital levels |
| O | Output-only, digital levels |
| I/O | Bidirectional input/output signal, digital levels |
| Prg | Bidirectional pin, programmable to operate either as input or output, digital levels |
| AI | Input-only, analog levels |
| AO | Output-only, analog levels |
| AI/AO | Bidirectional, analog levels |
| PWR | Power |
| GND | Ground |

Table 3 Abbreviations for Buffer Type

| Abbreviations | Description |
|---------------|--|
| A | Analog characteristics, see the AC/DC specification for more information. |
| Prg | Programmable (open-drain/push-pull, pull-up/pull-down characteristic are programmable) |
| PU | Pull up (internal, weak) |

2.2.3 Input/Output Signals

Table 4 to Table 15 provide a detailed description of all the pins.

2.2.3.1 Ethernet Twisted Pair Interface

Unused TPI signals must be unconnected.

Table 4 Ethernet Twisted Pair Interface Signals

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|--------|----------|-------------|--|
| Ethernet Port Twisted Pair Interface | | | | |
| A15 | TPAP_0 | AI/AO | A | Port 0 Transmit/Receive Positive/Negative |
| B15 | TPAN_0 | AI/AO | A | |
| A14 | TPBP_0 | AI/AO | A | |
| B14 | TPBN_0 | AI/AO | A | |
| A13 | TPCP_0 | AI/AO | A | |
| B13 | TPCN_0 | AI/AO | A | |
| A12 | TPDP_0 | AI/AO | A | |
| B12 | TPDN_0 | AI/AO | A | |
| A11 | TPAP_1 | AI/AO | A | Port 1 Transmit/Receive Positive/Negative |
| B11 | TPAN_1 | AI/AO | A | |
| A10 | TPBP_1 | AI/AO | A | |
| B10 | TPBN_1 | AI/AO | A | |
| A9 | TPCP_1 | AI/AO | A | |
| B9 | TPCN_1 | AI/AO | A | |
| A8 | TPDP_1 | AI/AO | A | |
| B8 | TPDN_1 | AI/AO | A | |
| A7 | TPAP_2 | AI/AO | A | Port 2 Transmit/Receive Positive/Negative |
| B7 | TPAN_2 | AI/AO | A | |
| A6 | TPBP_2 | AI/AO | A | |
| B6 | TPBN_2 | AI/AO | A | |
| A5 | TPCP_2 | AI/AO | A | |
| B5 | TPCN_2 | AI/AO | A | |
| A4 | TPDP_2 | AI/AO | A | |
| B4 | TPDN_2 | AI/AO | A | |
| A3 | TPAP_3 | AI/AO | A | Port 3 Transmit/Receive Positive/Negative |
| B3 | TPAN_3 | AI/AO | A | |
| A2 | TPBP_3 | AI/AO | A | |
| B2 | TPBN_3 | AI/AO | A | |
| B1 | TPCP_3 | AI/AO | A | |
| C2 | TPCN_3 | AI/AO | A | |
| C1 | TPDP_3 | AI/AO | A | |

Table 4 Ethernet Twisted Pair Interface Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---------------------------------|--------|----------|-------------|---|
| D2 | TPDN_3 | AI/AO | A | |
| N2 | TPAP_4 | AI/AO | A | Port 4 Transmit/Receive Positive/Negative |
| P1 | TPAN_4 | AI/AO | A | |
| P2 | TPBP_4 | AI/AO | A | |
| R1 | TPBN_4 | AI/AO | A | |
| R2 | TPCP_4 | AI/AO | A | |
| T2 | TPCN_4 | AI/AO | A | |
| R3 | TPDP_4 | AI/AO | A | |
| T3 | TPDN_4 | AI/AO | A | |
| R4 | TPAP_5 | AI/AO | A | Port 5 Transmit/Receive Positive/Negative |
| T4 | TPAN_5 | AI/AO | A | |
| R5 | TPBP_5 | AI/AO | A | |
| T5 | TPBN_5 | AI/AO | A | |
| R6 | TPCP_5 | AI/AO | A | |
| T6 | TPCN_5 | AI/AO | A | |
| R7 | TPDP_5 | AI/AO | A | |
| T7 | TPDN_5 | AI/AO | A | |
| R8 | TPAP_6 | AI/AO | A | Port 6 Transmit/Receive Positive/Negative |
| T8 | TPAN_6 | AI/AO | A | |
| R9 | TPBP_6 | AI/AO | A | |
| T9 | TPBN_6 | AI/AO | A | |
| R10 | TPCP_6 | AI/AO | A | |
| T10 | TPCN_6 | AI/AO | A | |
| R11 | TPDP_6 | AI/AO | A | |
| T11 | TPDN_6 | AI/AO | A | |
| R12 | TPAP_7 | AI/AO | A | Port 7 Transmit/Receive Positive/Negative |
| T12 | TPAN_7 | AI/AO | A | |
| R13 | TPBP_7 | AI/AO | A | |
| T13 | TPBN_7 | AI/AO | A | |
| R14 | TPCP_7 | AI/AO | A | |
| T14 | TPCN_7 | AI/AO | A | |
| R15 | TPDP_7 | AI/AO | A | |
| T15 | TPDN_7 | AI/AO | A | |
| Ethernet Port Test Point | | | | |
| D6 | RCAL_0 | AI/AO | A | Test Point for GPHY Ethernet Ports 0 to 3 Test point, do not connect. |
| N6 | RCAL_1 | AI/AO | A | Test Point for GPHY Ethernet Ports 4 to 7 Test point, do not connect. |

2.2.3.2 USXGMII Interface
Table 5 USXGMII Interface Signals

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|------------------|----------|-------------|--|
| D15 | URXP_0 | AI | A | Differential USXGMII 0 Data Input Pair These are the negative and positive signals of the differential input pair of the USXGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for USXGMII. These pins must be AC-coupled. |
| C16 | URXM_0 | AI | A | |
| E16 | UTXP_0 | AO | A | Differential USXGMII 0 Data Output Pair These are the negative and positive signals of the differential output pair of the USXGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for USXGMII. These pins must be AC-coupled. |
| E15 | UTXM_0 | AO | A | |
| B16 | URESREF_0 | AI/AO | A | External USXGMII Tuning Resistor 0 Attach a 200 Ω ($\pm 1\%$) resistor-to-ground on the board. |
| N15 | URXP_1 | AI | A | Differential USXGMII 1 Data Input Pair These are the negative and positive signals of the differential input pair of the USXGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for USXGMII. These pins must be AC-coupled. |
| P16 | URXM_1 | AI | A | |
| M16 | UTXP_1 | AO | A | Differential USXGMII 1 Data Output Pair These are the negative and positive signals of the differential output pair of the USXGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for USXGMII. These pins must be AC-coupled. |
| M15 | UTXM_1 | AO | A | |
| R16 | URESREF_1 | AI/AO | A | External USXGMII Tuning Resistor 1 Attach a 200 Ω ($\pm 1\%$) resistor-to-ground on the board. |

2.2.3.3 MDIO Interface

Table 6 MDIO Management Interface Signals

| Ball No. | Name | Pin Type | Buffer Type | Function |
|-----------------------------|---------------|----------|-------------|---|
| MDIO Slave Interface | | | | |
| L14 | MDINT | O | | MDIO Interrupt from Any GPHY The interrupt interrupts an external block such as a higher-level management entity or a device controller of an SoC, on detection of certain events and states inside the GPHY device. Voltage Domain: 1.8 V / 3.3 V |
| | GPIO4 | Prg | Prg | General Purpose IO 4 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 1.8 V / 3.3 V |
| K16 | MDC_S | I | | MDIO Slave Clock The external controller provides the serial clock of up to 25 MHz on this input. Voltage Domain: 1.8 V / 3.3 V |
| | GPIO5 | Prg | Prg | General Purpose IO 5 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 1.8 V / 3.3 V |
| K15 | MDIO_S | I/O | | MDIO Slave Data Input/Output The external controller uses this signal to address internal registers and to transfer data to and from the internal registers. Voltage Domain: 1.8 V / 3.3 V |
| | GPIO6 | Prg | Prg | General Purpose IO 6 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 1.8 V / 3.3 V |

2.2.3.4 QSPI Interface

Table 7 QSPI Management Interface Signals

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|-----------------|----------|-------------|--|
| K14 | QSPI_D0 | I/O | | QSPI Data 0 QSPI interface data 0 Voltage Domain: 3.3 V |
| | GPIO9 | Prg | Prg | General Purpose IO 9 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| J14 | QSPI_D1 | I/O | | QSPI Data 1 QSPI interface data 1 Voltage Domain: 3.3 V |
| | GPIO10 | Prg | Prg | General Purpose IO 10 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| J15 | QSPI_D2 | I/O | | QSPI Data 2 QSPI interface data 2 Voltage Domain: 3.3 V |
| | GPIO11 | Prg | Prg | General Purpose IO 11 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| H14 | QSPI_D3 | I/O | | QSPI Data 3 QSPI interface data 3 Voltage Domain: 3.3 V |
| | GPIO12 | Prg | Prg | General Purpose IO 12 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| J16 | QSPI_CLK | O | | QSPI Clock QSPI interface clock output Voltage Domain: 3.3 V |
| | GPIO13 | Prg | Prg | General Purpose IO 13 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |

Table 7 QSPI Management Interface Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|-----------------|----------|-------------|--|
| H16 | QSPI_CS | O | | QSPI Chip Select QSPI interface chip select Voltage Domain: 3.3 V |
| | GPIO14 | Prg | Prg | General Purpose IO 14 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| H15 | QSPI_RST | O | | QSPI Reset QSPI Reset Voltage Domain: 3.3 V |
| | GPIO15 | Prg | Prg | General Purpose IO 15 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |

2.2.3.5 I²C Interface

Table 8 I²C Management Interface Signals

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|-----------|----------|-------------|--|
| L12 | I2C_SCL_0 | O | | I²C 0 Clock Output I ² C 0 interface clock output Voltage Domain: 3.3 V |
| | GPIO16 | Prg | Prg | General Purpose IO 16 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| K13 | I2C_SDA_0 | I/O | | I²C 0 Data I ² C 0 interface data Voltage Domain: 3.3 V |
| | GPIO17 | Prg | Prg | General Purpose IO 17 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |

2.2.3.6 Reset Interface

Table 9 Reset Signals

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|-------|----------|-------------|--|
| G3 | HRSTN | I | PU | Hardware Reset Asynchronous active low device reset Voltage Domain: 3.3 V |

2.2.3.7 LED/UART/JTAG Interface
Table 10 LED and Debug Interface Signals

| Ball No. | Name | Pin Type | Buffer Type | Function |
|--------------------|------------------|----------|-------------|--|
| LED Signals | | | | |
| E1 | PHYLED1_0 | I/O | | GPHY LED1 for Port 0 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO20 | Prg | Prg | General Purpose IO 20 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| | FW_UTXD | O | | Firmware UART Data Output Firmware UART interface data output Voltage Domain: 3.3 V |
| F3 | PHYLED2_0 | I/O | | GPHY LED2 for Port 0 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO21 | Prg | Prg | General Purpose IO 21 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| | FW_URXD | I | | Firmware UART Data Input Firmware UART interface data input Voltage Domain: 3.3 V |
| F1 | PHYLED1_1 | I/O | | GPHY LED1 for Port 1 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO23 | Prg | Prg | General Purpose IO 23 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| | FW_UTXD | O | | Firmware UART Data Output Firmware UART interface data output Voltage Domain: 3.3 V |
| F2 | PHYLED2_1 | I/O | | GPHY LED2 for Port 1 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO24 | Prg | Prg | General Purpose IO 24 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |

Table 10 LED and Debug Interface Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|-----------|----------|-------------|--|
| G1 | PHYLED1_2 | I/O | | GPHY LED1 for Port 2 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO26 | Prg | Prg | General Purpose IO 26 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| | TDI | I | | JTAG Serial Test Data Input Voltage Domain: 3.3 V <i>Note: No external pull-up required.</i> |
| | FW_UTXD | O | | Firmware UART Data Output Firmware UART interface data output Voltage Domain: 3.3 V |
| G2 | PHYLED2_2 | I/O | | GPHY LED2 for Port 2 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO27 | Prg | Prg | General Purpose IO 27 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| | TMS | I | | JTAG Test Mode Select Voltage Domain: 3.3 V <i>Note: No external pull-up required.</i> |
| H1 | PHYLED1_3 | I/O | | GPHY LED1 for Port 3 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO29 | Prg | Prg | General Purpose IO 29 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| | TCK | I | | JTAG Test Clock The signals TDI, TDO and TMS are synchronous subject to this JTAG test clock. Voltage Domain: 3.3 V |
| | FW_UTXD | O | | Firmware UART Data Output Firmware UART interface data output Voltage Domain: 3.3 V |

Table 10 LED and Debug Interface Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|------------------|----------|-------------|--|
| H2 | PHYLED2_3 | I/O | | GPHY LED2 for Port 3 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO30 | Prg | Prg | General Purpose IO 30 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| | TDO | I/O | | JTAG Serial Test Data Output JTAG test data output. Voltage Domain: 3.3 V <i>Note: No external pull-up required.</i> |
| J1 | PHYLED1_4 | I/O | | GPHY LED1 for Port 4 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO32 | Prg | Prg | General Purpose IO 32 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| | FW_UTXD | O | | Firmware UART Data Output Firmware UART interface data output Voltage Domain: 3.3 V |
| J2 | PHYLED2_4 | I/O | | GPHY LED2 for Port 4 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO33 | Prg | Prg | General Purpose IO 33 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| K1 | PHYLED1_5 | I/O | | GPHY LED1 for Port 5 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO35 | Prg | Prg | General Purpose IO 35 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| | FW_UTXD | O | | Firmware UART Data Output Firmware UART interface data output Voltage Domain: 3.3 V |

Table 10 LED and Debug Interface Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|-----------|----------|-------------|--|
| K2 | PHYLED2_5 | I/O | | GPHY LED2 for Port 5 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO36 | Prg | Prg | General Purpose IO 36 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| L1 | PHYLED1_6 | I/O | | GPHY LED1 for Port 6 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO38 | Prg | Prg | General Purpose IO 38 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| | FW_UTXD | O | | Firmware UART Data Output Firmware UART interface data output Voltage Domain: 3.3 V |
| L2 | PHYLED2_6 | I/O | | GPHY LED2 for Port 6 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO39 | Prg | Prg | General Purpose IO 39 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| M1 | PHYLED1_7 | I/O | | GPHY LED1 for Port 7 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO41 | Prg | Prg | General Purpose IO 41 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| | FW_UTXD | O | | Firmware UART Data Output Firmware UART interface data output Voltage Domain: 3.3 V |

Table 10 LED and Debug Interface Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|-----------|----------|-------------|--|
| L3 | PHYLED2_7 | I/O | | GPHY LED2 for Port 7 LED control output, drives single-color or dual color LEDs. Voltage Domain: 3.3 V |
| | GPIO42 | Prg | Prg | General Purpose IO 42 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| M2 | TRSTN | I | | JTAG Test Enabling At logic HIGH: the GPIO pins are used as JTAG interface (TCK, TDI, TDO, and TMS) At logic LOW: the GPIO pins their normal application mode Voltage Domain: 3.3 V |

2.2.3.8 Miscellaneous Signals

Table 11 Miscellaneous Signals

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---------------------------|--------------|----------|-------------|--|
| Reset and Clocking | | | | |
| G16 | XTAL1 | AI | A | Crystal: Oscillator Input A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must tie both pins to GND. |
| | CLK | AI | A | Crystal Oscillator: Clock Input A clock of 25, 50, or 156.25 MHz must be connected to CLK. See Section 7.7.2 for the clock details. XTAL2 must not be connected. |
| G15 | XTAL2 | AO | A | Crystal: Oscillator Output A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must tie both pins to GND. |
| F13 | GPC0 | Prg | | General Purpose Clock 0 General purpose clock for SyncE or external devices. Either input or output mode. Voltage Domain: 3.3 V |
| | GPIO44 | Prg | Prg | General Purpose IO 44 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| G13 | GPC1 | Prg | | General Purpose Clock 1 General purpose clock for SyncE or external devices. Either input or output mode. Voltage Domain: 3.3 V |
| | GPIO45 | Prg | Prg | General Purpose IO 45 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| F14 | GPC2 | Prg | | General Purpose Clock 2 General purpose clock for SyncE or external devices. Either input or output mode. Voltage Domain: 3.3 V |
| | GPIO46 | Prg | Prg | General Purpose IO 46 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |

Table 11 Miscellaneous Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|--------------|----------|-------------|---|
| J13 | GPC3 | Prg | | General Purpose Clock 3 General purpose clock for SyncE or external devices. Either input or output mode. Voltage Domain: 3.3 V |
| | GPIO47 | Prg | Prg | General Purpose IO 47 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| L15 | GPIO0 | Prg | Prg | General Purpose IO 0 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 1.8 V / 3.3 V |
| | EXTINT0 | Prg | Prg | External Interrupt 0 Voltage Domain: 1.8 V / 3.3 V |
| H3 | GPIO1 | Prg | Prg | General Purpose IO 1 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| | EXTINT1 | Prg | Prg | External Interrupt 1 Voltage Domain: 3.3 V |
| J3 | GPIO2 | Prg | Prg | General Purpose IO 2 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |
| K3 | GPIO3 | Prg | Prg | General Purpose IO 3 Either input or output mode. The output characteristic is either open drain or push-pull. Voltage Domain: 3.3 V |

2.2.3.9 Power Supply for GPHY

Table 12 Power Supply Pins for GPHY

| Ball No. | Name | Pin Type | Buffer Type | Function |
|-------------|------------|----------|-------------|--|
| C11 | VDDA3V3_0 | PWR | | GPHY 0, 3.3 V Voltage Domain Supply This is the PHY 0 AFE 3.3 V supply. |
| C9 | VDDA3V3_1 | PWR | | GPHY 1, 3.3 V Voltage Domain Supply This is the PHY 1 AFE 3.3 V supply. |
| C7 | VDDA3V3_2 | PWR | | GPHY 2, 3.3 V Voltage Domain Supply This is the PHY 2 AFE 3.3 V supply. |
| C5 | VDDA3V3_3 | PWR | | GPHY 3, 3.3 V Voltage Domain Supply This is the PHY 3 AFE 3.3 V supply. |
| P5 | VDDA3V3_4 | PWR | | GPHY 4, 3.3 V Voltage Domain Supply This is the PHY 4 AFE 3.3 V supply. |
| P7 | VDDA3V3_5 | PWR | | GPHY 5, 3.3 V Voltage Domain Supply This is the PHY 5 AFE 3.3 V supply. |
| P9 | VDDA3V3_6 | PWR | | GPHY 6, 3.3 V Voltage Domain Supply This is the PHY 6 AFE 3.3 V supply. |
| P11 | VDDA3V3_7 | PWR | | GPHY 7, 3.3 V Voltage Domain Supply This is the PHY 7 AFE 3.3 V supply. |
| D7, D8 | VDDA1V8_0 | PWR | | GPHY 0, 1, 2, 3, 1.8 V Voltage Domain Supply This is the 1.8 V supply for PHY 0 to PHY 3 AFE voltage domain. It supplies mixed signal blocks in the AFE. |
| N7, N8 | VDDA1V8_1 | PWR | | GPHY 4, 5, 6, 7, 1.8 V Voltage Domain Supply This is the 1.8 V supply for PHY 4 to PHY 7 AFE voltage domain. It supplies mixed signal blocks in the AFE. |
| E6, E8, E11 | VDDA0V8_0 | PWR | | GPHY 0, 1, 2, 3, 0.8 V Voltage Domain Supply This is the supply for PHY 0 to PHY 3 low voltage domain. It supplies mixed signal blocks in the AFE. |
| M6, M8, M11 | VDDA0V8_1 | PWR | | GPHY 4, 5, 6, 7, 0.8 V Voltage Domain Supply This is the supply for PHY 4 to PHY 7 low voltage domain. It supplies mixed signal blocks in the AFE. |
| D3, E3, N3 | VDD3V3PAD0 | PWR | | Power Supply Digital Domain 3.3 V 3.3 V Voltage Digital Power Supply |
| D12, N12 | VDD3V3PAD1 | PWR | | Power Supply Digital Domain 3.3 V 3.3 V Voltage Digital Power Supply |
| H13 | VDDP_PAD | PWR | | Power Supply Digital Domain 1.8V / 3.3 V 3.3 V or 1.8 V Pad Voltage Digital Power Supply based on pin strapping. |

Table 12 Power Supply Pins for GPHY (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|--|--------------------------|----------|-------------|---|
| F4, G4, F6, G6, F8, G8, F10, G10, H5, J5, H7, J7, H9, J9, K4, L4, K6, L6, K8, L8, K10, L10 | VDDD0V8_C OR | PWR | | Power Supply Digital Domain 0.8 V 0.8 V Core Voltage Digital Power Supply |
| H11 | VDDA1V8PO RXO | PWR | | Power Supply Domain 1.8 V |
| D9, D10 | VDDA1V2CD B0 | PWR | | Power Supply Domain 1.2 V |
| N9, N10 | VDDA1V2CD B1 | PWR | | Power Supply Domain 1.2 V |
| J11 | VDDA1V8_PL L | PWR | | Power Supply Domain 1.8 V |
| F12 | VDDD0V8REF | PWR | | Power Supply Digital Domain 0.8 V |
| G11 | VDDD0V8PO ST | PWR | | Power Supply Digital Domain 0.8 V |
| K12 | VDDA1V8_PV T | PWR | | Power Supply Domain 1.8 V |
| H12 | VCC1V8_OTP | PWR | | Power Supply Domain 1.8 V |

2.2.3.10 Power Supply for USXGMII

Table 13 Power Supply Pins for USXGMII

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|-----------|----------|-------------|--|
| D13, D14 | VA0V8_0 | PWR | | USXGMII 0 - 0.8 V Analog Domain Supply |
| E13 | VPHA1V8_0 | PWR | | USXGMII 0 - 1.8 V Domain Supply |
| N13, N14 | VA0V8_1 | PWR | | USXGMII 1 - 0.8 V Analog Domain Supply |
| M13 | VPHA1V8_1 | PWR | | USXGMII 1 - 1.8 V Domain Supply |

2.2.3.11 Power Supply for TPI (AFE)

Table 14 Power Supply Pins for TPI (AFE)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|----------|----------|-------------|---------------|
| A1, A16, C3, C4, C6, C8, C10, C12, C13, D1, D4, D5, D11, E2, E4, E5, E7, E9, E10 | TPVSSA_0 | GND | | Analog Ground |
| M4, M5, M7, M9, M10, N1, N4, N5, N11, P3, P4, P6, P8, P10, P12, P13, T1, T16 | TPVSSA_1 | GND | | Analog Ground |

2.2.3.12 Ground

Table 15 Ground Pins

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---------------|----------|-------------|--------------------------------------|
| E12, F5, G5, F7, G7, F9, G9, F11, G14, H4, J4, H6, J6, H8, J8, H10, J10, J12, K5, L5, K7, L7, K9, L9, K11, L11, L13, L16, M3, M12 | VSSD | GND | | Digital Ground |
| C14, C15, D16, E14, M14, N16, P14, P15 | UVSS | GND | | USXGMII Ground |
| F15, F16, G12 | VSS_XO | GND | | XO Device Ground XO ground |

3 Functional Description

3.1 Power Supply, Clock, and Reset

This section provides the information required to power up the MxL86289C.

3.1.1 Power Supply

These four power supply rails are required: 3.3 V, 0.8 V, 1.8 V, and 1.2 V. Refer to [Section 7.7.1](#) for the power up sequence.

3.1.2 Clock

An internal PLL circuit generates the required internal clocks, based on an external reference clock.

The available options are:

- An external 25 MHz crystal connected to the MxL86289C. [Section 7.7.9](#) documents the required crystal specification.
- 25 MHz direct from an external oscillator
- An external CML/LVPECL reference clock operating at 50 MHz
- An external LVPECL reference clock operating at 156.25 MHz

3.1.3 Reset Generation

The external hardware reset input (HRSTN pin) resets all the hardware modules including the pin strapping information during boot:

- Driving the HRSTN pin low causes an asynchronous reset of the MxL86289C system.
- Releasing the HRSTN pin high triggers the power-on sequence.

The HRSTN pin is internally connected to a weak internal pull-up resistor.

3.1.4 Power-On Sequence

The MxL86289C powers on when the power is applied and the HRSTN pin is high. See [Figure 18](#).

The steps executed at power on are:

1. Lock the internal PLL.
2. Read the pin strap information, see [Section 3.1.5](#) for more information.
3. Boot the microprocessor from the internal ROM.
4. In flashless mode, wait for the firmware to download into on-chip memory.
5. Authenticate the firmware image in the flash memory device or on-chip memory.
6. Auto-negotiate the link speeds for the Ethernet TPI and USXGMII interfaces.
7. Train and link up each interface in accordance with the IEEE 802.3 [\[3\]](#) standards.

3.1.5 Configuration by Pin Strapping

The MxL86289C is configurable by means of pin strapping on a number of the GPIO pins. The pin strapping configurations are captured during the chip power-on sequence until the reset initialization is complete.

The pin strap values are set to logical high or low by connecting the corresponding pin via an external 1 kΩ resistor to either ground or the pin supply voltage.

[Table 16](#) and [Table 17](#) describe the pin strap mapping.

Table 16 Pin Names Used for Pin Strapping

| Ball Name | Ball Number | Configuration Item Description |
|-----------|-------------|--------------------------------|
| GPC1 | G13 | PS_PHY_MADDR(4) |
| GPC2 | F14 | PS_PHY_MADDR(3) |
| GPC3 | J13 | PS_CLK_SEL |
| GPIO1 | H3 | PS_CLK_SEL1 |
| GPIO2 | J3 | PS_RJ45_TAB |
| MDINT | L14 | PS_MDINT_POLARITY |
| GPIO3 | K3 | PS_MDIO_VOLTAGE |
| GPC0 | F13 | PS_SUPER_ISOLATE |
| QSPI_CS | H16 | PS_FLASHLESS |

Table 17 Pin Strapping Configuration Description

| Pin Strapping Signals | Description |
|-----------------------|---|
| PS_PHY_MADDR(4:3) | MDIO PHY Address Specifies the most significant two bits of the MDIO address. The lowest three bits are hard-coded to 0, 1, 2, 3, 4, 5, 6, and 7 for each BASE-T port of the MxL86289C. |
| PS_MDINT_POLARITY | MDIO Interrupt Polarity Specifies the polarity of the MDIO interrupt. 0 _B HIGH MDIO interrupt is active high. 1 _B LOW MDIO interrupt is active low. |
| PS_RJ45_TAB | RJ45 Tab Configuration Specifies the tab-up or tab-down configuration of the RJ45. Each BASE-T port has the same configuration. 1 _B DOWN Tab-down 0 _B UP Tab-up |
| PS_MDIO_VOLTAGE | MDIO Voltage Specifies whether the maximum voltage level used by the MDIO signals is 3.3 V or 1.8 V. 0 _H LOW MDIO_S, MDC_S, MDINT, and GPIO0 signal pins are supplied with 1.8 V. In this configuration, V _{DDP} must be supplied with 1.8 V. 1 _H NORMAL MDIO_S, MDC_S, MDINT, and GPIO0 signal pins are supplied with 3.3 V. In this configuration, V _{DDP} must be supplied with 3.3 V. |

Table 17 Pin Strapping Configuration Description (cont'd)

| Pin Strapping Signals | Description |
|---------------------------|---|
| PS_CLK_SEL PS_CLK_SEL1 | <p>Input Clock Selection Specifies the input clock frequency used. MSB is PS_CLK_SEL1. LSB is PS_CLK_SEL.</p> <p>11_B 25 25 MHz 10_B 50 50 MHz 01_B 156 156.25 MHz 00_B RES Reserved</p> |
| PS_SUPER_ISOLATE | <p>Super Isolate Specifies whether the PHY is immediately active after a reset or is halted until it is manually activated.</p> <p>0_H HALT The PHYs are inactive after reset. 1_H NORMAL The PHYs are active after reset.</p> |
| PS_FLASHLESS | <p>Flashless Specifies whether the device operates with or without an external flash memory device.</p> <p>0_H FLASHLESS A flash memory device is not attached. 1_H NORMAL A flash memory device is attached.</p> |

Alternative ways to configure the MxL86289C after the boot process are to use the MDIO interface and write into various control registers, as detailed in [Section 3.3](#), or to use the FCA [\[2\]](#).

3.2 MDIO Slave Interface

The SMDIO module and the Ethernet PHY (GPHY) port 0 to 7 are directly attached to the MDIO slave interface as shown in the [Figure 4](#). Each GPHY port supports both IEEE 802.3 clause 22 and clause 45 protocol. It allows direct access to the PHY using the correct MDIO PHY address. The MDIO address used for this access is configurable through pin-strapping, as described in [Section 3.1.5](#).

The SMDIO module provides access to the external flash memory device via the QSPI interface and the internal SRAM. The MxL86289C supports downloading of firmware to the flash memory device or the internal SRAM via the SMDIO module attached to the MDIO bus. In the flash mode, whereby the firmware is downloaded to the external flash memory device, the MDIO address used for this access is the same MDIO address as GPHY port 0 defined by the pin strapping. In the flashless mode, whereby the firmware is downloaded to the internal SRAM, the MDIO address used for this access is $1F_H$. The MxL86289C user guide [\[2\]](#) describing the driver software executed on the external processor must be followed to execute this feature. The SMDIO module supports only IEEE 802.3 clause 22 protocol.

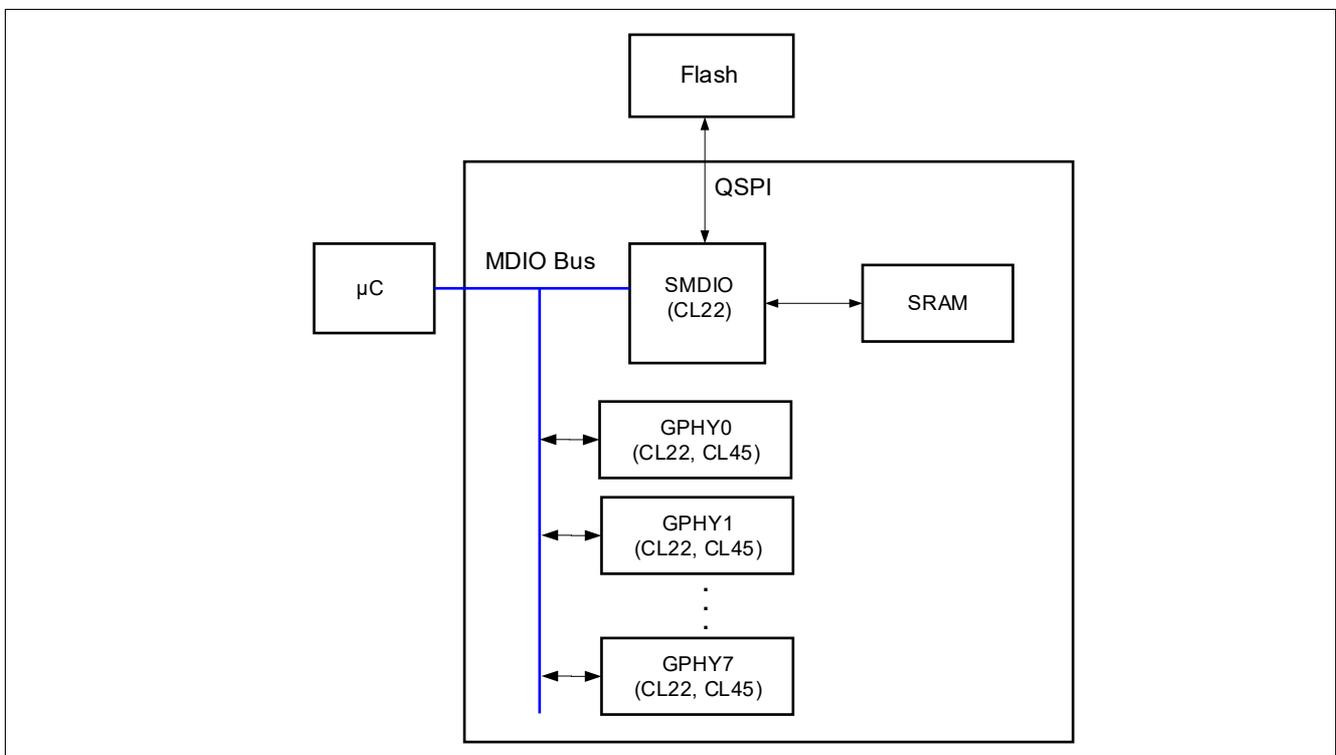


Figure 4 MDIO Slave

When other devices in the system need to be configured through MDIO, they must be connected to the MDIO slave interface and configured such that no addressing conflict arises.

The standard MDIO protocol requires a 32-bit preamble at the beginning of each read or write access. To speed up the data exchange, reduce the preamble down to 1 bit for the second and subsequent accesses.

The standard MDIO protocol uses a clock rate of 2.5 MHz on MDC. To speed up the data exchange, increase the clock applied on MDC_S to the maximum 25 MHz. Refer to the AC characteristics in [Section 7.7.4](#) for more detail.

3.3 Configuration via MDIO Management Interface

It is possible to connect an external controller's STA to the chip's slave MDIO interface. This allows access to the MDIO and MMD registers standardized in IEEE 802.3, enabling the STA to control the chip configuration and retrieve status information. The MDIO transactions are any of the three types described in IEEE 802.3 Clause 22, Clause 22 Extended, and Clause 45 [3].

Figure 5 and Table 18 show the minimum time required for the MDIO to be available for access.

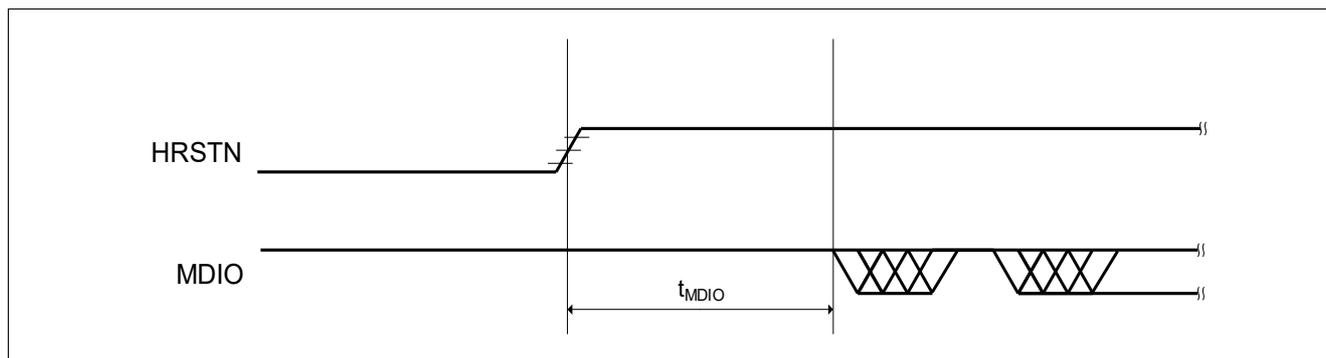


Figure 5 MDIO Access Timing

Table 18 MDIO Ready Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| MDIO Ready Time with Flash Device Attached | T_{MDIO} | 750 | – | – | ms | Flash Memory Mode This is the minimum amount of time the MDIO interface is unavailable while the MxL86289C boots and the firmware is downloaded from an external flash device using the QSPI interface. |
| MDIO Ready Time without Flash Device Attached | T_{MDIO} | 50 | – | – | ms | Flashless Mode This is the minimum amount of time the MDIO interface requires before a firmware download can be initiated from a host MAC SoC using the MDIO interface. MDIO and MMD register access is only available after the firmware download has completed and successfully authenticated. |

3.4 I²C Master Interface

The MxL86289C has one chip-integrated I²C master controller. The Inter-IC (I²C) Bus was developed by Philips Semiconductors (now NXP Semiconductors). This specification is compliant with [\[10\]](#).

The I²C is a simple, bi-directional half-duplex bus with data transfers of up to 100 Kbps in standard mode, up to 400 Kbps in fast mode, up to 1000 Kbps in fast mode plus, and up to 3.4 Mbps in high-speed (hs) mode.

I²C provides a protocol allowing devices to communicate directly with each other via two wires. One line is responsible for the clock synchronization (SCL), the other is responsible for the data transfer (SDA). The number of devices connected to the I²C bus is limited only by a maximum bus capacity of 400 pF. Each device is recognized by a unique address.

The two bi-directional bus lines, a Serial Data (SDA) line and a Serial Clock (SCL) line, are connected to a positive supply voltage via pull-up resistors. The output stages of devices must have an open drain to perform the required wired-AND function. One line is pulled low when one of the open-drain transistors is selected. Otherwise, no signal is asserted to the line. The external pull-up resistors lift the level to HIGH.

The I²C specification defines a master/slave relationship where each device works either as a transmitter or a receiver depending on the device function. This functionality is set in the initialization procedure of each module.

Features

- One I²C controller
- Master-mode supported
- Compatible to the I²C specification version 6.0, April 2014¹⁾
- Data transfer in standard- (0 to 100 kBaud), fast- (0 to 400 kBaud), fast mode plus (0 to 1 Mbps) and high-speed mode (0 to 3.4 Mbps)

1) For deviations of timing values compared to the Philips Semiconductors (now NXP Semiconductors*) specifications, see [Chapter 7 Electrical Characteristics](#).

3.5 Quad Serial Peripheral Interface

A Quad Serial Peripheral Interface (QSPI) is equipped to provide access to external Quad-SPI flash memory devices. The MxL86289C requires an external Quad-SPI flash memory to operate in flash mode. Flashless mode allows the firmware to be downloaded via the slave MDIO. The mode is selectable by pin strapping.

Use of an additional QSPI flash memory device depends upon the device operation mode:

- In flash mode, the firmware for the MxL86289C is stored in an external QSPI flash memory device and transferred over the QSPI interface. In flash mode, an external QSPI flash memory device is required.
- In flashless mode, the firmware for the MxL86289C is stored on a host SoC and transferred over the slave MDIO interface. In flashless mode, an external QSPI flash memory device is not required.

The QSPI supports:

- Up to 101.5625 MHz for single/double data rate
- eXecution In Place (XIP), fully memory mapped access for CPU
- Addressing up to 512 MB range

3.5.1 Supported Flash Memory Devices

Table 19 lists the qualified flash memory devices. However, it is possible for the user to select a device not present in the list after consideration of command compatibility and timing compatibility as listed in **Table 20**. The flash memory device must support 101.5625 MHz single data rate.

Table 19 Supported Flash Memory Devices

| Vendor | Model |
|----------|--------------|
| Macronix | MX25L6433F |
| Winbond | W25Q64JV-DTR |

Table 20 Flash command and timing

| Instruction | Abbreviation | Command | Command Cycles | Address Cycles | Dummy Cycles | Data Cycles |
|-----------------------------|--------------|-----------------|----------------|----------------|--------------|---------------------|
| Write Enable | WREN | 06 _H | 8 | 0 | 0 | 0 |
| Write Disable | WRDI | 04 _H | 8 | 0 | 0 | 0 |
| Read ID | RDID | 9F _H | 8 | 0 | 0 | 24 |
| Read Status Register | RDSR | 05 _H | 8 | 0 | 0 | 8 |
| Write Status Register | WRSR | 01 _H | 8 | 0 | 0 | 8 |
| Read Configuration Register | RDCR | 15 _H | 8 | 0 | 0 | 8 |
| Read Data Bytes | READ | 03 _H | 8 | 24 | 0 | 8 |
| Fast Read | FREAD | 0B _H | 8 | 24 | 8 | 8 |
| Quad Read | 4READ | EB _H | 8 | 6 | 10 | 2 |
| XIP | XIP | EB _H | 8 | 6 | 10 | 2 x n ¹⁾ |
| Chip Erase | CE | C7 _H | 8 | 0 | 0 | 0 |
| Block Erase | BE | D8 _H | 8 | 24 | 0 | 0 |
| Sector Erase | SE | 20 _H | 8 | 24 | 0 | 0 |
| Page Program | PP | 02 _H | 8 | 24 | 0 | 8 x n ¹⁾ |
| Reset Enable | RSTEN | 66 _H | 8 | 0 | 0 | 0 |
| Reset | RST | 99 _H | 8 | 0 | 0 | 0 |

1) n is the number of bytes

3.6 Ethernet PHY Interface

The Ethernet PHY implements the physical layer of the Ethernet standard. It supports Digital Signal Processing (DSP) and Analog Signal Processing (ASP) functions in transmitting data over the twisted pair cable.

3.6.1 Twisted Pair Interface

The Twisted Pair Interface (TPI) of the MxL86289C is fully compliant with IEEE 802.3. The MxL86289C integrates series resistors required to terminate the TPI links with a 100 Ω nominal impedance to facilitate a low-power implementation and reduce PCB costs. As a consequence, it is possible to connect the TPI pins directly via a transformer to the RJ45 connector. Additional external circuitry is required for common-mode termination and rejection as described in [Section 7.8.1](#).

[Figure 6](#) shows a schematic of the TPI circuitry taking these components into account.

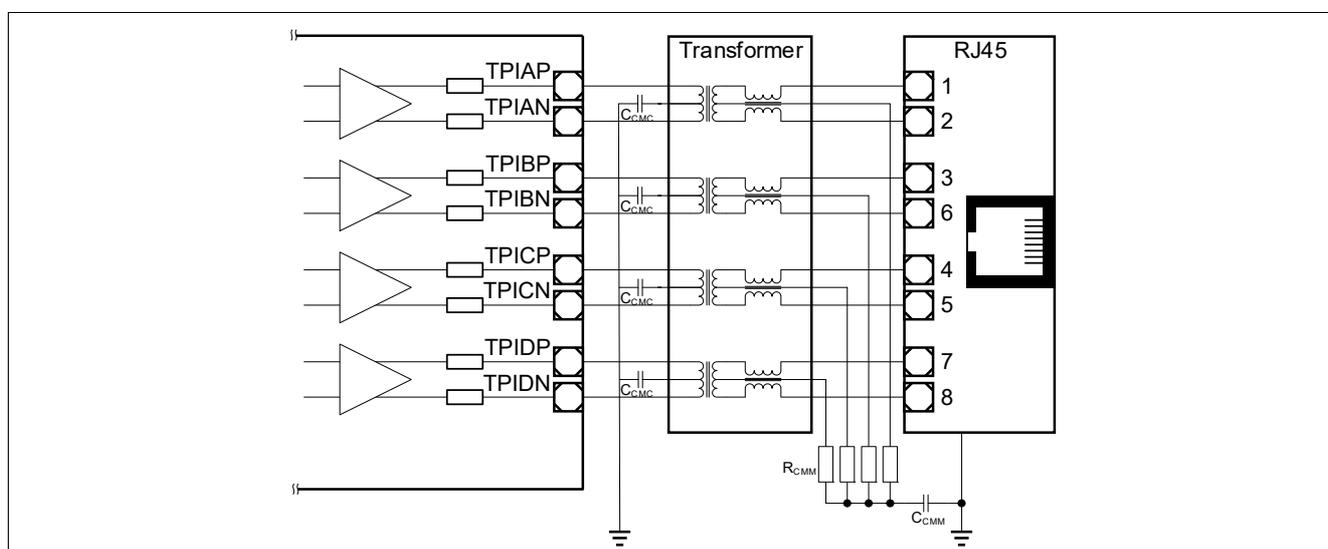


Figure 6 Twisted-Pair Interface of MxL86289C Including Transformer and RJ45 Plug

3.6.2 Transformerless Ethernet

Transformerless Ethernet (TLE) is required for backplane applications where the use of a transformer is not always required to fulfill the galvanic decoupling requirements of the isolation specifications. In such applications, removing the transformer reduces both the external bill of material and the space requirements on the PCB.

As the MxL86289C incorporates a voltage-mode line driver, the only stringent requirement is to use AC coupling, which is achievable using simple SMD type series capacitors. The value of the capacitors is selected such that the high-pass characteristics correspond to an equivalent standard transformer based application. The recommended value is $C_{\text{coupling}} = 100 \text{ nF}$. [Figure 7](#) shows the external circuitry for TLE.

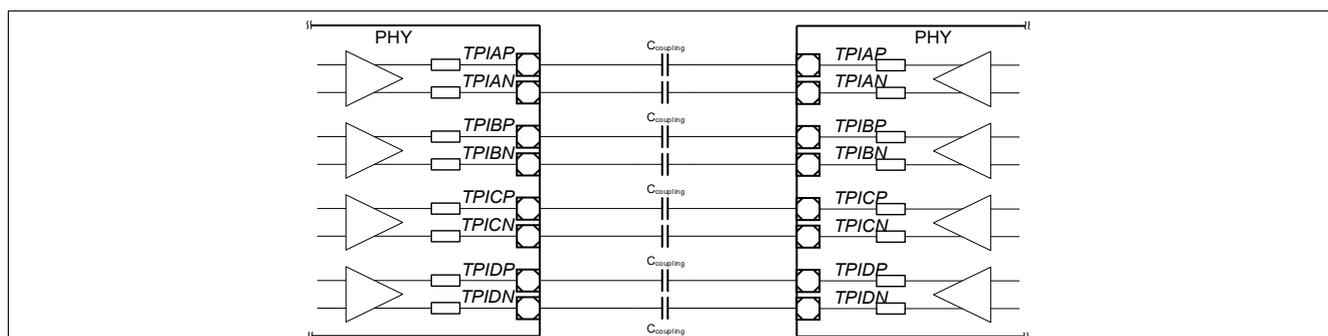


Figure 7 External Circuitry for the Transformerless Ethernet Application

3.6.3 Auto-Negotiation

The MxL86289C supports auto-negotiation (ANEG) as part of the startup procedure to exchange capability information with the link partner. ANEG is enabled at the MxL86289C initialization and its 2.5 Gbps speed capability is advertised. The ANEG procedure is executed according to IEEE 802.3 Clause 28, Clause 40, and IEEE 802.3 Clause 126 [3]. When the link partner does not support ANEG, the MxL86289C determines the link speed configuration using parallel detection as described in Clause 28.

With MDIO commands, it is possible to disable ANEG and change the advertised link rates. The STA is also able to disable ANEG. In this situation, the system configuration must ensure compatibility between link partners to allow link up in a compatible mode.

Attention: *STD_CTRL.DPLX only takes effect when the ANEG process is disabled and the GPHY TPI is not operating in loopback mode, that is, bits STD_CTRL.ANEN and STD_CTRL.LB are set to zero. Forced half-duplex mode (STD_CTRL.DPLX = 0b0) is only supported in 10BASE-T and 100BASE-TX speed modes. This field is ignored for higher speeds. This field is also ignored for transparent mode because half-duplex is not supported in this mode.*

3.6.4 Auto-Downspeed

The auto-downspeed (ADS) feature implements a process to renegotiate the link with a lower speed when the link quality is insufficient. The feature ensures maximum interoperability even in harsh, or inadequate, cable infrastructure environments. In particular, ADS is applied during the 2.5GBASE-T/1000BASE-T training phase. ADS is also required when the quality or characteristics of the cable in use cannot support the advertised speed.

For example, it is possible to advertise 2.5GBASE-T/1000BASE-T during ANEG when both link partners are connected via a cable that does not support the 4-pair Gigabit Ethernet mode. The MxL86289C detects such a configuration to avoid repeating link up failures and clears the 2.5GBASE-T/1000BASE-T capability in the ANEG advertisement registers. After the resulting link down, the next ANEG procedure no longer advertises 1000BASE-T/2.5GBASE-T. The next link up is done at the next advertised speed below 1000 Mbps.

The MxL86289C also executes an ADS procedure when the signal quality is not suited to a 1000BASE-T/2.5GBASE-T link up due to increased alien noise or a loop length that significantly exceeds the standard specification.

When the MxL86289C is configured not to advertise a speed capability below 1000 Mbps, the ADS feature is automatically disabled.

3.6.5 Polarity Reversal Correction

For each of the 4 pairs, the MxL86289C automatically detects and corrects any inversion of the signal polarity on the P and N signals. The detection is done during the auto-negotiation phase. The detected polarity is frozen when the link is established, and remains unchanged until the link is dropped.

The polarity corrections applied are indicated in the register: PMA_MGBT_POLARITY (register 1.130); and are valid after auto-negotiation is complete.

3.6.6 Auto-Crossover Correction

To maximize interoperability, even in inadequate wiring environments, the MxL86289C automatically performs cable crossover (MDI-X) correction. [Table 21](#) lists the supported pair-mappings detectable and correctable by the device.

The MxL86289C automatically detects and corrects crossed cable configuration, where the transmit-receive pairing between partners does not match. The auto-crossover function is fully compliant with IEEE 802.3, Clause 40.4.4 [3], in 1000BASE-T and 2.5GBASE-T mode.

Functional Description

The corrections applied are indicated in the register: PMA_MGBT_POLARITY (register 1.130) and are valid when auto-negotiation is complete.

Table 21 Supported Twisted Pair Mappings on a Cat 5 or Better Cable

| Crossover Modes on RJ45 ¹⁾ | | RJ45 Pinning | | | | | | | |
|---------------------------------------|---|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| Mode | Description | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 11 | Straight cable, standard compliant | TPIAP (A+) | TPIAN (A-) | TPIBP (B+) | TPICP (C+) | TPICN (C-) | TPIBN (B-) | TPIDP (D+) | TPIDN (D-) |
| 00 | Full Gigabit Ethernet MDI-X This is standard-compliant MDI-X with pair A/B swapped and pair C/D swapped. | TPIBP (B+) | TPIBN (B-) | TPIAP (A+) | TPIDP (D+) | TPIDN (D-) | TPIAN (A-) | TPICP (C+) | TPICN (C-) |

1) This pin assignment is according to TIA/EIA-568-A/B.

3.6.7 RJ45 Tab Up or Tab Down Configuration

Figure 8 shows that the RJ45 plug on the system PCB is solderable with the tab either up or down.

The difference between tab up and tab down is a swap in position between A and D, and a swap in position between B and C. The pin strap PS_RJ45_TAB allows the system designer to perform this configuration. As a result, a PCB layout does not need to be modified when a RJ45 tab up or down socket needs to be mounted. The single pin strap is applicable to all ports, which are either all tab down or all tab up.

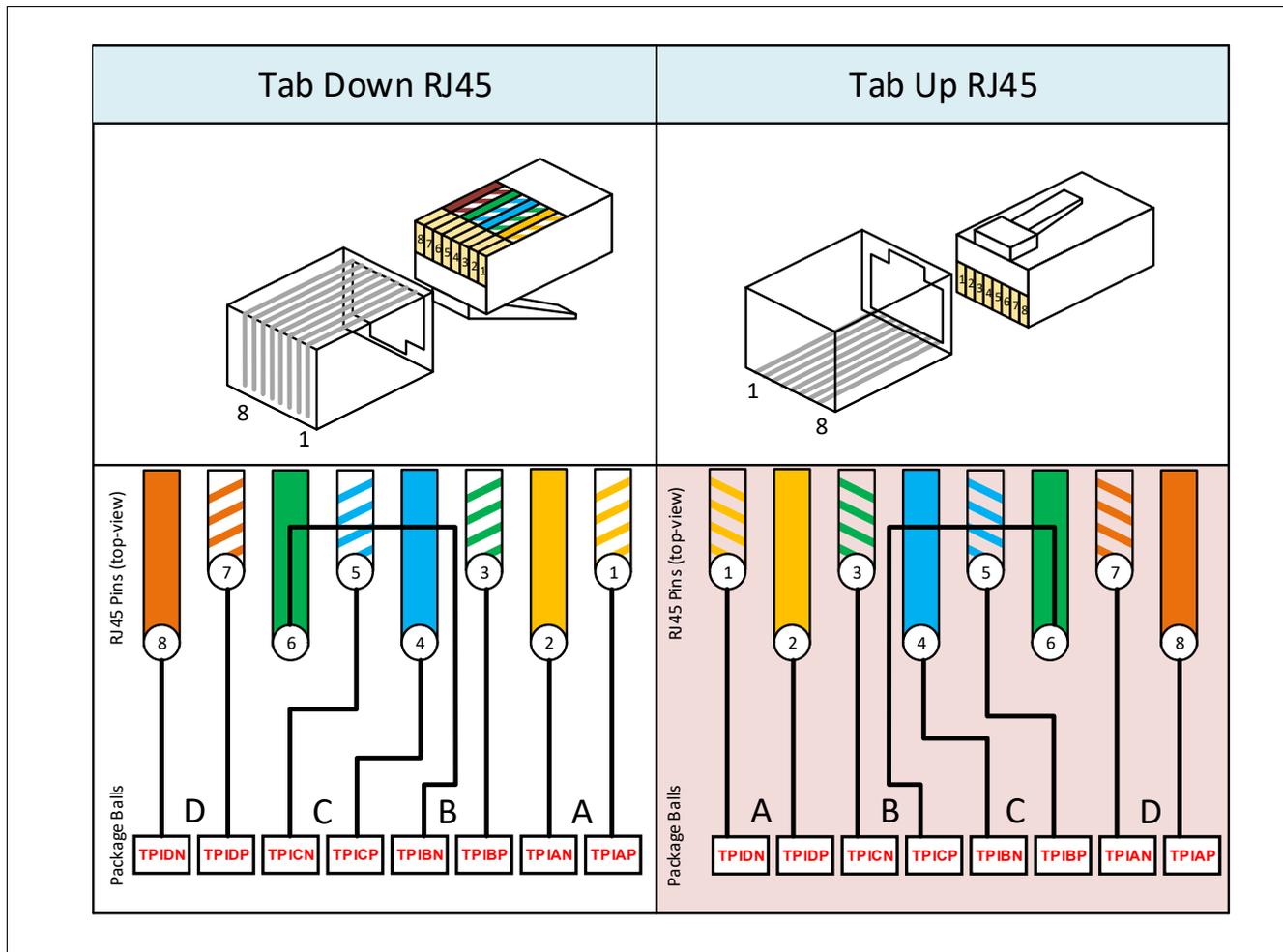


Figure 8 RJ45 Tab Up or Tab Down Configuration

3.6.8 Wake-on-LAN

The MxL86289C supports WoL. The MxL86289C generates an interrupt to an external controller when it detects special WoL Ethernet packets. This allows the controller to enter sleep mode when there is no Ethernet traffic to process, and be woken up when traffic starts. WoL packets are detected at all link speeds. **Figure 9** shows the scenario when connected to an external device.

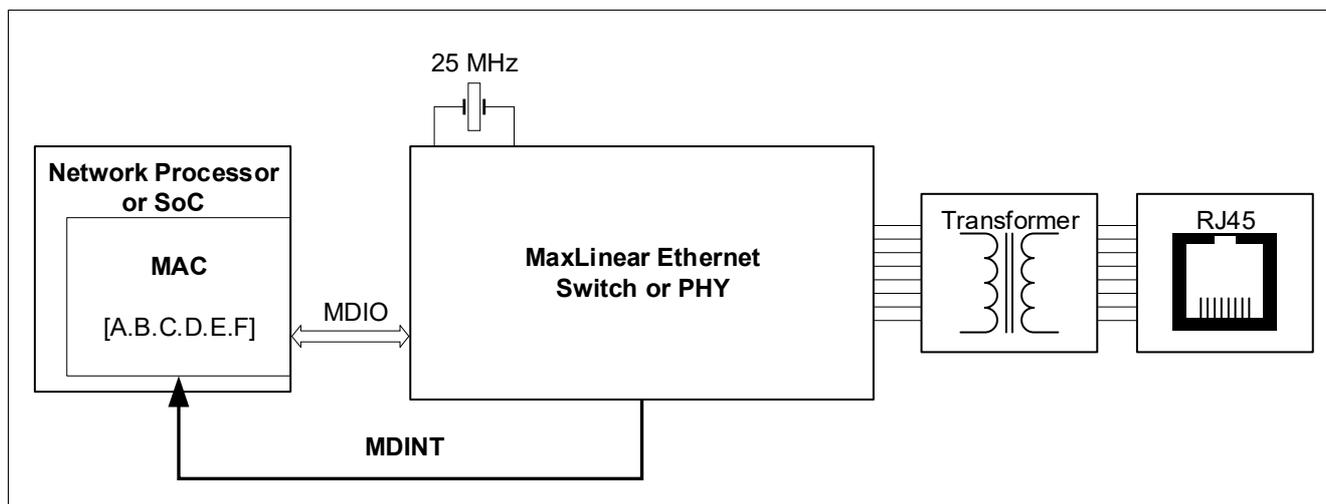


Figure 9 WoL Application Block Diagram

The most commonly used WoL packet is called a magic packet, which contains the MAC address of the device to be woken up, and an optional password called SecureON. The MAC address and the optional SecureON password relevant for the WoL logic inside the MxL86289C are configurable in the WoL MDIO registers in the Vendor Specific 2, VSPEC2 MMD, device described in **Chapter 4**. When such a configured magic packet is received, an MDINT interrupt is issued.

Table 22 gives an example programming sequence for these configuration registers.

Table 22 Programming Sequence for the Wake-on-LAN Functionality

| Step | Register Access | Remark |
|------|--|--|
| 1 | MDIO.MMD.WOLAD01 = EEFF _H | Programs the fifth and sixth MAC address bytes. |
| 2 | MDIO.MMD.WOLAD23 = CCDD _H | Programs the third and fourth MAC address bytes. |
| 3 | MDIO.MMD.WOLAD45 = AAB B _H | Programs the first and second MAC address bytes. |
| 4 | MDIO.MMD.WOLPW01 = 4455 _H | Programs the fifth and sixth SecureON password bytes. |
| 5 | MDIO.MMD.WOLPW23 = 2233 _H | Programs the third and fourth SecureON password bytes. |
| 6 | MDIO.MMD.WOLPW45 = 0011 _H | Programs the first and second SecureON password bytes. |
| 7 | MDIO.PHY.IMASK.WOL = 1 _B | Enables the wake-on-LAN interrupt mask. |
| 8 | MDIO.MMD.WOLCTRL.WOL.EN = 1 _B | Enables wake-on-LAN functionality. |

3.7 Ethernet SerDes Interface

The MxL86289C implements two Ethernet serial data interfaces. [Table 4](#) lists the data rates supported by the USXGMII interface.

The external PHY is able to initiate clause 37 auto-negotiation to change speed and new link up. In USXGMII mode, the interface supports the Packet Control Header (PCH) over preamble to transport control or timestamp indications between the MAC and the PHY.

Table 23 Ethernet SerDes Interface Feature List

| Modes | Baudrate | Coding | Link Speed | IEEE Clause | Auto-Negotiation Clause |
|------------|--------------|---------|---|-------------|-------------------------|
| 10G-QXGMII | 10.3125 GT/s | 64b/66b | 2.5 Gbps, 1 Gbps, 100 Mbps, and 10 Mbps | 49 | 37 |

3.7.1 Ethernet SerDes Interface Configuration at Power On

The MxL86289C USXGMII interface is configured to operate automatically after reset. It is not necessary for the STA to change the VSPEC1_PM_CTRL.USXGMII_REACH register to operate in this default mode.

These are the steps in the default process:

1. USXGMII auto-negotiation is enabled by default.
2. The TPI configuration after link up defines the corresponding USXGMII PHY-side port configuration. The MAC-side SoC must configure its USXGMII MAC-side interface to match the MxL86289C PHY-side configuration.
3. The MxL86289C API describes the procedure to update the Rx/Tx equalization parameters. The MxL86289C automatically updates the Rx/Tx equalization parameters for standard trace lengths based on the trace length programmed in VSPEC1_PM.USXGMII_REACH. For custom trace lengths, the Rx/Tx equalization parameters are configured using the API [\[1\]](#).

3.8 LED Interface

This section describes the LED interface.

3.8.1 LED

The MxL86289C allows 16 synchronized LEDs to be used for visual status indication. Each LED pin drives either a single color LED or dual color LED.

3.8.2 LED Configuration

The MxL86289C API [1] describing the driver software executed on the Host SoC must be followed to configure this interface.

Figure 10 shows the external LED connected to either ground or the power rail in single color mode.

Figure 11 and **Figure 12** show the connection of single and dual color LEDs when the pin is also used for pin strapping.

Note: These figures do not show the full recommended circuits with all the necessary components. Refer to the relevant HDK/EVK PCB design documentation for more details.

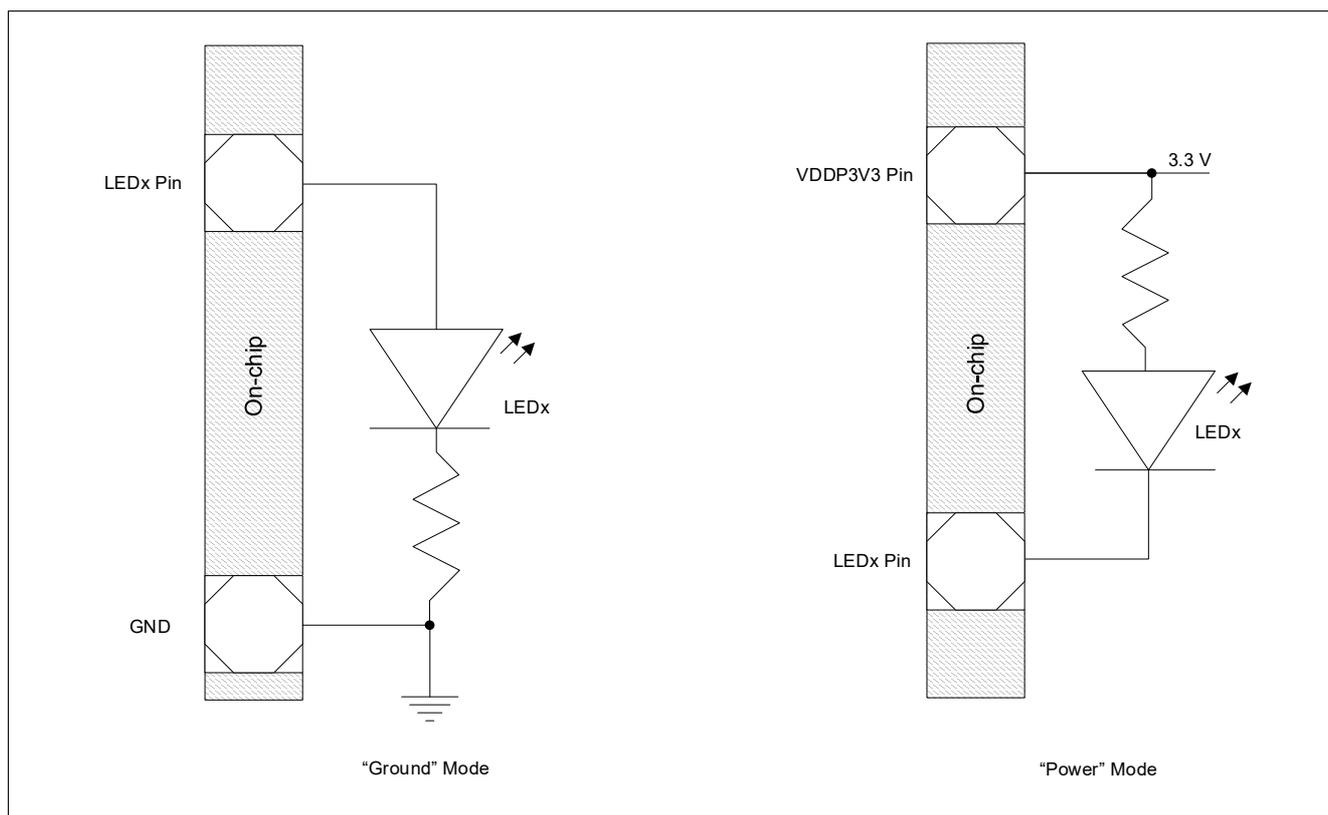


Figure 10 LED Connection Options to Ground or Power Supply

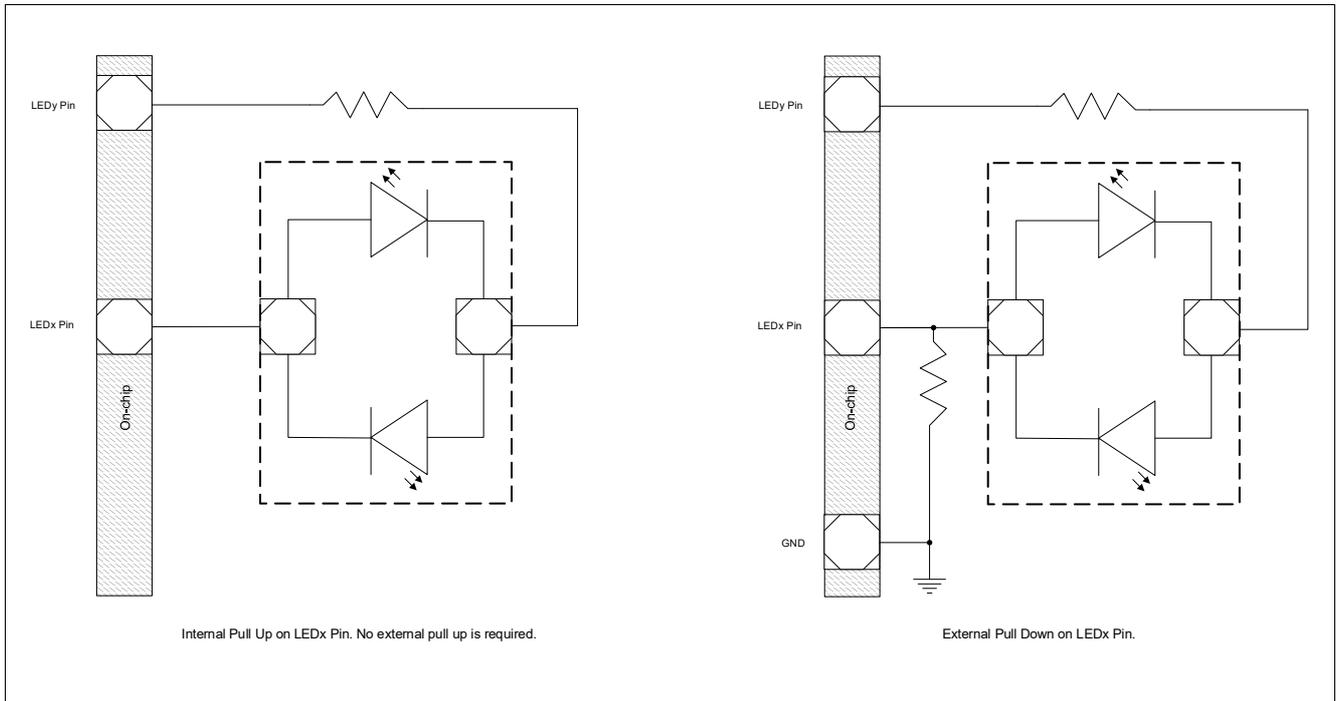


Figure 11 Connection of a Dual Color LED and Configuring Pin Strap Value

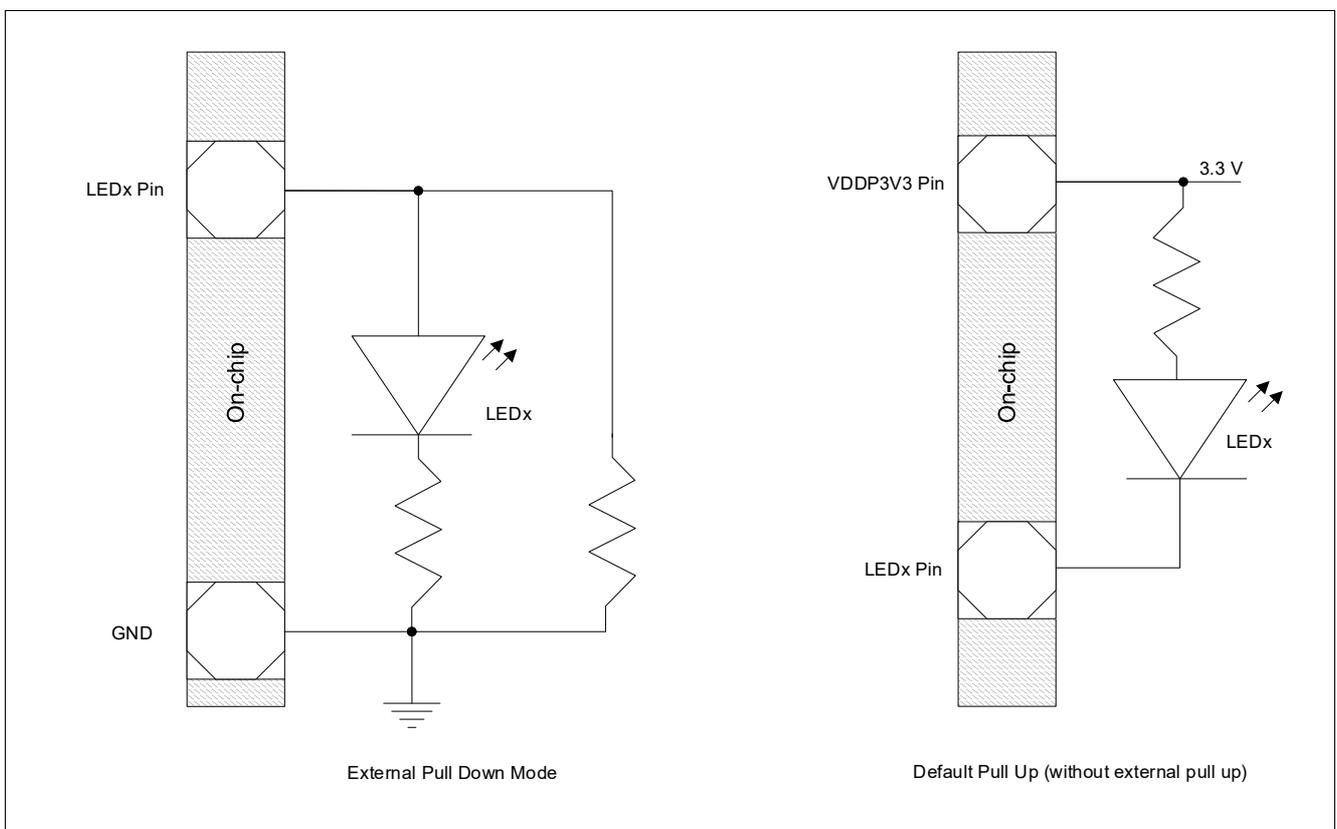


Figure 12 Connection of a Single Color LED and Configuring Pin Strap Value

3.8.3 LED Brightness Control

There are two LED brightness modes configurable by the API [1], based on the system requirement.

- LED Brightness Level Maximum Mode
Fixed level signal (no pulses) for maximum brightness, also available as a control signal for other purposes.
- LED Brightness Level Control Mode (Constant Mode)
Allows the configuration of 16 levels of LED brightness. See [Brightness Control](#).

Brightness Control

This block controls the brightness of the LED by controlling the time duration for which the LED is on/off. The persistence characteristic of the eye causes it to perceive this as LED brightness. When LED is off, the output is disabled. When the LED is on, the output is enabled. The brightness control affects the LED output enable directly.

[Figure 13](#) shows the brightness control frequency is 81.25 Hz, where each period is divided into 64 slots.

In the LED brightness level maximum mode, the LED is enabled in all 64 slots, as shown in brightness level 0 which is the maximum brightness.

In the LED brightness level control mode, the LED is enabled for n consecutive slots, where n is determined by the configured brightness level. [Figure 13](#) shows the brightness level in active low mode, whereby brightness level 15 is the minimum brightness.

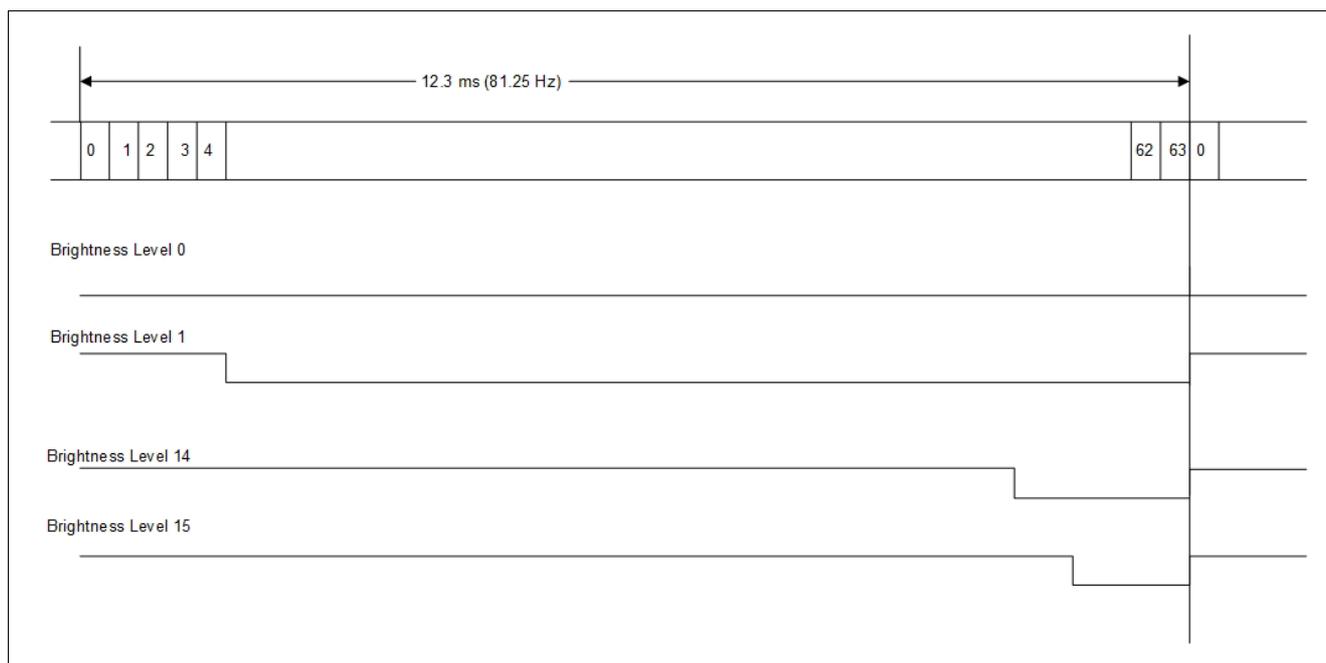


Figure 13 LED Brightness Control by Controlling LED Output Enable/Disable

3.9 Precision Time Protocol

The MxL86289C provides support for the Precision Time Protocol (PTP) feature, which is used to precisely synchronize clocks at the system level. PTP is used to synchronize the time of day (ToD) of slave clocks to a master clock over Ethernet networks. It is standardized in IEEE 1588-2002, and in IEEE 1588-2008 as a second revision (1588v2). The MxL86289C has built-in hardware support to provide high precision and easy to use PTP clock synchronization.

The MxL86289C supports PTP with these features:

- Implementation of a 64-bit counter, which counts with a granularity of 2 ns.
- Two 16 entry deep FIFOs with overflow and underflow support, one FIFO to store the timestamps and CRCs of outgoing packets, and one FIFO to store the timestamps and CRCs of incoming packets.
- Timestamps are captured with high precision in transmitted and received PTP packets when the start of frame delimiter of a packet is detected.
- Timestamps can be triggered by the edge of an input signal to allow synchronous latching of the timestamp of the on-chip counter, and the counter of an external master or slave clock to calculate counter differences. It is possible to select GPC0, GPC1, GPC2, or GPC3 as the input for the trigger signal.
- A recurring pulse signal can be generated either at the GPC0, GPC1, GPC2, or GPC3. The signal can be a Pulse Per Second (PPS) signal or a signal with another configurable frequency.

- **2-step Time Stamping**

This scheme uses a Follow_Up message to carry the time stamp of the corresponding sync message. The time stamp is not inserted in the sync message on the fly while the packet is being transmitted, but later in the next PTP message. This scheme allows the MxL86289C to perform hardware-assisted precise time stamping capture, using the PHY layer to precisely indicate when the packet Start-of-Frame Delimiter (SFD) symbol is sent out or received on the physical layer. The time stamp, together with the corresponding packet CRC, is stored in a memory area on the MxL86289C.

- **1-step Time Stamping**

This scheme is used to reduce the number of PTP messages. In this scheme, the MxL86289C MAC inserts the time stamp in the sync message on the fly when it passes through the MxL86289C MAC layer. The MxL86289C inserts the time stamp in the PTP sync message on the fly.

Attention: 1-step Time Stamping is not supported in transparent mode

3.9.1 PTP Configuration

The MxL86289C API [\[1\]](#) describing the driver software executed on the external processor SoC must be followed to configure this feature.

3.10 Pulse Per Second

The MxL86289C provides support for Pulse Per Second (PPS) signal generation, which is used at the PCB level to synchronize various devices. The general purpose clock pins GPC0, GPC1, GPC2, or GPC3 are configured for this purpose.

3.10.1 PPS Configuration

The MxL86289C API [\[1\]](#) describing the driver software executed on the external processor SoC must be followed to configure this feature.

3.11 Synchronous Ethernet

The MxL86289C allows a Synchronous Ethernet (SyncE) interface to support transportation of a source clock from a clock master to clock clients. When the TPI is a clock slave, the MxL86289C receives the synchronization clock from the Ethernet cable, and provides it to the system on pin GPC0, GPC1, GPC2, or GPC3. When the TPI is a clock master, the MxL86289C receives the clock from the system on pin GPC0, GPC1, GPC2, or GPC3 and sends it over the Ethernet cable as a clock master.

It is configurable to synchronize to one of these clock sources:

- Recovered received clock by SerDes
- Recovered received clock by 2.5G BASE-T PHY
- Input clock via GPC0, GPC1, GPC2, or GPC3

These functions are clocked from the synchronized clock:

- SerDes
- 2.5GBASE-T PHY
- 1588/PTP timers
- Output clock via GPC0, GPC1, GPC2, or GPC3

Loss of signal detection is integrated on chip and all the modules are supplied seamlessly with clocks generated from the local source when the external master clock signal is not available.

3.11.1 SyncE Configuration

The MxL86289C API [\[1\]](#) describing the driver software executed on the external processor SoC must be followed to configure this feature.

3.12 Smart-AZ

The Smart-AZ feature is relevant when the 8-Port 2.5 Gigabit Ethernet PHY is connected to a MAC SoC that does not implement the EEE feature in its MAC layer. In this case, the MAC SoC is not able to initiate a transition to the low-power idle state.

To alleviate the limitation of such a MAC SoC, the MxL86289C detects the conditions that may lead to low-power idle and generates the control messages to enter EEE mode in accordance with the IEEE 802.3az standard.

The Smart-AZ feature is not enabled by default and is not supported in transparent mode.

3.13 Preemption

The IEEE 802.3br [3] and IEEE 802.1Qbu standards [12] introduced a one-level Ethernet frame preemption paradigm. In this approach, frames transmitted through a switch output port are classified as express frames or preemptable frames, depending on their priority levels. Express frames are able to preempt preemptable frames. Two frames belonging to the same class are not able to preempt each other. This allows the transmission of non-critical frames to be interrupted by critical frames, hence avoiding critical frames being blocked for long periods of time.

The MxL86289C does not preempt any Ethernet frames or change the order of the Ethernet frames. However, it is preemption-aware and able to identify the various preemption classes. The PCH transports preemption information over the USXGMII interface, consequently the MxL86289C also supports this feature in the PCH.

This feature is relevant in a Time Sensitive Network.

Attention: Preemption is only supported in transparent mode when the MxL86289C is not operating in 10BASE-T. Preemptable frames are dropped in SmartAZ mode.

3.14 Power Management

This section describes the power management functions of the MxL86289C integrated Ethernet PHY.

3.14.1 Power States

Figure 14 illustrates the power states and transitions of each integrated Ethernet PHY.

In this state diagram, the (0.11) syntax corresponds to the value of bit 11 from register 0 in device 0, which is `STD_CTRL.PD`. This is the Power Down (PD) bit in `MDIO STD_CTRL`, described in Chapter 4. The STA is able to use this `STD_CTRL.PD` field to bring the physical interface into the **POWER DOWN State**.

The other states are automatically entered by the MxL86289C depending on the context, and following the EEE protocol. This is done without any intervention from the STA.

The Normal Link Pulse (NLP) and Fast Link Pulse (FLP) are received on the TPI from a link partner and used to wake up the MxL86289C and enter auto-negotiation.

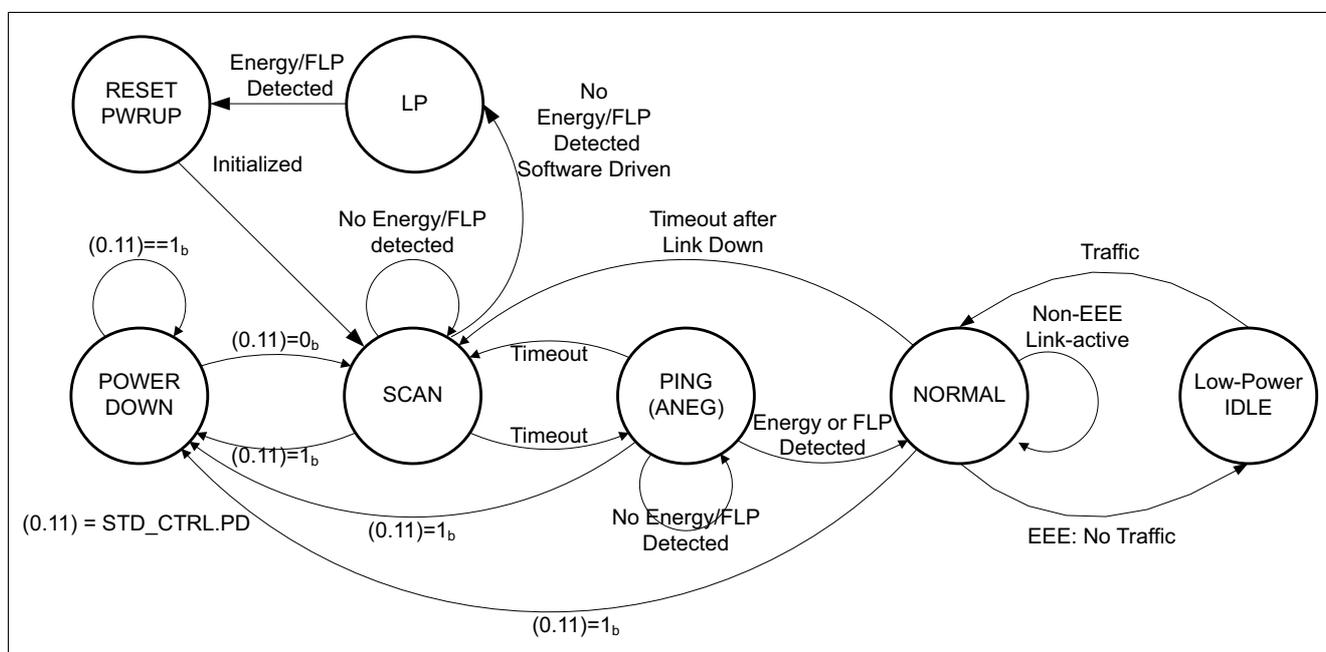


Figure 14 State Diagram for Power Down State Management

3.14.2 RESET PWRUP

The MxL86289C starts up in the RESET Power Up (PWRUP) state after either a hardware reset or power up. After initialization, the PHYs always transition to the **SCAN (ANEG) State**.

3.14.3 POWER DOWN State

The **POWER DOWN State** is entered by setting the PD bit (0.11) of the MDIO standard register `STD_CTRL` to 1, regardless of the current state of the device. The **POWER DOWN State** corresponds to power down as specified in IEEE 802.3, Clause 22.2.4.1.5. Some signal processing blocks are stopped to save energy, but the MxL86289C still responds to MDIO messages.

Exiting the **POWER DOWN State** is triggered by setting the PD bit (0.11) of `STD_CTRL` to 0, which initiates a transition to the **SCAN (ANEG) State**.

3.14.4 SCAN (ANEG) State

The SCAN state differs from the **POWER DOWN State** in that the receiver periodically scans for signal energy or FLP bursts on the TPI. There is no transmission in this state. When an FLP burst is received, the MxL86289C enters the auto-negotiation protocol to exchange capabilities with the link partner and establish a data link in the **NORMAL State**.

3.14.5 PING (ANEG) State

The PING state is similar to the **SCAN (ANEG) State** except that the transceiver transmits an FLP burst onto the TPI for a programmable amount of time. This is used to wake potential link partners from the **POWER DOWN State**. This state corresponds to the state of ANEG described in Clause 28 of the IEEE standard [3].

3.14.6 Low-Power State

The MxL86289C's Low-Power (LP) state is enabled by configuring the MDIO register `PHY_CTL2.LP`. The LP state is entered automatically when there is no Ethernet cable connected to the MxL86289C. The MxL86289C firmware detects this condition when no energy or Link Pulse is present on the TPI and enters the LP state. It is intended to set the MxL86289C into its maximum power saving state. In this state, most digital domains are in reset. Only a minimal amount of circuitry (analog/digital) operates to detect signal energy on the receiver of a TPI and trigger a wake-up.

When the port is in the LP state, the STAs do not have access to the corresponding MDIO/MMD registers.

The LP state is exited upon detection of signal energy on the twisted pair (either NLP or FLP). The port transitions to the **RESET PWRUP** state automatically. The STA host is also able to trigger an LP state exit by applying an API [1] to wake up the specific port that entered the LP state.

It is possible for the STA host to be informed of the LP entry condition. By setting the `PHY_IMASK.LP` bit to ACTIVE, the STA requests the MDINT interrupt from the port when the entry conditions are met. **Figure 15** shows all the LP related control bits and communication mechanism between the STA and the MxL86289C.

It is possible for the STA host to be informed of the LP exit condition. By setting the `VSPEC1_IMASK.CDET` bit to ACTIVE, the STA requests the MDINT interrupt from the port when energy on the link is detected during auto-negotiation. Even when none of the ports are in the LP state, this interrupt is triggered whenever energy is first detected on the link. When the STA triggers the LP state exit via a wake-up request, and there is no energy on the link after the LP state exit, no interrupt is asserted.

Attention: An active-high MDINT in push-pull mode (default is tristate mode) is not supported in the LP mode.

Attention: VSPEC1_IMASK.CDET is not supported in forced speed 10BASE-T/100BASE-TX mode. Auto-negotiation is required to support this feature.

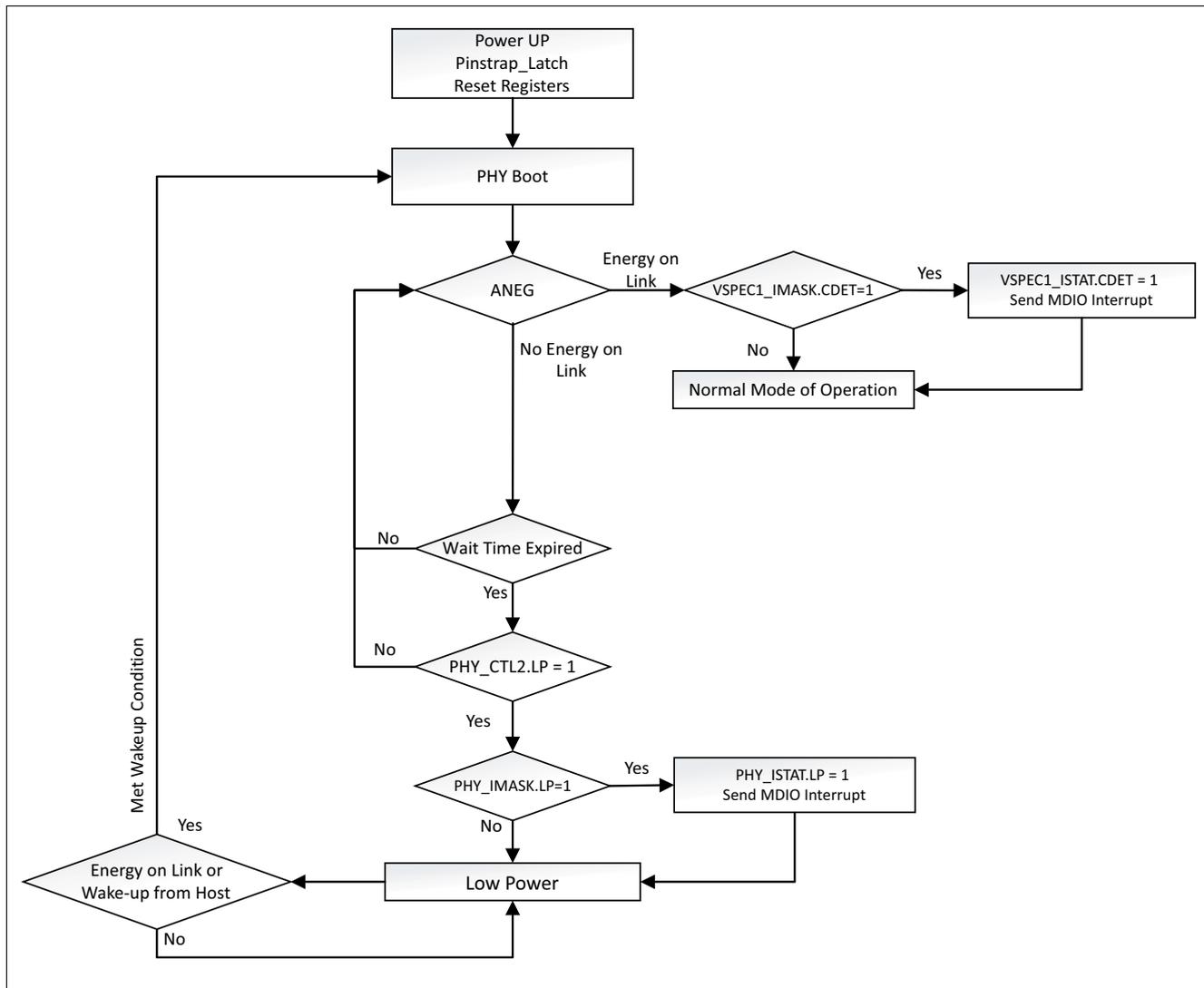


Figure 15 Low Power Sequence

Table 24 Low Power State Entry and Exit Sequence

| Step | State | Remark |
|------|--|---|
| 1 | ACTIVE The LP feature is enabled by setting <code>PHY_CTL2.LP = 1</code> | Use the MDIO register <code>PHY_CTL2.LP</code> to enable or disable the LP feature. |
| 2 | ANEG, Ability Detect | The firmware detects no energy on the cable when no FLP is received for a long period of time. When the LP feature is not enabled, this time is fixed to between 6.4 and 9.6 seconds. When the LP feature is enabled, this time is configured using the <code>VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM</code> register. Time in seconds = 4 x value programmed. Default time is 4 seconds. (<code>VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM = 1</code>). There is an initial time of between 2.4 and 5.6 seconds, which adds on to the programmed time. |
| 3 | LP Entry Timer | This time is configured with the <code>VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM</code> register. The value is set in steps of 4 seconds. The default time is 4 seconds. |
| 4 | LP Entry | The MxL86289C saves MDIO LP persistent registers. An interrupt is sent to indicate entry into the LP state. |
| 5 | LP State | Power consumption is saved in this state. The MxL86289C listens to energy pulses from the link partner ANEG as a condition to trigger an exit from the LP state. Only a minimal amount of circuitry operates to detect signal energy on TPI and trigger a wake-up. The port LEDs and MDIO interface are disabled. |
| 6 | LP Exit (Option 1) Based on energy detected on the cable | The MxL86289C restores the configurations in the MDIO registers. An interrupt is sent to indicate an exit from the LP state. |
| 7 | LP Exit (Option 2) Based on a wake-up request from the STA | The STA is able to request an LP exit by using a provided API. The MxL86289C restores the configurations in the MDIO registers. No interrupt is sent to notify LP exit. Since MDIO/MMD register access is unavailable for ports in the low power state, this option is only available if there is at least one port not in the low power state. |
| 8 | ANEG, LINK-UP, and ACTIVE | The MxL86289C operates in normal power modes. |

These are persistent MDIO registers saved and restored during LP entry-exit.

1. STD_CTRL.SSM
2. STD_CTRL.DPLX
3. STD_CTRL.ANEN
4. STD_CTRL.SSL
5. STD_AN_ADV.TAF
6. STD_AN_ADV.XNP
7. STD_GCTRL.MBTHD
8. STD_GCTRL.MBTDF
9. STD_GCTRL.MSPT
10. STD_GCTRL.MS
11. STD_GCTRL.MSEN
12. PHY_IMASK
13. PHY_CTL1.AMDIX
14. PHY_CTL1.MDIAB
15. PHY_CTL1.MDICD
16. PHY_CTL1.POLA
17. PHY_CTL1.POLB
18. PHY_CTL1.POLC
19. PHY_CTL1.POLD
20. PHY_CTL2.LPI
21. PHY_CTL2.ANPD
22. PHY_CTL2.PSCL
23. PHY_CTL2.LP
24. PHY_CTL2.STICKY
25. PHY_CTL2.SDETP
26. PHY_LED
27. ANEG_CTRL.ANEG_ENAB
28. ANEG_MGBT_AN_CTRL.LDL
29. ANEG_MGBT_AN_CTRL.FR
30. ANEG_MGBT_AN_CTRL.FR2G5BT
31. ANEG_MGBT_AN_CTRL.AB2G5BT
32. ANEG_MGBT_AN_CTRL.PT
33. ANEG_MGBT_AN_CTRL.MS_MAN_EN
34. ANEG_MGBT_AN_CTRL.MSCV
35. ANEG_EEE_AN_ADV1.EEE_100BTX
36. ANEG_EEE_AN_ADV1.EEE_1000BT
37. ANEG_EEE_AN_ADV2.EEE2G5
38. ANEG_MGBT_AN_CTRL2.THPBYP2G5
39. VSPEC1_NBT_DS_CTRL.NO_NRG_RST
40. VSPEC1_NBT_DS_CTRL.DOWNSHIFTEN
41. VSPEC1_NBT_DS_CTRL.DOWNSHIFT_THR
42. VSPEC1_NBT_DS_CTRL.NRG_RST_CNT
43. VSPEC1_NBT_DS_CTRL.FORCE_RST
44. VSPEC1_LED0
45. VSPEC1_LED1
46. VSPEC1_PM_CTRL
47. VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM
48. VSPEC1_IMASK
49. VSPEC1_FRCTL.CAP_EXT
50. VSPEC1_FRCTL.CAP_TXDIS

- 51. VSPEC1_FRCTL.CAP_THPBYP
- 52. VSPEC1_FRCTL.CAP_CISCO
- 53. VSPEC1_FRCTL.CAP_IEEE
- 54. VSPEC1_FRCTL.MAX_FR_RETRY
- 55. VSPEC2_WOL_CTRL
- 56. VPSPEC2_WOL_AD01
- 57. VPSPEC2_WOL_AD23
- 58. VPSPEC2_WOL_AD45
- 59. VPSPEC2_WOL_PW01
- 60. VPSPEC2_WOL_PW23
- 61. VPSPEC2_WOL_PW45

3.14.7 NORMAL State

The NORMAL state is used to establish and maintain a link connection. When a connection is dropped, the MxL86289C moves back into the [SCAN \(ANEG\) State](#).

3.14.8 Low Power IDLE State - Energy-Efficient Ethernet

The IEEE 802.3 standard [3] describes the EEE operation supported by the MxL86289C in the various speeds of 100BASE-TX, 1000BASE-T, and 2.5GBASE-T. The general idea of EEE is to save power during periods of low link utilization. Instead of sending active idle data, the transmitters are switched off for a short period of time. This is called the quiet period. The link is kept active by means of a frequent refresh cycle initiated by the PHY itself while in the low power state. This sequence is repeated until a wake request is generated by one of the link partner MACs. The MxL86289C follows the IEEE 802.3 standard regarding EEE. Figure 16 illustrates the principle. This state is entered automatically when the low power idle conditions are met.

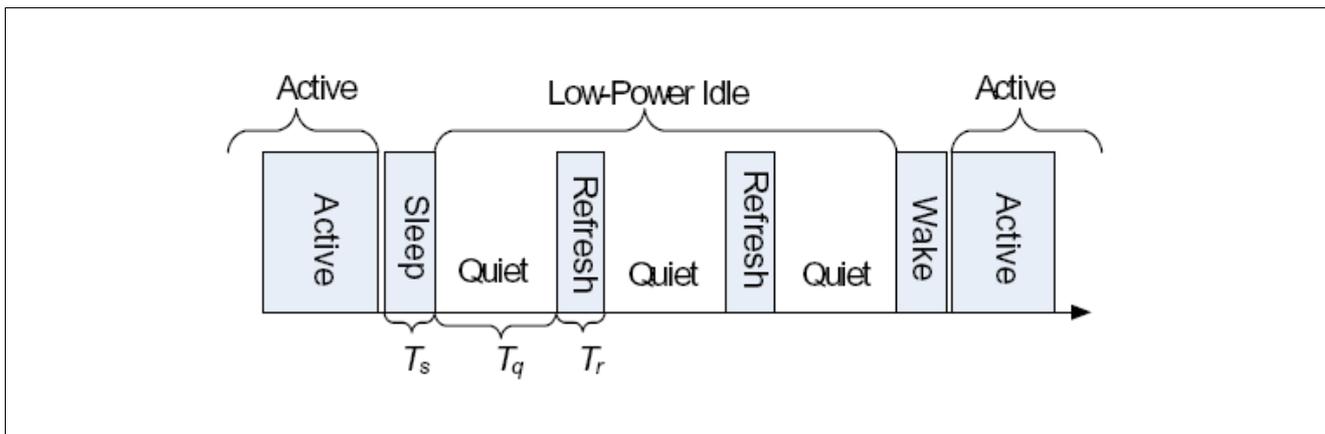


Figure 16 EEE Low Power Idle Sequence

3.15 Firmware Upgrade

The MxL86289C provides a Firmware Upgrade feature that allows feature and functional enhancements of the MxL86289C in the field.

It is possible to download a new firmware image via the MxL86289C's **MDIO Slave Interface** to a serial flash memory device connected to the MxL86289C's QSPI. The MxL86289C is then able to fetch the upgraded firmware from the flash memory after a reboot.

For Security Development Lifecycle (SDL) [13] reasons, the MxL86289C only accepts firmware images electronically signed by MaxLinear. When authentication of the flash image by the MxL86289C fails, or the download of the image is aborted or fails, the MxL86289C resets and wait for a new image to be downloaded.

In flashless mode, the host MAC SoC must transfer the MxL86289C's firmware image into the MxL86289C's on-chip memory at the MxL86289C's boot-up time. MaxLinear will provide the procedure to facilitate the firmware transfer. To upgrade the MxL86289C's firmware image, the device must be put into the reset state and restarted. This allows the usual **Power-On Sequence** to occur with the newly upgraded firmware image to be downloaded over the MDIO slave interface using a dedicated MDIO address. Once the firmware image has been transferred to the MxL86289C's on-chip memory, it is authenticated. After successfully authenticating the image, the MxL86289C continues with normal boot process. If authentication fails, or the image download fails or is aborted, the MxL86289C resets and waits for the host MAC SoC to restart the process.

The supported options for upgrading the firmware image are:

- The firmware is upgradeable over the MDIO slave interface to the flash memory device.
- Firmware download over the MDIO slave interface with MDIO address 0x1F to on-chip memory in flashless mode.
- In addition firmware download into "empty" flash is supported over MDIO slave interface.

Attention: The MDIO slave interface for firmware download or upgrade supports IEEE 802.3 Clause 22 only.

Attention: The MDIO address for firmware download or upgrade to flash is defined by the pin strapping in Table 17 with the lowest three bits equal to 0.

Attention: After the firmware upgrade to the flash memory is completed, the MxL86289C must be rebooted such that the new image is authenticated. The same requirement also applies to flash memory devices that are programmed directly by customers, which do not use the firmware upgrade procedure provided in this section.

The procedure to download firmware over the MDIO slave interface is documented in [2]. It provides information on the update/download process and which actions are required in the MAC SoC application.

Security feature to prevent flash memory wear-out due to frequent updates (flash anti-wear out) is not supported within the MxL86289C. When the system to which the MxL86289C is attached mandates such features, they must be supported by the system itself. Flash memory components typically support a minimum of 100,000 erase/program cycles, so flash wear-out is unlikely. However, ensuring a minimum interval between flash updates decreases the likelihood of wear-out. An interval of one hour sets the minimum time before wear-out to longer than 11 years. The system is also expected to ensure that the firmware is only installed when a new firmware is available and does not attempt to install a new firmware after every reboot in flash mode.

Security feature to prevent rollback of the image to a previous version (anti-rollback) is supported within the MxL86289C. The MxL86289C verifies that the new firmware has a higher or same security version number (SVN) than the previously installed firmware before executing it. If this step fails due to the firmware SVN being a lower version, the MxL86289C resets itself and waits for the host SoC to download a new image to the flash memory over the MDIO slave interface. In flashless mode, the MxL86289C resets itself and waits for the host MAC SoC to restart the firmware transfer process. If the system does not desire to have this anti-rollback feature, MaxLinear will deliver firmware images with fixed SVN, such that the security check will always pass.

4 MDIO and MMD Register Interface Description

This chapter describes the MDIO and MMD registers available to support the MxL86289C feature set. These registers are accessible by an external management entity (called STA in IEEE) to control, configure, or read the status of the MxL86289C. After power-on, the MxL86289C resets the MDIO and MMD registers to default values sufficient to operate without specific programming.

All the register definitions, behaviors, and fields are strictly compliant with IEEE 802.3. Refer to IEEE 802.3 [3] for more information about the registers. The only registers not referenced in IEEE 802.3 are two register groups that are vendor-specific: VSPEC1 and VSPEC2. These allow custom functions related to MxL86289C.

In the register descriptions, the section or table references refer to the IEEE 802.3 [3].

4.1 MDIO-specific Terminology

This list describes how the common IEEE 802.3 terms relate to MDIO and MMD register concepts discussed in this chapter.

- **STA:** Station Management. A host connected to the MDIO interface. STAs are generally Media Access Controllers (MACs). The STA drives the MDIO bus as a clock master and the MxL86289C is an MDIO slave.
- **Host:** Used as a synonym of STA in this document.
- **PHY:** Physical Layer. In the MxL86289C, this encompasses Analog Signal Processing, Digital Signal Processing, and Physical Coding Sublayer (PCS). The PHY contains several sublayers that are individually manageable entities known as MDIO manageable devices (MMDs).
- **MMD:** MDIO Manageable Device. The list of MMDs available in the MxL86289C is in [Section 4.3](#).
- **Device:** In the context of the MDIO/MMD registers, a device is a register bank grouped by logical sublayers of the PHY layer.
- **Clause:** Refers to a particular section of the IEEE 802.3 standard [3]. In particular, Clause 22 describes MDIO device 0 and Clause 45 describes the other MMDs.
- **MII:** Media Independent Interface. This encompasses the MDIO and the (G)MII as described in Clause 22. STD registers in device 0 are also called MII registers.

4.2 Register Naming and Numbering

The register numbering convention in this document is similar to that of IEEE 802.3.

The numbering syntax uses three numbers, a.b.c, as specified in IEEE 802.3, paragraph 45.1 [3], and the notation is generalized to Clause 22 registers in device 0 STD. The alphanumeric syntax also uses the same structure and uses the names of the MMD devices, registers, and register fields separated by underscores and dots.

4.2.1 Register Numbering

The syntax is as follows, with a, b, and c written as decimal numbers:

a.b.c = <DEVICE_NUMBER>.<REGISTER_NUMBER>.<FIELD_NUMBER>

When the last indicator (c) is omitted, the register numbering refers to the full register.

When a field is more than a single bit, the bit range is indicated using a colon (for example, 1:3 is the field of bits 1 to 3). In an MDIO register, the least significant bit is bit 0 and most significant bit is bit 15. All MDIO registers are 16-bit wide.

4.2.2 Register Naming

The syntax is as follows, with AA, BB, and CC written as alphanumeric strings:

AA_BB.CC = <DEVICE_NAME>.<REGISTER_NAME>.<FIELD_NAME>

When the last indicator (CC) is omitted, the register naming refers to the full register.

The fields named RES, RES1, and RES2 refer to reserved fields as per IEEE 802.3.

4.2.3 Examples

STD_STAT.ANOK is the name of the field 0.1.5, which indicates that auto-negotiation is complete.

ANEG_CTRL.ANEG_RESTART is the name of the field 7.0.9, which allows the STA to restart the Ethernet ANEG procedure.

ANEG_PHYID1 is the complete 16-bit register number 7.2, for the PHY identifier 1 number.

VSPEC1_LED1.BLINKS is the 4-bit wide field number 30.2.15:12, which contains LED1 slow blinking configuration.

4.3 MMD Devices Present in MxL86289C

The MMD devices implement groups of standardized registers under the management of the STA.

Table 25 MDIO/MMD Devices Present in MxL86289C

| MDIO/MMD Name | Device Number (decimal) | Description |
|---------------|-------------------------|--|
| STD | 0 | MDIO Standard Device as described in Clause 22. This also contains a number of MxL86289C-specific PHY registers. |
| PMA/PMD | 1 | Control and status registers related to the PMA/PMD signal processing modules |
| PCS | 3 | Control and status registers related to the PCS encoding/decoding device |
| ANEG | 7 | Control and status registers related to the auto-negotiation device |
| VSPEC1 | 30 | MxL86289C-specific LED control and other MxL86289C-specific control |
| VSPEC2 | 31 | MxL86289C-specific WoL control |

4.4 Responsibilities of the STA

The MxL86289C responds to all published register addresses for the device and returns a value of zero for undefined and unsupported registers.

In accordance with IEEE 802.3 guidelines, it is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs of the MxL86289C.

The MxL86289C ignores writes to the PMA/PMD speed selection bits that select speeds not advertised in the PMA/PMD speed ability register. The PMA/PMD speed selection defaults to a supported ability.

4.5 MDIO Access Protocols to Read / Write Registers

All the MDIO/MMD registers are accessible from an external chip connected to the MDIO bus on the MDIO_S and MDC_S pins. The MxL86289C supports several MDIO frame protocols:

- Clause 22: To access Device 0
- Clause 22 Extended: To access other devices using the indirection scheme specified by IEEE 802.3
 - Dev 1: PMAPMD
 - Dev 3: PCS
 - Dev 7: ANEG
 - Dev 30: VSPEC1
 - Dev 31: VSPEC2
- Clause 45: to access all devices

Both Clause 22 Extended and Clause 45 are used to access MMD devices. However, the mechanism implemented in the MxL86289C provides faster speeds using Clause 45. It creates differences in latencies in the MDIO reply:

- The Clause 22 Extended protocol involves an indirect mechanism.
- The Clause 45 protocol provides faster replies.

The Clause 22 registers are accessed using the Clause 45 electrical interface and the Clause 22 management frame structure. Refer to IEEE 802.3 section 45 [\[3\]](#).

5 MDIO Registers Detailed Description

Table 26 Register Access Type

| Mode | Symbol |
|--|--------|
| Read-Only Register (Status or Ability Register) | RO |
| Read-Write Register (MDIO Register) | RW |
| Read-Write Self-Clearing Register (bit cleared after read from MDIO) | RWSC |
| Read-Only Self-Clearing Register (bit cleared after read from MDIO) | ROSC |
| Read-Only Latching Low Register | ROLL |
| Read-Only Latching High Register | ROLH |

5.1 Standard Management Registers

This section describes the IEEE 802.3 standard management registers corresponding to Clause 22.

Table 27 Registers Overview- Standard Management Registers

| Register Short Name | Register Long Name | Reset Value |
|-----------------------------|--|---------------------------------|
| STD_CTRL | STD Control (Register 0.0) | 3040 _H |
| STD_STAT | Status Register (Register 0.1) | 7949 _H |
| STD_PHYID1 | PHY Identifier 1 (Register 0.2) | C133 _H |
| STD_PHYID2 | PHY Identifier 2 (Register 0.3) | 5400 _H ¹⁾ |
| STD_AN_ADV | Auto-Negotiation Advertisement (Register 0.4) | 9DE1 _H |
| STD_AN_LPA | Auto-Negotiation Link Partner Ability (Register 0.5) | 1DE0 _H |
| STD_AN_EXP | Auto-Negotiation Expansion (Register 0.6) | 0064 _H |
| STD_AN_NPTX | Auto-Negotiation Next Page Transmit Register (Register 0.7) | 2001 _H |
| STD_AN_NPRX | Auto-Negotiation Link Partner Received Next Page Register (Register 0.8) | 0000 _H |
| STD_GCTRL | Gigabit Control Register (Register 0.9) | 0200 _H |
| STD_GSTAT | Gigabit Status Register (Register 0.10) | 0000 _H |
| STD_MMDCTRL | MMD Access Control Register (Register 0.13) | 0000 _H |
| STD_MMDDATA | MMD Access Data Register (Register 0.14) | 0000 _H |
| STD_XSTAT | Extended Status Register (Register 0.15) | 2000 _H |

1) For the device specific reset value, see the Product and Package Naming table in the [Product Ordering Information](#) chapter.

5.1.1 Standard Management Register Descriptions

This section describes all the STD registers in detail.

STD Control (Register 0.0)

This register controls the main functions of the PHY.

IEEE Standard Register=0.0

STD_CTRL

STD Control (Register 0.0)

Reset Value

3040_H

| | | | | | | | | | | | |
|------------|-----------|------------|-------------|-----------|-------------|-------------|-------------|------------|------------|---|------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 0 |
| RST | LB | SSL | ANEN | PD | ISOL | ANRS | DPLX | COL | SSM | | RES |
| RWSC | RW | RW | RW | RW | RW | RWSC | RW | RW | RW | | RO |

| Field | Bits | Type | Description |
|-------|------|------|---|
| RST | 15 | RWSC | <p>Reset Resets the PHY to its default state. Active links are terminated. This is a self-clearing bit, which is set to zero by the hardware after a reset is performed.</p> <p>0_B NORMAL Normal operational mode 1_B RESET Resets the device.</p> |
| LB | 14 | RW | <p>Loopback on GMII This mode enables looping back of MII data from the transmit to the receive direction. No data is transmitted to the Ethernet PHY. The device operates at the selected speed. The collision signal remains de-asserted unless otherwise forced by the collision test.</p> <p>0_B NORMAL Normal operational mode 1_B ENABLE Closes the loopback from Tx to Rx at xMII.</p> |
| SSL | 13 | RW | <p>Forced Speed Selection LSB This bit only takes effect when bit ANEN is set to zero, which disables the auto-negotiation process. This is the lower bit (LSB) of the forced speed selection and is used in conjunction with the higher bit (MSB). The standard procedure to force 2500 Mbps operation (when ANEG is disabled) is to program PMA_CTRL with 1.0.6 = 1.0.13 = 1 and 1.0.5:2 = [0 1 1 0]. The GPHY mirrors 1.0.6, 1.0.13 and 0.0.6, 0.0.13. This is the MSB LSB bit value encoding:</p> <p>00_B 10 Mbps 01_B 100 Mbps 10_B 1000 Mbps 11_B Reserved, defaults to 2500 Mbps operation when the PMA_CTRL register 1.0.5:2 equals [0 1 1 0].</p> |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|--|
| ANEN | 12 | RW | Auto-Negotiation Enable Allows enabling and disabling of the auto-negotiation process capability of the PHY. When enabled, the force bits for duplex mode (CTRL.DPLX) and the speed selection (CTRL.SSM, CTRL.SSL) become inactive; otherwise, the force bits define the PHY operation. 0 _B DISABLE Disables the auto-negotiation protocol. 1 _B ENABLE Enables the auto-negotiation protocol. |
| PD | 11 | RW | Power Down Forces the device into a power down state (SLEEP) in which power consumption is the bare minimum required to still maintain the MII management interface communication. When activating the power down functionality, the PHY terminates active data links. The MII interface is also stopped in power down mode. 0 _B NORMAL Normal operational mode 1 _B POWERDOWN Forces the device into power down mode. |
| ISOL | 10 | RW | Isolate The isolation mode isolates the PHY from the MAC. The MAC interface inputs are ignored, whereas the MAC interface outputs are set to tristate (high-impedance). 0 _B NORMAL Normal operational mode 1 _B ISOLATE Isolates the PHY from the MAC. |
| ANRS | 9 | RWSC | Restart Auto-Negotiation Restarts the auto-negotiation process on the MDI. This bit does not have any effect when auto-negotiation is disabled using CTRL.ANEN. This bit is self-clearing after the auto-negotiation process is initiated. 0 _B NORMAL Stays in current mode. 1 _B RESTART Restarts auto-negotiation. |
| DPLX | 8 | RW | Forced Duplex Mode This bit only takes effect when bit CTRL.ANEN is set to zero, which disables the auto-negotiation process. This bit controls the forced duplex mode. It allows forcing of the PHY into full-duplex or half-duplex mode. This bit does not take effect in loopback mode, when bit CTRL.LB is set to 1 _B . It is only possible to force the duplex mode to half-duplex in 10BASE-T and 100BASE-TX speed modes. This field is ignored for higher speeds. 0 _B HD Half-duplex 1 _B FD Full-duplex |
| COL | 7 | RW | Collision Test Allows testing of the COL signal at the xMII interface. When the collision test is enabled, the state of the TX_EN signal is looped back to the COL signal within a minimum latency. 0 _B DISABLE Normal operational mode 1 _B ENABLE Activates the collision test. |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|---|
| SSM | 6 | RW | <p>Forced Speed Selection MSB</p> <p>This bit only takes effect when bit ANEN is set to zero, which disables the auto-negotiation process. This is the higher bit (MSB) of the forced speed selection and is used in conjunction with the lower bit (LSB).</p> <p>The preferred way to force 2500 Mbps operation (when ANEG is disabled) is to program PMA_CTRL with 1.0.6 = 1.0.13 = 1 and 1.0.5:2 = [0 1 1 0].</p> <p>The GPHY mirrors 1.0.6, 1.0.13 and 0.0.6, 0.0.13.</p> <p>This is the MSB LSB bit value encoding:</p> <p>00_B 10 Mbps 01_B 100 Mbps 10_B 1000 Mbps 11_B Reserved, defaults to 2500 Mbps operation when the PMA_CTRL register 1.0.5:2 equals [0 1 1 0].</p> |
| RES | 5:0 | RO | <p>Reserved</p> <p>Write as zero, ignore on read.</p> |

Status Register (Register 0.1)

This register contains status and capability information about the device. All the bits are read-only. A write access by the MAC does not have any effect. Refer to IEEE 802.3 22.2.4.2.

IEEE Standard Register=0.1

STD_STAT
Reset Value
Status Register (Register 0.1)
7949_H

| | | | | | | | | | | | | | | | | |
|-------------|-------------------|-------------------|-------------|-------------|--------------|-------------------|------------|------------|-------------|-------------|-----------|-------------|-----------|-----------|-------------|----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| CBT4 | CBTX F | CBTX H | XBTF | XBTH | CBT2F | CBT2 H | EXT | RES | MFPS | ANOK | RF | ANAB | LS | JD | XCAP | |
| ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | rolh | ro | roll | rolh | ro |

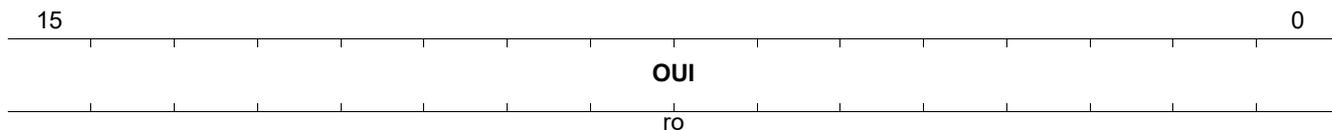
| Field | Bits | Type | Description |
|-------|------|------|---|
| CBT4 | 15 | RO | IEEE 100BASE-T4 Specifies the 100BASE-T4 ability. 0 _B DISABLED PHY does not support this mode. 1 _B ENABLED PHY supports this mode. |
| CBTXF | 14 | RO | IEEE 100BASE-TX Full Duplex Specifies the 100BASE-TX full duplex capability. 0 _B DISABLED PHY does not support this mode. 1 _B ENABLED PHY supports this mode. |
| CBTXH | 13 | RO | IEEE 100BASE-TX Half-Duplex Specifies the 100BASE-TX half-duplex capability. 0 _B DISABLED PHY does not support this mode. 1 _B ENABLED PHY supports this mode. |
| XBTF | 12 | RO | IEEE 10BASE-T Full-Duplex Specifies the 10BASE-T full-duplex capability. 0 _B DISABLED PHY does not support this mode. 1 _B ENABLED PHY supports this mode. |
| XBTH | 11 | RO | IEEE 10BASE-T Half-Duplex Specifies the 10BASE-T half-duplex capability. 0 _B DISABLED PHY does not support this mode. 1 _B ENABLED PHY supports this mode. |
| CBT2F | 10 | RO | IEEE 100BASE-T2 Full-Duplex Specifies the 100BASE-T2 full-duplex capability. 0 _B DISABLED PHY does not support this mode. 1 _B ENABLED PHY supports this mode. |
| CBT2H | 9 | RO | IEEE 100BASE-T2 Half-Duplex Specifies the 100BASE-T2 half-duplex capability. 0 _B DISABLED PHY does not support this mode. 1 _B ENABLED PHY supports this mode. |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|---|
| EXT | 8 | RO | Extended Status The extended status registers are used to specify 1000 Mbps speed capabilities in the register XSTAT. 0 _B DISABLED No extended status information available in register 15 1 _B ENABLED Extended status information available in register 15 |
| RES | 7 | RO | Reserved Ignore when read. |
| MFPS | 6 | RO | Management Preamble Suppression Specifies the Management Frame (MF) preamble suppression ability. 0 _B DISABLED PHY requires management frames with preamble. 1 _B ENABLED PHY accepts management frames without preamble. |
| ANOK | 5 | RO | Auto-Negotiation Completed Indicates whether the auto-negotiation process is completed or in progress. 0 _B RUNNING Auto-negotiation process is in progress. 1 _B COMPLETED Auto-negotiation process is completed. |
| RF | 4 | ROLH | Remote Fault Indicates the detection of a remote fault event. GPHY does not indicate RF. 0 _B INACTIVE No remote fault condition detected 1 _B ACTIVE Remote fault condition detected |
| ANAB | 3 | RO | Auto-Negotiation Ability Specifies the auto-negotiation ability. 0 _B DISABLED PHY is not able to perform auto-negotiation. 1 _B ENABLED PHY is able to perform auto-negotiation. |
| LS | 2 | ROLL | Link Status Indicates the link status of the PHY to the link partner. 0 _B INACTIVE The link is down. No communication with link partner possible. 1 _B ACTIVE The link is up. Data communication with link partner is possible. |
| JD | 1 | ROLH | Jabber Detect Indicates that a jabber event was detected. 0 _B NONE No jabber condition detected 1 _B DETECTED Jabber condition detected |
| XCAP | 0 | RO | Extended Capability Indicates the availability and support of extended capability registers. 0 _B DISABLED Only base registers are supported. 1 _B ENABLED Extended capability registers are supported. |

PHY Identifier 1 (Register 0.2)

This code specifies the Organizationally Unique Identifier (OUI), and the vendor's model and revision number.
IEEE Standard Register=0.2

STD_PHYID1 **Reset Value**
PHY Identifier 1 (Register 0.2) **C133_H**



| Field | Bits | Type | Description |
|-------|------|------|--|
| OUI | 15:0 | RO | Organizationally Unique Identifier Bits 3:18 |

PHY Identifier 2 (Register 0.3)

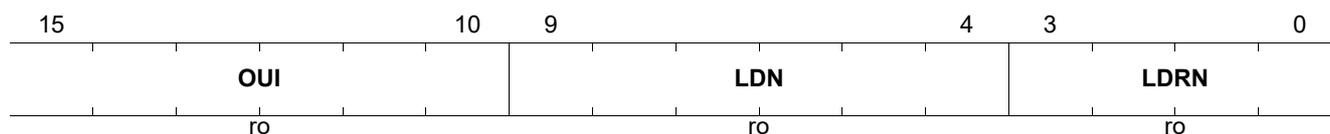
IEEE Standard Register=0.3

STD_PHYID2

PHY Identifier 2 (Register 0.3)

Reset Value

5400_H



| Field | Bits | Type | Description |
|-------|-------|------|---|
| OUI | 15:10 | RO | Organizationally Unique Identifier Bits 19:24 |
| LDN | 9:4 | RO | Device Number Specifies the device number ¹⁾ to distinguish between several different products. |
| LDRN | 3:0 | RO | Device Revision Number Specifies the device revision number ¹⁾ to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the [Product Ordering Information](#) chapter.

Auto-Negotiation Advertisement (Register 0.4)

This register contains the advertised abilities of the PHY during auto-negotiation.

IEEE Standard Register=0.4

STD_AN_ADV

Auto-Negotiation Advertisement (Register 0.4)

Reset Value

9DE1_H

| | | | | | | | | | | | |
|-----------|------------|-----------|------------|----|--|------------|---|---|--|-----------|---|
| 15 | 14 | 13 | 12 | 11 | | | 5 | 4 | | | 0 |
| NP | RES | RF | XNP | | | TAF | | | | SF | |
| rw | ro | rw | rw | | | rw | | | | rw | |

| Field | Bits | Type | Description |
|-------|------|------|--|
| NP | 15 | RW | <p>Next Page The next page indication is encoded in bit AN_ADV.NP regardless of the selector field value or link code word encoding. The PHY always advertises NP when a 1000BASE-T mode is advertised during auto-negotiation.</p> <p>0_B INACTIVE No next page to follow 1_B ACTIVE Additional next page(s) to follow</p> |
| RES | 14 | RO | <p>Reserved Write as zero, ignore on read.</p> |
| RF | 13 | RW | <p>Remote Fault This bit allows indication of a fault to the link partner.</p> <p>0_B NONE No remote fault is indicated. 1_B FAULT A remote fault is indicated.</p> |
| XNP | 12 | RW | <p>Extended Next Page Indicates the GPHY supports transmission of extended next pages (XNP).</p> <p>0_B UNABLE GPHY is XNP unable. 1_B ABLE GPHY is XNP able.</p> |
| TAF | 11:5 | RW | <p>Technology Ability Field This is an 8-bit wide field containing information indicating supported technologies. The GPHY supports half-duplex and full-duplex 10BASE-T and 100BASE-TX and also both symmetric and asymmetric PAUSE.</p> <p>40_H PS_ASYM Advertises asymmetric pause 20_H PS_SYM Advertises symmetric pause 10_H DBT4 Advertises 100BASE-T4 08_H DBT_FDX Advertises 100BASE-TX full-duplex 04_H DBT_HDX Advertises 100BASE-TX half-duplex 02_H XBT_FDX Advertises 10BASE-T full-duplex 01_H XBT_HDX Advertises 10BASE-T half-duplex</p> |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|---|
| SF | 4:0 | RW | <p>Selector Field</p> <p>This field is a 5-bit wide field for encoding 32 possible messages. The encodings are defined in IEEE 802.3-2008 Annex 28A. Unspecified combinations are reserved for future use. Reserved combinations of this field are not to be transmitted.</p> <p>00001_B IEEE802DOT3 Selects the IEEE 802.3 technology.</p> |

Auto-Negotiation Link Partner Ability (Register 0.5)

IEEE Standard Register=0.5

When the auto-negotiation is complete, this register contains the advertised ability of the link partner. The bit definitions are a direct representation of the received link code word.

STD_AN_LPA
Auto-Negotiation Link Partner Ability (Register 0.5)
Reset Value
1DE0_H

| | | | | | | | | | | | | | | | | | | |
|-----------|------------|-----------|------------|----|--|--|--|--|--|---|---|--|--|--|--|--|--|-----------|
| 15 | 14 | 13 | 12 | 11 | | | | | | 5 | 4 | | | | | | | 0 |
| NP | ACK | RF | XNP | | | | | | | | | | | | | | | SF |
| ro | ro | ro | rw | | | | | | | | | | | | | | | ro |

| Field | Bits | Type | Description |
|-------|------|------|--|
| NP | 15 | RO | Next Page Next page request indication from the link partner. 0 _B INACTIVE No next page to follow 1 _B ACTIVE Additional next pages to follow |
| ACK | 14 | RO | Acknowledge Acknowledgment indication from the link partner's link code word. 0 _B INACTIVE The device did not receive its link partner's link code word. 1 _B ACTIVE The device received its link partner's link code word. |
| RF | 13 | RO | Remote Fault Remote fault indication from the link partner. 0 _B NONE Remote fault is not indicated by the link partner. 1 _B FAULT Remote fault is indicated by the link partner. |
| XNP | 12 | RW | Extended Next Page Indicates the GPHY supports transmission of extended next pages (XNP). 0 _B UNABLE Link partner is XNP unable. 1 _B ABLE Link partner is XNP able. |
| TAF | 11:5 | RW | Technology Ability Field 40 _H PS_ASYM Advertises asymmetric pause 20 _H PS_SYM Advertises symmetric pause 10 _H DBT4 Advertises 100BASE-T4 08 _H DBT_FDX Advertises 100BASE-TX full-duplex 04 _H DBT_HDX Advertises 100BASE-TX half-duplex 02 _H XBT_FDX Advertises 10BASE-T full-duplex 01 _H XBT_HDX Advertises 10BASE-T half-duplex |
| SF | 4:0 | RO | Selector Field 00001 _B IEEE802DOT3 Selects the IEEE 802.3 technology |

Auto-Negotiation Expansion (Register 0.6)

This is the auto-negotiation expansion register indicating the status of the link partner's auto-negotiation. This register is valid only after the auto-negotiation is completed.

Refer to IEEE 802.3 28.2.4.1.5.

IEEE Standard Register=0.6

STD_AN_EXP

Auto-Negotiation Expansion (Register 0.6)

Reset Value

0064_H

| | | | | | | | | |
|------------|---|-------------------|-------------------|------------|-------------------|------------|-----------|-------------------|
| 15 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RES | | RNPL A | RNPS L | PDF | LPNP C | NPC | PR | LPAN C |
| ro | | ro | ro | rolh | ro | ro | rolh | ro |

| Field | Bits | Type | Description |
|--------|------|------|--|
| RES | 15:7 | RO | Reserved Write as zero, ignore on read. |
| RNPLA | 6 | RO | Receive Next Page Location Able According to 802.3-2015, indicates the Rx NP location is indicated by field RNPSL. 0 _B UNABLE Received Next Page Storage Location is not specified by bit (6.5). 1 _B ABLE Received Next Page Storage Location is specified by bit (6.5). |
| RNPSL | 5 | RO | Receive Next Page Storage Location According to 802.3-2015, indicates the Rx NP is in register 0.8 for the GPHY. 0 _B FIVE Link partner next pages are stored in register 5. 1 _B EIGHT Link partner next pages are stored in register 8. |
| PDF | 4 | ROLH | Parallel Detection Fault 0 _B NONE A fault was not detected via the parallel detection function. 1 _B FAULT A fault was detected via the parallel detection function. |
| LPNPC | 3 | RO | Link Partner Next Page Capable 0 _B UNABLE Link partner is unable to exchange next pages. 1 _B CAPABLE Link partner is capable of exchanging next pages. |
| NPC | 2 | RO | Next Page Capable 0 _B UNABLE GPHY is unable to exchange next pages. 1 _B CAPABLE GPHY is capable of exchanging next pages. |
| PR | 1 | ROLH | Page Received 0 _B NONE A new page was not received. 1 _B RECEIVED A new page was received. |
| LPANPC | 0 | RO | Link Partner Auto-Negotiation Capable 0 _B UNABLE Link partner is unable to auto-negotiate. 1 _B CAPABLE Link partner is auto-negotiation capable. |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|--|
| MCF | 10:0 | RW | <p>Message or Unformatted Code Field</p> <p>When the Message Page bit is set to 1_B (0.7.13), this field is the Message Code Field of a message page used in next page exchange. The message codes are described in IEEE 802.3 Appendix 28C. It is used to indicate the type of message in UCF1 and UCF2.</p> <p>00_H Reserved 01_H Null message 02_H One Unformatted Page (UP) with TAF follows 03_H Two UPs with TAF follows 04_H Remote fault details message 05_H OUI message 06_H PHY ID message 07_H 100BASE-T2 message 08_H 1000BASE-T message 09_H MULTIGBASE-T message 0A_H EEE technology capability follows in next UP 0B_H OUI XNP</p> |

Auto-Negotiation Link Partner Received Next Page Register (Register 0.8)

This register contains the next page link code word received from the link partner. Refer to IEEE 802.3-2008 28.2.4.1.7.

IEEE Standard Register=0.8

STD_AN_NPRX

Reset Value

Auto-Negotiation Link Partner Received Next Page Register (Register 0.8)

0000_H

| | | | | | | | | | | | | | | | | |
|-----------|------------|-----------|-------------|-------------|------------|--|--|--|--|--|--|--|--|--|--|---|
| 15 | 14 | 13 | 12 | 11 | 10 | | | | | | | | | | | 0 |
| NP | ACK | MP | ACK2 | TOGG | MCF | | | | | | | | | | | |
| ro | ro | ro | ro | ro | rw | | | | | | | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|--|
| NP | 15 | RO | Next Page 0 _B INACTIVE No next pages to follow 1 _B ACTIVE Additional next page(s) to follow |
| ACK | 14 | RO | Acknowledge 0 _B INACTIVE The device did not receive its link partner's link code word. 1 _B ACTIVE The device received its link partner's link code word. |
| MP | 13 | RO | Message Page Indicates the content of MCF is either an unformatted page or a formatted message. 0 _B UNFOR Unformatted page 1 _B MESSG Message page |
| ACK2 | 12 | RO | Acknowledge 2 0 _B INACTIVE Device is not able to comply with the message. 1 _B ACTIVE Device complies with the message. |
| TOGG | 11 | RO | Toggle This bit always takes the opposite value of the Toggle bit in the previously exchanged link code word. 0 _B ZERO Previous value of the transmitted link code word was 1 _B . 1 _B ONE Previous value of the transmitted link code word was 0 _B . |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|---|
| MCF | 10:0 | RW | <p>Message or Unformatted Code Field</p> <p>This field is the Message Code Field of a message page used in next page exchange.</p> <p>The message codes are described in IEEE 802.3 Appendix 28C. It is used to indicate the type of message in UCF1 and UCF2.</p> <p>00_H Reserved 01_H Null message 02_H One Unformatted Page (UP) with TAF follows 03_H Two UPs with TAF follows 04_H Remote fault details message 05_H OUI message 06_H PHY ID message 07_H 100BASE-T2 message 08_H 1000BASE-T message 09_H MULTIGBASE-T message 0A_H EEE technology capability follows in next UP 0B_H OUI XNP</p> |

Gigabit Control Register (Register 0.9)

This is the control register to configure the Gigabit Ethernet behavior of the PHY. Refer to IEEE 802.3-2008 40.5.1.1.

IEEE Standard Register=0.9

STD_GCTRL

Gigabit Control Register (Register 0.9)

Reset Value

0200_H

| | | | | | | | | | | | |
|----|----|------|----|------|-----------|-----------|-----|--|--|--|---|
| 15 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | | | | 0 |
| TM | | MSEN | MS | MSPT | MBTF D | MBTH D | RES | | | | |
| rw | | rw | rw | rw | rw | rw | ro | | | | |

| Field | Bits | Type | Description |
|-------|-------|------|--|
| TM | 15:13 | RW | Transmitter Test Mode This register field allows enabling of the standard transmitter test modes. 000 _B NOP Normal operation 001 _B WAV Test mode 1 transmit waveform test 010 _B JITM Test mode 2 transmit jitter test in master mode 011 _B JITS Test mode 3 transmit jitter test in slave mode 100 _B DIST Test mode 4 transmitter distortion test |
| MSEN | 12 | RW | Master/Slave Manual Configuration Enable 0 _B DISABLED Disables master/slave manual configuration value. 1 _B ENABLED Enables master/slave manual configuration value. |
| MS | 11 | RW | Master/Slave Configuration Value Allows forcing of master or slave mode manually when AN_GCTRL.MSEN is set to 1 _B . 0 _B SLAVE Configures PHY as slave during master/slave negotiation. 1 _B MASTER Configures PHY as master during master/slave negotiation. |
| MSPT | 10 | RW | Master/Slave Port Type Defines whether the PHY advertises itself as a multi- or single-port device, which in turn impacts the master/slave resolution function. 0 _B SPD Single-port device 1 _B MPD Multi-port device |
| MBTFD | 9 | RW | 1000BASE-T Full-Duplex Advertises the 1000BASE-T full-duplex capability; always forced to 1 in converter mode. 0 _B DISABLED Advertises PHY as not 1000BASE-T full-duplex capable 1 _B ENABLED Advertises PHY as 1000BASE-T full-duplex capable |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|---|
| MBTHD | 8 | RW | <p>1000BASE-T Half-Duplex Always advertises the 1000BASE-T half-duplex capability as disabled. The GPHY does not support 1000BASE-T half-duplex capability.</p> <p>0_B DISABLED Advertises PHY as not 1000BASE-T half-duplex capable</p> <p>1_B ENABLED Advertises PHY as 1000BASE-T half-duplex capable</p> |
| RES | 7:0 | RO | <p>Reserved Write as zero, ignore on read.</p> |

Gigabit Status Register (Register 0.10)

This is the status register used to reflect the Gigabit Ethernet status of the PHY. Refer to IEEE 802.3-2022 40.5.1.1.

IEEE Standard Register=0.10

STD_GSTAT
Gigabit Status Register (Register 0.10)
Reset Value
0000_H

| | | | | | | | | | | | | | | | | | | | |
|---------------------|-------------------|---------------------|---------------------|-------------------|-------------------|------------|---|---|------------|--|--|--|--|--|--|--|--|--|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | | | | | | | | | | | 0 |
| MSFA ULT | MSRE S | LRXS TAT | RRXS TAT | MBTF D | MBTH D | RES | | | IEC | | | | | | | | | | |
| rwsc | ro | ro | ro | ro | ro | ro | | | rwsc | | | | | | | | | | |

| Field | Bits | Type | Description |
|---------|------|------|--|
| MSFAULT | 15 | RWSC | Master/Slave Manual Configuration Fault This bit is set when the number of failed master-slave resolutions reaches 7. It is cleared upon each read of GSTAT. This bit self clears on auto-negotiation enable or auto-negotiation complete. 0 _B OK Master/slave manual configuration resolved successfully 1 _B NOK Master/slave manual configuration resolved with a fault |
| MSRES | 14 | RO | Master/Slave Configuration Resolution 0 _B SLAVE Local PHY configuration resolved to SLAVE 1 _B MASTER Local PHY configuration resolved to MASTER |
| LRXSTAT | 13 | RO | Local Receiver Status Indicates the status of the local receiver. 0 _B NOK Local receiver not OK 1 _B OK Local receiver OK |
| RRXSTAT | 12 | RO | Remote Receiver Status Indicates the status of the remote receiver. 0 _B NOK Remote receiver not OK 1 _B OK Remote receiver OK |
| MBTFD | 11 | RO | Link Partner Capable of Operating 1000BASE-T Full-Duplex 0 _B DISABLED Link partner is not capable of operating 1000BASE-T full-duplex 1 _B ENABLED Link partner is capable of operating 1000BASE-T full-duplex |
| MBTHD | 10 | RO | Link Partner Capable of Operating 1000BASE-T Half-Duplex 0 _B DISABLED Link partner is not capable of operating 1000BASE-T half-duplex 1 _B ENABLED Link partner is capable of operating 1000BASE-T half-duplex |
| RES | 9:8 | RO | Reserved Write as zero, ignore on read. |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|--|
| IEC | 7:0 | RWSC | Idle Error Count Indicates the idle error count. This field contains a cumulative count of the errors detected when the receiver receives idles. |

MMD Access Control Register (Register 0.13)

The MMD access control register is used in conjunction with the MMDDATA register to access the MMD register space. This uses address directing as specified in IEEE 802.3 Clause 22 Extended.

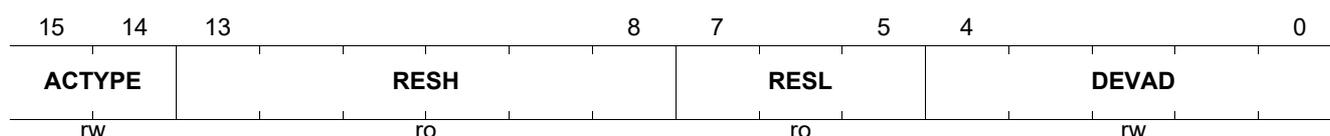
IEEE Standard Register=0.13

STD_MMDCTRL

Reset Value

MMD Access Control Register (Register 0.13)

0000_H

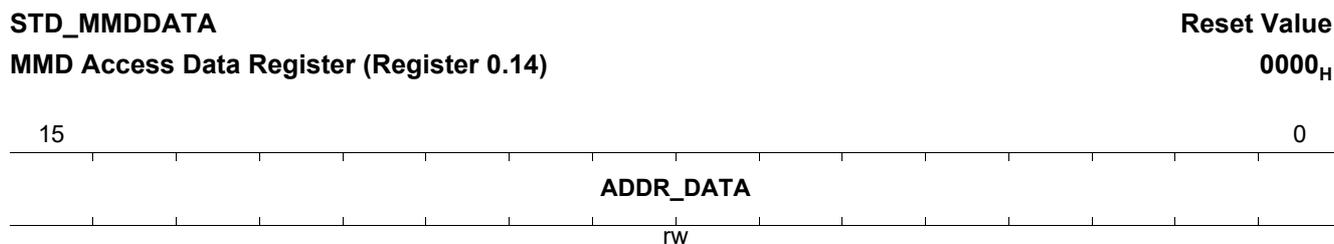


| Field | Bits | Type | Description |
|--------|-------|------|---|
| ACTYPE | 15:14 | RW | Access Type Function When the MMDDATA register is accessed via an address access (ACTYPE=0), the access is directed to the address register within the MMD associated with the value in the DEVAD field. Otherwise, both the DEVAD field and the MMD address register direct the MMDDATA register data accesses to the appropriate registers within that MMD. 00 _B ADDRESS Accesses to the MMDDATA register access the MMD individual address register. 01 _B DATA Accesses to the MMDDATA register access the register within the MMD selected. 10 _B DATA_PI Accesses to the MMDDATA register access the register within the MMD selected. 11 _B DATA_PIWR Accesses to the MMDDATA register access the register within the MMD selected. |
| RESH | 13:8 | RO | Reserved Write as zero, ignored on read. |
| RESL | 7:5 | RO | Reserved Write as zero, ignored on read. |
| DEVAD | 4:0 | RW | Device Address The DEVAD field directs any accesses of register MMDDATA to the appropriate MMD as described in IEEE 802.3-2008 Clause 45.2. |

MMD Access Data Register (Register 0.14)

The MMD access data register is used in conjunction with the MMD access control (MMDCTRL) register to access the MMD register space. For more information on MMD access, refer to IEEE 802.3-2008 Clause 22.2.4.3.12, Clause 45.2, and Annex 22D.

IEEE Standard Register=0.14



| Field | Bits | Type | Description |
|-----------|------|------|---|
| ADDR_DATA | 15:0 | RW | Address or Data Register This register accesses either a specific MMD address register or the data content of the MMD register to which this address register points. The MMDCTRL register defines which function is currently valid. |

Extended Status Register (Register 0.15)

This register contains extended status and capability information about the PHY. All the bits are read-only. A write access does not have any effect.

IEEE Standard Register=0.15

STD_XSTAT

Reset Value

Extended Status Register (Register 0.15)

2000_H

| | | | | | | | |
|-------------|-------------|-------------|-------------|----|-------------|---|-------------|
| 15 | 14 | 13 | 12 | 11 | 8 | 7 | 0 |
| MBXF | MBXH | MBTF | MBTH | | RESH | | RESL |
| ro | ro | ro | ro | | ro | | ro |

| Field | Bits | Type | Description |
|-------|------|------|--|
| MBXF | 15 | RO | 1000BASE-X Full-Duplex Capability Specifies whether the PHY is capable of operating 1000BASE-X full-duplex. 0 _B DISABLED PHY does not support this mode. 1 _B ENABLED PHY supports this mode. |
| MBXH | 14 | RO | 1000BASE-X Half-Duplex Capability Specifies whether the PHY is capable of operating 1000BASE-X half-duplex. 0 _B DISABLED PHY does not support this mode. 1 _B ENABLED PHY supports this mode. |
| MBTF | 13 | RO | 1000BASE-T Full-Duplex Capability Specifies whether the PHY is capable of operating 1000BASE-T full-duplex. 0 _B DISABLED PHY does not support this mode. 1 _B ENABLED PHY supports this mode. |
| MBTH | 12 | RO | 1000BASE-T Half-Duplex Capability GPHY do not support 1000BASE-T half-duplex capability. 0 _B DISABLED PHY does not support this mode. 1 _B ENABLED PHY supports this mode. |
| RESH | 11:8 | RO | Reserved Ignore when read. |
| RESL | 7:0 | RO | Reserved Ignore when read. |

5.2 PHY-specific Management Registers

This section describes the PHY-specific management registers in device 0.

Table 28 Registers Overview- PHY-specific Management Registers

| Register Short Name | Register Long Name | Reset Value |
|-----------------------------|--|-------------------|
| PHY_STAT1 | Physical Layer Status 1 (Register 0.17) | 000C _H |
| PHY_CTL1 | Physical Layer Control 1 (Register 0.19) | 0001 _H |
| PHY_CTL2 | Physical Layer Control 2 (Register 0.20) | 0006 _H |
| PHY_ERRCNT | Error Counter (Register 0.21) | 0000 _H |
| PHY_MIISTAT | Media-Independent Interface Status (Register 0.24) | 0000 _H |
| PHY_IMASK | Interrupt Mask Register (Register 0.25) | 0000 _H |
| PHY_ISTAT | Interrupt Status Register (Register 0.26) | 0000 _H |
| PHY_LED | LED Control Register (Register 0.27) | FF00 _H |
| PHY_TPGCTRL | Test-Packet Generator Control (Register 0.28) | 0000 _H |
| PHY_TPGDATA | Test-Packet Generator Data (Register 0.29) | 00AA _H |
| PHY_FWV | Firmware Version Register (Register 0.30) | 0000 _H |

5.2.1 PHY-specific Management Register Descriptions

This section describes all the PHY registers in detail.

Physical Layer Status 1 (Register 0.17)

This register reports PHY link information, for example link-up, polarity reversals, and port mapping. The content of this register is only valid when the link is up.

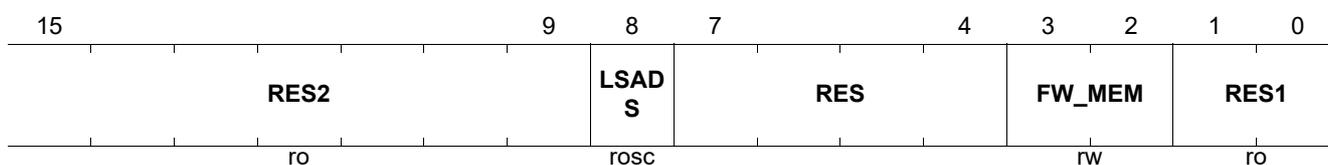
IEEE Standard Register=0.17

PHY_STAT1

Physical Layer Status 1 (Register 0.17)

Reset Value

000C_H



| Field | Bits | Type | Description |
|--------|------|------|--|
| RES2 | 15:9 | RO | Reserved Write as zero, ignored on read. |
| LSADS | 8 | ROSC | Link Speed Auto-Downspeed Status Monitors the status of the Auto-Downspeed (ADS). 0 _B NORMAL Did not perform any link speed ADS. 1 _B DETECTED Detected an ADS. |
| FW_MEM | 3:2 | RW | Firmware Memory Location Indicates memory target used for firmware execution. 11 _B RAM Firmware is executed from SRAM. Others: Reserved. |
| RES1 | 1:0 | RO | Reserved Write as zero, ignored on read. |

Physical Layer Control 1 (Register 0.19)

This register controls the PHY functions.

IEEE Standard Register=0.19

PHY_CTL1
Physical Layer Control 1 (Register 0.19)
Reset Value
0001_H

| | | | | | | | | | | | | | |
|-------|----|-------|-------|---|---|------|------|------|------|-----------|-----------|-----|-------|
| 15 | 13 | 12 | 11 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| TLOOP | | TXOFF | TXADJ | | | POLD | POLC | POLB | POLA | MDIC D | MDIA B | RES | AMDIX |
| rw | | rw | rw | | | rw | rw | rw | rw | rw | rw | ro | rw |

| Field | Bits | Type | Description |
|-------|-------|------|---|
| TLOOP | 15:13 | RW | Test Loop Configures predefined test loops. 000 _B OFF Test loops are switched off - normal operation. 001 _B NETL Near-end test loop 010 _B FETL Far-end test loop. 100 _B RJTL RJ45 connector test loop. 101 _B FETL S Standalone far-end test loop. No dependency on GMII_TX_CLK and GMII_RX_CLK. Others: Reserved. |
| TXOFF | 12 | RW | Transmitter Off This register bit turns the transmitter off. This feature is used for return loss measurements. 0 _B ON Transmitter is on. 1 _B OFF Transmitter is off. |
| TXADJ | 11:8 | RW | Transmit Level Adjustment Reserved. |
| POLD | 7 | RW | Polarity Inversion Control on Port D 0 _B NORMAL Polarity normal 1 _B INVERTED Polarity inversion |
| POLC | 6 | RW | Polarity Inversion Control on Port C 0 _B NORMAL Polarity normal 1 _B INVERTED Polarity inversion |
| POLB | 5 | RW | Polarity Inversion Control on Port B 0 _B NORMAL Polarity normal 1 _B INVERTED Polarity inversion |
| POLA | 4 | RW | Polarity Inversion Control on Port A 0 _B NORMAL Polarity normal 1 _B INVERTED Polarity inversion |
| MDICD | 3 | RW | Mapping of MDI Ports C and D Used when Auto-MDIX is OFF to force the MDIX cable crossover configuration. 0 _B MDI Normal MDI mode 1 _B MDIX Crossover MDI-X mode |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|--|
| MDIAB | 2 | RW | Mapping of MDI Ports A and B Used when Auto-MDIX is OFF to force the MDIX cable crossover configuration. 0 _B MDI Normal MDI mode 1 _B MDIX Crossover MDI-X mode |
| RES | 1 | RO | Reserved |
| AMDIX | 0 | RW | PHY Performs Auto-MDI/MDI-X or Uses Manual MDI/MDI-X 0 _B MANUAL PHY uses manual MDI/MDI-X. 1 _B AUTO PHY performs Auto-MDI/MDI-X. |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|--|
| ANPD | 1 | RW | <p>Auto-Negotiation Power Down Allows enabling/disabling of the power down modes during auto-negotiation looking for a link partner.</p> <p>0_B OFF ANPD is disabled. 1_B ON ANPD is enabled.</p> |
| LPI | 0 | RW | <p>Assert LPI via MDIO Controls assertion/de-assertion of the LPI by the MDIO instead of following the (X)GMII LPI. Used to force the EEE on the TPI (ignoring the LPI indication from MAC).</p> <p>0_B DE-ASSERT LPI is de-asserted on TPI. 1_B ASSERT LPI is asserted on TPI.</p> |

Error Counter (Register 0.21)

This register controls the error counter. It allows the number of errors detected in the PHY to be counted for monitoring purposes.

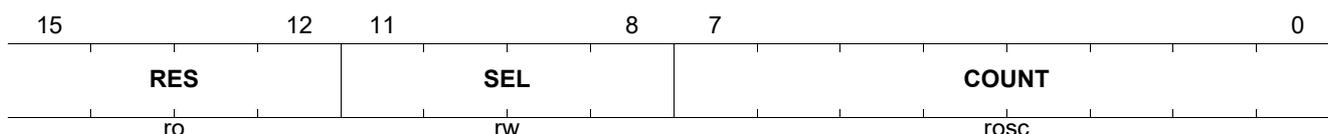
IEEE Standard Register=0.21

PHY_ERRCNT

Error Counter (Register 0.21)

Reset Value

0000_H



| Field | Bits | Type | Description |
|-------|-------|------|---|
| RES | 15:12 | RO | Reserved Write as zero, ignored on read. |
| SEL | 11:8 | RW | Select Error Event Configures which error type the error counter counts: 0000 _B RXERR Receive errors are counted. 0001 _B RXACT Receive frames are counted. 0010 _B ESDERR ESD errors are counted. 0011 _B SSDERR SSD errors are counted. 0100 _B TXERR Transmit errors are counted. 0101 _B TXACT Transmit frames events are counted. 0110 _B COL Collision events are counted. 1000 _B NLD Number of Link Down events are counted. 1001 _B NDS Number of ADS events are counted. 1010 _B RES Reserved 1011 _B RES Reserved |
| COUNT | 7:0 | ROSC | Counter Value This counter value is updated each time the selected error event is detected. The counter value is reset every time a read operation on this register is performed or the error event is changed. The counter saturates at value FF _H . |

Interrupt Mask Register (Register 0.25)

This register defines the mask for the Interrupt Status Register (ISTAT), which contains the event source for the MDINT interrupt sent from the GPHY to an external chip.

The information about the interrupt source is indicated in the ISTAT register.

IEEE Standard Register=0.25

PHY_IMASK

Reset Value

Interrupt Mask Register (Register 0.25)

0000_H

| | | | | | | | | | | | | | | | |
|-----|------|------|------|-----|-----|-----|-----|----|------|------|-------|-------|------|------|------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| WOL | MSRE | NPRX | NPTX | ANE | ANC | RES | LOR | LP | TEMP | ADSC | MDIPC | MDIXC | DXMC | LSPC | LSTC |
| RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

| Field | Bits | Type | Description |
|-------|------|------|--|
| WOL | 15 | RW | Wake-on-LAN Event Mask When active and masked in IMASK, the MDINT is activated upon detection of a valid WoL event. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |
| MSRE | 14 | RW | Master/Slave Resolution Error Mask When active, MDINT is activated upon detection of a master/slave resolution error (MSRE) during a 1000BASE-T ANEG. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |
| NPRX | 13 | RW | Next Page Received Mask When active, MDINT is activated upon reception of a next page in STD_AN_NPRX. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |
| NPTX | 12 | RW | Next Page Transmitted Mask When active, MDINT is activated upon transmission of the currently stored next page in STD_AN_NPTX. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |
| ANE | 11 | RW | Auto-Negotiation Error Mask When active, MDINT is activated upon detection of an ANEG error. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |
| ANC | 10 | RW | Auto-Negotiation Complete Mask When active, MDINT is activated upon completion of the ANEG process. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|---|
| LOR | 8 | RW | SyncE Loss Of Reference When active, MDINT is activated upon loss of SyncE reference clock. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |
| LP | 7 | RW | LP Entry Indication Mask 0 _B INACTIVE Interrupt is masked out. The STA does not need to be informed of the event. 1 _B ACTIVE Interrupt is activated. The STA receives MDINT when the PHY is about to enter LP. |
| TEMP | 6 | RW | TEMP 0 _B INACTIVE Interrupt is masked out. The STA does not need to be informed of the event. 1 _B ACTIVE Interrupt is activated. The interrupt is triggered when the temperature goes beyond the normal operating range. |
| ADSC | 5 | RW | Link Speed Auto-Downspeed Detect Mask When active, MDINT is activated upon detection of a link speed ADS event. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |
| MDIPC | 4 | RW | MDI Polarity Change Detect Mask When active, MDINT is activated upon detection of an MDI polarity change event. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |
| MDIXC | 3 | RW | MDIX Change Detect Mask When active, MDINT is activated upon detection of an MDI/MDIX cross-over change event. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |
| DXMC | 2 | RW | Duplex Mode Change Mask When active, MDINT is activated upon detection of full or half-duplex change. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |
| LSPC | 1 | RW | Link Speed Change Mask When active, MDINT is activated upon detection of link speed change. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |
| LSTC | 0 | RW | Link State Change Mask When active, MDINT is activated upon detection of link status change. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |

Interrupt Status Register (Register 0.26)

This register defines the event source for the MDINT interrupt sent from the GPHY to an external chip.

PHY_ISTAT is a cleared on read by the STA.

IEEE Standard Register=0.26

PHY_ISTAT
Reset Value
Interrupt Status Register (Register 0.26)
0000_H

| | | | | | | | | | | | | | | | |
|------------|-------------|-------------|-------------|------------|------------|------------|------------|-----------|-------------|-------------|--------------|--------------|-------------|-------------|-------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| WOL | MSRE | NPRX | NPTX | ANE | ANC | RES | LOR | LP | TEMP | ADSC | MDIPC | MDIXC | DXMC | LSPC | LSTC |
| rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc |

| Field | Bits | Type | Description |
|-------|------|------|--|
| WOL | 15 | ROSC | Wake-on-LAN Interrupt Status When this bit is set, the MDINT is activated upon detection of a valid WoL event. 0 _B INACTIVE This event is not the interrupt source. 1 _B ACTIVE The WoL event is the source of the interrupt. |
| MSRE | 14 | ROSC | Master/Slave Resolution Error Interrupt Status When this bit is set, the MDINT is activated upon detection of a MSRE during a 1000BASE-T ANEG. 0 _B INACTIVE This event is not the interrupt source. 1 _B ACTIVE The MSRE event is the source of the interrupt. |
| NPRX | 13 | ROSC | Next Page Received Interrupt Status When this bit is set, the MDINT is activated upon reception of a next page in STD_AN_NPRX. 0 _B INACTIVE This event is not the interrupt source. 1 _B ACTIVE The NPRX event is the source of the interrupt. |
| NPTX | 12 | ROSC | Next Page Transmitted Interrupt Status When this bit is set, the MDINT is activated upon transmission of the currently stored next page in STD_AN_NPTX. 0 _B INACTIVE This event is not the interrupt source. 1 _B ACTIVE The NPTX event is the source of the interrupt. |
| ANE | 11 | ROSC | Auto-Negotiation Error Interrupt Status When this bit is set, the MDINT is activated upon detection of an ANEG error. 0 _B INACTIVE This event is not the interrupt source. 1 _B ACTIVE The ANEG error event is the source of the interrupt. |
| ANC | 10 | ROSC | Auto-Negotiation Complete Interrupt Status When this bit is set, the MDINT is activated upon completion of the ANEG process. 0 _B INACTIVE This event is not the interrupt source. 1 _B ACTIVE The ANEG complete event is the source of the interrupt. |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|---|
| LOR | 8 | ROSC | SyncE Loss Of Reference When this bit is set, MDINT is activated upon loss of SyncE reference clock. 0 _B INACTIVE This event is not the interrupt source. 1 _B ACTIVE The LOR change event is the source of the interrupt. |
| LP | 7 | ROSC | LP Entry Indication 0 _B INACTIVE No indication of LP entry 1 _B ACTIVE Indication of LP entry. |
| TEMP | 6 | ROSC | TEMP Indicates that thermal mitigation action must be taken when the temperature goes beyond the normal operating range. The GPHY implements ADS by default when this happens, but it is possible to disable ADS. When the SoC disables ADS, it is recommended that the SoC initiates a link down and changes the speed capability to cool the device back to the normal temperature range. When the temperature reaches the maximum absolute rating, the device resets for safety purposes. Thermal mitigation must ensure that the maximum absolute temperature limits are never reached. 0 _B INACTIVE This event is not the interrupt source. 1 _B ACTIVE The TEMP change event is the source of the interrupt. |
| ADSC | 5 | ROSC | Link Speed Auto-Downspeed Detect Interrupt Status When this bit is set, the MDINT is activated upon detection of a link speed ADS event. 0 _B INACTIVE This event is not the interrupt source. 1 _B ACTIVE The ADSC change event is the source of the interrupt. |
| MDIPC | 4 | ROSC | MDI Polarity Change Detect Interrupt Status When this bit is set, the MDINT is activated upon detection of an MDI polarity change event. 0 _B INACTIVE This event is not the interrupt source. 1 _B ACTIVE The MDIPC change event is the source of the interrupt. |
| MDIXC | 3 | ROSC | MDIX Change Detect Interrupt Status When this bit is set, the MDINT is activated upon detection of an MDI/MDIX cross-over change event. 0 _B INACTIVE This event is not the interrupt source. 1 _B ACTIVE The MDIX change event is the source of the interrupt. |
| DXMC | 2 | ROSC | Duplex Mode Change Interrupt Status When this bit is set, the MDINT is activated upon detection of a full or half-duplex change. 0 _B INACTIVE This event is not the interrupt source. 1 _B ACTIVE The DXMC change event is the source of the interrupt. |
| LSPC | 1 | ROSC | Link Speed Change Interrupt Status When this bit is set, the MDINT is activated upon detection of link speed change. 0 _B INACTIVE This event is not the interrupt source. 1 _B ACTIVE The LSPC change event is the source of the interrupt. |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|--|
| LSTC | 0 | ROSC | <p>Link State Change Interrupt Status When this bit is set, the MDINT is activated upon detection of link status change.</p> <p>0_B INACTIVE This event is not the interrupt source. 1_B ACTIVE The LSTC change event is the source of the interrupt.</p> |

LED Control Register (Register 0.27)

This register contains the control bits for direct access to the LEDs by setting the on/off LEDxDA bits (where x is from 0 to 1).

To directly control the LED, the integrated LED functions must be disabled by the LEDxEN bit in this register.

The integrated LED functions are specified in the more sophisticated LED control registers in the MMD device VSPEC1.

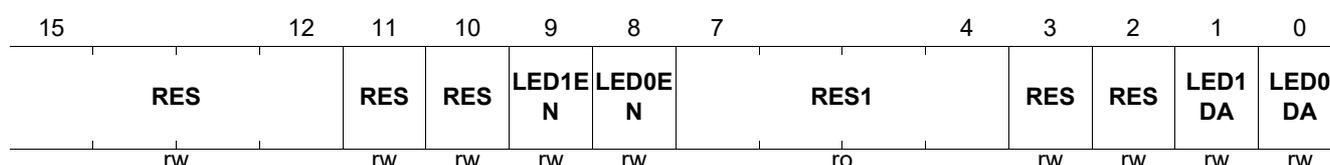
IEEE Standard Register=0.27

PHY_LED

LED Control Register (Register 0.27)

Reset Value

FF00_H



| Field | Bits | Type | Description |
|--------|-------|------|---|
| RES | 15:12 | RW | Reserved The default value must not be changed. |
| LED1EN | 9 | RW | Enable Integrated Function of LED1 Write a 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED1DA. 0 _B DISABLE Disables the integrated LED function. 1 _B ENABLE Enables the integrated LED function. |
| LED0EN | 8 | RW | Enable Integrated Function of LED0 Write a 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED0DA. 0 _B DISABLE Disables the integrated LED function. 1 _B ENABLE Enables the integrated LED function. |
| RES1 | 7:4 | RO | Reserved Write as zero, ignored on read. |
| LED1DA | 1 | RW | Direct Access to LED1 Write a 1 to this bit to illuminate the LED. LED1EN must be set to zero. 0 _B OFF Switch off the LED. 1 _B ON Switch on the LED. |
| LED0DA | 0 | RW | Direct Access to LED0 Write a 1 to this bit to illuminate the LED. LED0EN must be set to zero. 0 _B OFF Switch off the LED. 1 _B ON Switch on the LED. |

Test-Packet Generator Control (Register 0.28)

This register controls the operation of the integrated Test-Packet Generator (TPG). This module is only used for testing purposes.

IEEE Standard Register=0.28

PHY_TPGCTRL
Reset Value
Test-Packet Generator Control (Register 0.28)
0000_H

| | | | | | | | | | | | | | | |
|------------|----|-------------|-------------|-------------|----|-------------|---|-------------|-------------|---|-------------|---|-------------------|-----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 4 | 3 | 2 | 1 | 0 |
| RES | | MODE | RES3 | IPGL | | TYPE | | RES2 | SIZE | | RES1 | | STAR T | EN |
| rw | | rw | ro | rw | | rw | | ro | rw | | ro | | rw | rw |

| Field | Bits | Type | Description |
|-------|-------|------|--|
| RES | 15:14 | RW | Reserved Write as zero, ignore on read. |
| MODE | 13 | RW | TPG Mode Configures the packet generation mode. 0 _B CONTINUOUS Sends packets continuously. 1 _B SINGLE Sends a single packet. |
| RES3 | 12 | RO | Reserved Write as zero, ignore on read. |
| IPGL | 11:10 | RW | Inter-Packet Gap Length Configures the length of the inter-packet gap in bit times. 00 _B RES Reserved 01 _B BT96 Length is 96 bit times 10 _B BT960 Length is 960 bit times 11 _B BT9600 Length is 9600 bit times |
| TYPE | 9:8 | RW | Packet Data Type Configures the packet data type to be either predefined, byte increment, or random. When predefined, the content of the register TPGDATA is used. 00 _B RANDOM Uses random data as the packet content. 01 _B BYTEINC Uses byte increment as the packet content. 10 _B PREDEF Uses predefined content of the register TPGDATA. 11 _B RES Reserved. |
| RES2 | 7 | RO | Reserved. Write as zero, ignore on read. |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|--|
| SIZE | 6:4 | RW | <p>Packet Size Configures the size of the generated Ethernet packets in bytes. The size includes DA, SA, length/type, payload, and FCS.</p> <p>000_B B64 Packet length is 64 bytes 001_B B2048 Packet length is 2048 bytes 010_B B256 Packet length is 256 bytes 011_B B4096 Packet length is 4096 bytes 100_B B1024 Packet length is 1024 bytes 101_B B1518 Packet length is 1518 bytes 110_B B9000 Packet length is 9000 bytes</p> |
| RES1 | 3:2 | RO | <p>Reserved Write as zero, ignore on read.</p> |
| START | 1 | RW | <p>Start or Stop TPG Data Generation. Starts the TPG data generation. Depending on the MODE, the TPG sends only one packet or chunks of 10000 packets until stopped.</p> <p>0_B STOP Stops the TPG data generation. 1_B START Starts the TPG data generation.</p> |
| EN | 0 | RW | <p>Enable the TPG Enables the TPG for data generation.</p> <p>0_B DISABLE Disables the TPG 1_B ENABLE Enables the TPG</p> |

Test-Packet Generator Data (Register 0.29)

Specifies the payload data to be used when sending a non-random data packet. All payload data bytes are sent with this value.

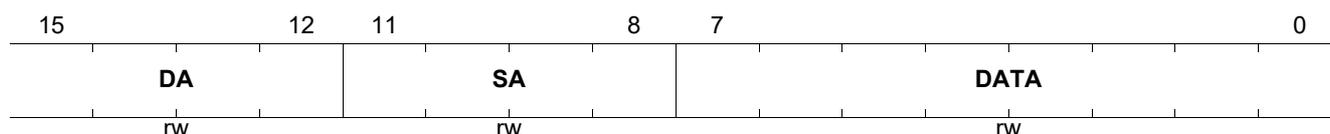
IEEE Standard Register=0.29

PHY_TPGDATA

Reset Value

Test-Packet Generator Data (Register 0.29)

00AA_H



| Field | Bits | Type | Description |
|-------|-------|------|--|
| DA | 15:12 | RW | Destination Address Configures the destination address nibble. The destination address builds up to 00-03-19-FF-FF-F[DA]. |
| SA | 11:8 | RW | Source Address Configures the source address nibble. The source address builds up to 00-03-19-FF-FF-F[SA]. |
| DATA | 7:0 | RW | Data Byte to be Transmitted This is the content of the payload bytes in the frame to send constant data. The bit masks are shown here. For configuration details, refer to the corresponding chapter. 80 _H PREC Selects whether to take full precision (1) or reduced precision (0) at bit 7 60 _H PREC2 For reduced precision, selects the options with bits [6:5] 10 _H RESERVED Reserved |

Firmware Version Register (Register 0.30)

This register contains the version of the PHY firmware. The firmware initializes the version number at boot time with its current software version. This register is read-only by the external STA.

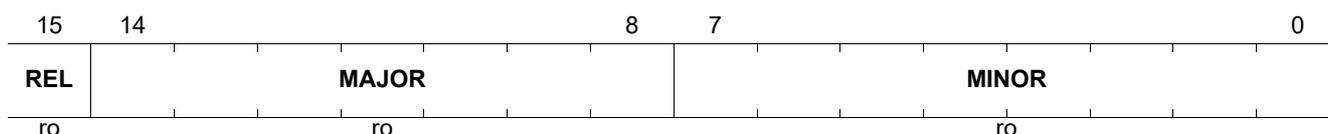
IEEE Standard Register=0.30

PHY_FWV

Firmware Version Register (Register 0.30)

Reset Value

0000_H



| Field | Bits | Type | Description |
|-------|------|------|--|
| REL | 15 | RO | Release Indication This parameter indicates either a test or a release version. 0 _B TEST Indicates a test version. 1 _B RELEASE Indicates a released version. |
| MAJOR | 14:8 | RO | Major Version Number Specifies the main version release number of the firmware. |
| MINOR | 7:0 | RO | Minor Version Number Specifies the sub-version release number of the firmware. |

Internal Test Modes CDIAG and ABIST (Register 0.31)

This is the control register used to configure the Gigabit Ethernet behavior of the PHY. Refer to IEEE 802.3 40.5.1.1.

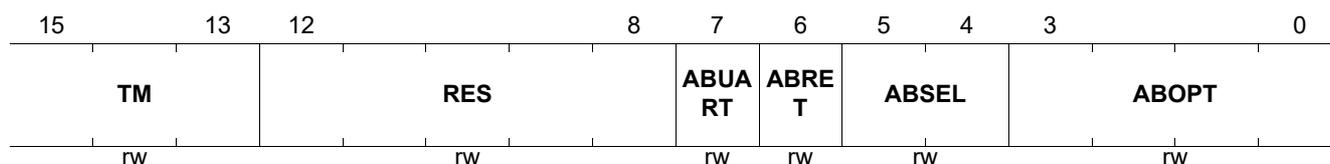
IEEE Standard Register=0.31

PHY_TEST

Reset Value

Internal Test Modes CDIAG and ABIST (Register 0.31)

0000_H



| Field | Bits | Type | Description |
|--------|-------|------|--|
| TM | 15:13 | RW | Proprietary Test Modes ABIST and CDIAG Enters the test mode. Any value different from 6 or 7 has no effect. 110 _B CDIAG GPHY-specific cable diagnostic 111 _B ABIST GPHY-specific analog built-in self-test |
| RES | 12:8 | RW | Reserved |
| ABUART | 7 | RW | ABIST UART Output for Debug When this bit is set to 1 _B , it enables a detail report on the debug UART output. This is used to debug the feature and not for production mode, because in that case the two LED signals are not used to indicate completion or pass fail. An alternative to the UART output is to read the STB via MDIO commands. 0 _B NORMAL ABIST normal output 1 _B UART ABIST output to UART |
| ABRET | 6 | RW | ABIST ReTrig When this bis is set to 1 _B , it enables a restart of the selected ABIST test. This is used to debug the feature and not for production mode. 0 _B NORMAL Normal mode 1 _B RETRIG Restarts the current ABIST test. |
| ABSEL | 5:4 | RW | ABIST Sub-mode Selection 00 _B ANALOG ABIST analog tests 01 _B DC ABIST DC tests 01 _B RES Reserved 11 _B RES Reserved |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|---|
| ABOPT | 3:0 | RW | ABIST Option for DC test 0000 _B ABIST DC test for 10BASE-T mode LD, maximum positive differential level 0001 _B ABIST DC test for 1000BASE-T mode LD, maximum positive differential level 0010 _B ABIST DC test for 10BASE-T mode LD, 0 differential level 0011 _B ABIST DC test for 1000BASE-T mode LD, 0 differential level 0100 _B ABIST DC test for 10BASE-T mode LD, maximum negative differential level 0101 _B ABIST DC test for 1000BASE-T mode LD, maximum negative differential level 0110 _B ABIST DC test for 2.5GBASE-T mode LD, maximum positive differential level 0111 _B ABIST DC test for 2.5GBASE-T mode LD, 0 differential level 1000 _B ABIST DC test for 2.5GBASE-T mode LD, maximum negative differential level |

6 MMD Registers Detailed Description

Table 29 Register Access Type

| Mode | Symbol |
|---|--------|
| Status Register (Status or Ability Register) | RO |
| Read-Write Register (MDIO Register) | RW |
| Read-Write Self-Clearing Register (bit is cleared after read from MDIO) | RWSC |
| Read-Only Self-Clearing Register (bit is cleared after read from MDIO) | ROSC |

6.1 Standard PMAPMD Registers for MMD=0x01

Table 30 Registers Overview- Standard PMAPMD Registers

| Register Short Name | Register Long Name | Reset Value |
|---|--|---------------------------------|
| PMA_CTRL1 | PMA/PMD Control 1 (Register 1.0) | 2058 _H |
| PMA_STAT1 | PMA/PMD Status 1 (Register 1.1) | 0000 _H |
| PMA_DEVID1 | PHY Identifier 1 (Register 1.2) | C133 _H |
| PMA_DEVID2 | PHY Identifier 2 (Register 1.3) | 5400 _H ¹⁾ |
| PMA_SPEED_ABILITY | PMA/PMD Speed Ability (Register 1.4) | 2070 _H |
| PMA_DIP1 | Devices in Package 1 (Register 1.5) | 008B _H |
| PMA_DIP2 | Devices in Package 2 (Register 1.6) | C000 _H |
| PMA_CTL2 | PMA/PMD Control 2 (Register 1.7) | 0030 _H |
| PMA_STAT2 | PMA/PMD Status 2 (Register 1.8) | 8200 _H |
| PMA_EXT_ABILITY | PMA/PMD Extended Ability (Register 1.11) | 41A0 _H |
| PMA_PACKID1 | AN Package Identifier (Register 1.14) | C133 _H |
| PMA_PACKID2 | AN Package Identifier (Register 1.15) | 5400 _H ¹⁾ |
| PMA_MGBT_EXTAB | PMAPMD Extended Ability (Register 1.21) | 0001 _H |
| PMA_MGBT_STAT | MULTIGBASE-T Status (Register 1.129) | 0000 _H |
| PMA_MGBT_POLARITY | MULTIGBASE-T Pair Swap and Polarity (Register 1.130) | 0003 _H |
| PMA_MGBT_TX_PBO | MULTIGBASE-T Tx Power Backoff and PHY Short Reach Setting (Register 1.131) | 0000 _H |
| PMA_MGBT_TEST_MODE | MULTIGBASE-T Test Mode (Register 1.132) | 0000 _H |
| PMA_MGBT_SNR_OPMARGIN_A | MULTIGBASE-T SNR Margin Channel A (Register 1.133) | 0000 _H |
| PMA_MGBT_SNR_OPMARGIN_B | MULTIGBASE-T SNR Margin Channel B (Register 1.134) | 0000 _H |
| PMA_MGBT_SNR_OPMARGIN_C | MULTIGBASE-T SNR Margin Channel C (Register 1.135) | 0000 _H |
| PMA_MGBT_SNR_OPMARGIN_D | MULTIGBASE-T SNR Margin Channel D (Register 1.136) | 0000 _H |
| PMA_MGBT_MINMARGIN_A | MULTIGBASE-T SNR Minimum Margin Channel A (Register 1.137) | 0000 _H |
| PMA_MGBT_MINMARGIN_B | MULTIGBASE-T SNR Minimum Margin Channel B (Register 1.138) | 0000 _H |
| PMA_MGBT_MINMARGIN_C | MULTIGBASE-T SNR Minimum Margin Chan C (Register 1.139) | 0000 _H |
| PMA_MGBT_MINMARGIN_D | MULTIGBASE-T SNR Minimum Margin Chan D (Register 1.140) | 0000 _H |
| PMA_MGBT_POWER_A | MULTIGBASE-T Rx Power Channel A (Register 1.141) | 0000 _H |
| PMA_MGBT_POWER_B | MULTIGBASE-T Rx Power Channel B (Register 1.142) | 0000 _H |
| PMA_MGBT_POWER_C | MULTIGBASE-T Rx Power Chan C (Register 1.143) | 0000 _H |
| PMA_MGBT_POWER_D | MULTIGBASE-T Rx Power Chan D (Register 1.144) | 0000 _H |
| PMA_MGBT_SKEW_DELAY_0 | MULTIGBASE-T Skew Delay 0 (Register 1.145) | 0000 _H |
| PMA_MGBT_SKEW_DELAY_1 | MULTIGBASE-T Skew Delay 1 (Register 1.146) | 0000 _H |

Table 30 Registers Overview- Standard PMAPMD Registers (cont'd)

| Register Short Name | Register Long Name | Reset Value |
|--|--|-------------------|
| PMA_MGBT_FAST_RETRAIN_STA_CTRL | MULTIGBASE-T Skew Delay 2 (Register 1.147) | 0010 _H |
| PMA_TIMESYNC_CAP | PMA TimeSync Capability Indication (Register 1.1800) | 0000 _H |

1) For the device specific reset value, see the Product and Package Naming table in the [Product Ordering Information](#) chapter.

6.1.1 PMAPMD Register Descriptions

This section describes all the PMAPMD registers in detail.

PMA/PMD Control 1 (Register 1.0)

IEEE Standard Register=1.0

PMA_CTRL1

PMA/PMD Control 1 (Register 1.0)

Reset Value

2058_H

| | | | | | | | | | | | |
|-----|-----|-----|-----|------------|----|-----|-----|---|-----------|-----|-----|
| 15 | 14 | 13 | 12 | 11 | 10 | 7 | 6 | 5 | 2 | 1 | 0 |
| RST | RES | SSL | RES | LOW_POWER* | | RES | SSM | | SPEED_SEL | NS1 | NS2 |
| RW | | RW | | RW | | | RW | | RW | RO | RO |

| Field | Bits | Type | Description |
|-----------|------|------|--|
| RST | 15 | RW | Reset 0 _B Normal operation 1 _B PMA/PMD reset |
| SSL | 13 | RW | Speed Selection (LSB) Used in conjunction with field SPEED_SEL_MSB. MSB LSB: 00 _B 10 Mbps 01 _B 100 Mbps 10 _B 1000 Mbps 11 _B Bits [5:2] select the speed (SPEED_SEL field) |
| LOW_POWER | 11 | RW | Low Power 0 _B Normal operation 1 _B Enters low power mode. |
| SSM | 6 | RW | Speed Selection (MSB) Used in conjunction with field SPEED_SEL_LSB. MSB LSB: 00 _B 10 Mbps 01 _B 100 Mbps 10 _B 1000 Mbps 11 _B Bits [5:2] select the speed (SPEED_SEL field) |
| SPEED_SEL | 5:2 | RW | Speed Selection Bit usage (from bit 5 to bit 2): 0 0 0 0 _B Not supported. The speed defaults to 2.5 Gbps. 0 0 0 1 _B Not supported. The speed defaults to 2.5 Gbps. 0 0 1 0 _B Not supported. The speed defaults to 2.5 Gbps. 0 0 1 1 _B Not supported. The speed defaults to 2.5 Gbps. 0 1 0 0 _B Not supported. The speed defaults to 2.5 Gbps. 0 1 0 1 _B Not supported. The speed defaults to 2.5 Gbps. 0 1 1 0 _B 2.5 Gbps 0 1 1 1 _B Not supported 1 x x x _B Reserved |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|--|
| NS1 | 1 | RO | Not Supported PMA remote loopback mode is not supported by the GPHY. |
| NS2 | 0 | RO | Not Supported PMA local loopback mode is not supported by the GPHY. |

PHY Identifier 1 (Register 1.2)

IEEE Standard Register=1.2

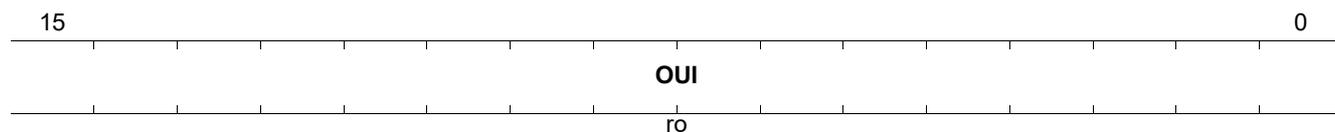
Bits 31 - 16 of device ID

PMA_DEVID1

Reset Value

PHY Identifier 1 (Register 1.2)

C133_H



| Field | Bits | Type | Description |
|-------|------|------|---|
| OUI | 15:0 | RO | Organizationally Unique Identifier Organizationally Unique Identifier Bits 3:18 |

PHY Identifier 2 (Register 1.3)

IEEE Standard Register=1.3

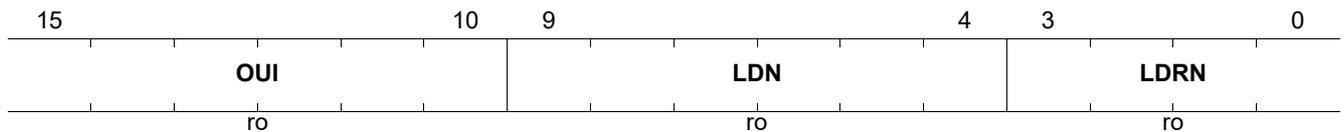
Bits 15 - 0 of device ID

PMA_DEVID2

PHY Identifier 2 (Register 1.3)

Reset Value

5400_H



| Field | Bits | Type | Description |
|-------|-------|------|---|
| OUI | 15:10 | RO | Organizationally Unique Identifier Bits 19:24 |
| LDN | 9:4 | RO | Device Number Specifies the device number ¹⁾ to distinguish between several different products. |
| LDRN | 3:0 | RO | Device Revision Number Specifies the device revision number ¹⁾ to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the [Product Ordering Information](#) chapter.

PMA/PMD Speed Ability (Register 1.4)

IEEE Standard Register=1.4

PMA_SPEED_ABILITY
Reset Value
PMA/PMD Speed Ability (Register 1.4)
2070_H

| | | | | | | | | | | | | | | | |
|-----|--------|---------|------|-----|-----|----------|---------|------------|---------|----------|-----------|-----|----------|----------|----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RES | CAP_5G | CAP_2G5 | RES2 | RES | RES | CAP_100G | CAP_40G | CAP_10_1G* | CAP_10M | CAP_100M | CAP_1000M | RES | R10PASS* | CAP_2BA* | CAP_10G* |
| | ro | ro | ro | | | ro | ro | ro | ro | ro | ro | | ro | ro | ro |

| Field | Bits | Type | Description |
|--------------------|------|------|--|
| CAP_5G | 14 | RO | Not Supported 0 _B PMA/PMD is not capable of operating as 5 Gbps. 1 _B PMA/PMD is capable of operating at 5 Gbps. |
| CAP_2G5 | 13 | RO | 2.5 G capable 0 _B PMA/PMD is not capable of operating as 2.5 Gbps. 1 _B PMA/PMD is capable of operating at 2.5 Gbps. |
| RES2 | 12 | RO | Reserved Value always 0 |
| CAP_100G | 9 | RO | Not Supported 0 _B PMA/PMD is not capable of operating as 100 Gbps. 1 _B PMA/PMD is capable of operating at 100 Gbps. |
| CAP_40G | 8 | RO | Not Supported 0 _B PMA/PMD is not capable of operating as 40 Gbps. 1 _B PMA/PMD is capable of operating at 40 Gbps. |
| CAP_10_1G | 7 | RO | Not Supported 0 _B PMA/PMD is not capable of operating at 10 Gbps downstream and 1 Gbps upstream. 1 _B PMA/PMD is capable of operating at 10 Gbps downstream and 1 Gbps upstream. |
| CAP_10M | 6 | RO | 10M capable 0 _B PMA/PMD is not capable of operating as 10 Mbps. 1 _B PMA/PMD is capable of operating at 10 Mbps. |
| CAP_100M | 5 | RO | 100M capable 0 _B PMA/PMD is not capable of operating as 100 Mbps. 1 _B PMA/PMD is capable of operating at 100 Mbps. |
| CAP_1000M | 4 | RO | 1000M capable 0 _B PMA/PMD is not capable of operating as 1000 Mbps. 1 _B PMA/PMD is capable of operating at 1000 Mbps. |
| R10PASS_TS_CAPABLE | 2 | RO | Not Supported 0 _B PMA/PMD is not capable of operating as 10PASS-TS. 1 _B PMA/PMD is capable of operating as 10PASS-TS. |

| Field | Bits | Type | Description (cont'd) |
|--------------|------|------|--|
| CAP_2BASE_TL | 1 | RO | Not Supported 0 _B PMA/PMD is not capable of operating as 2BASE-TL. 1 _B PMA/PMD is capable of operating as 2BASE-TL. |
| CAP_10G_CAP | 0 | RO | Not Supported 0 _B PMA/PMD is not capable of operating at 10 Gbps. 1 _B PMA/PMD is capable of operating at 10 Gbps. |

| Field | Bits | Type | Description (cont'd) |
|-----------|------|------|---|
| WIS | 2 | RO | WIS Present 0 _B WIS not present in package 1 _B WIS present in package |
| PMD_PMA | 1 | RO | PMD/PMA Present This bit is always set to 1 _B in the GPHY. 0 _B PMA/PMD not present in package 1 _B PMA/PMD present in package |
| CLAUSE_22 | 0 | RO | Clause 22 Registers Present This bit is always set to 1 _B in the GPHY. 0 _B Clause 22 registers not present in package 1 _B Clause 22 registers present in package |

Devices in Package 2 (Register 1.6)

IEEE Standard Register=1.6

PMA_DIP2

Devices in Package 2 (Register 1.6)

Reset Value

C000_H

| | | | | | | | | | | | |
|--------------------|--------------------|----------------------|------------|--|--|--|--|--|--|--|---|
| 15 | 14 | 13 | 12 | | | | | | | | 0 |
| VSPE C2 | VSPE C1 | CLA_2 2_* | RES | | | | | | | | |
| ro | ro | ro | ro | | | | | | | | |

| Field | Bits | Type | Description |
|------------|------|------|--|
| VSPEC2 | 15 | RO | Vendor-specific Device 2 This bit is always set to 1 _B in the GPHY. 0 _B Vendor-specific device 2 not present in package 1 _B Vendor-specific device 2 present in package |
| VSPEC1 | 14 | RO | Vendor-specific Device 1 This bit is always set to 1 _B in the GPHY. 0 _B Vendor-specific device 1 not present in package 1 _B Vendor-specific device 1 present in package |
| CLA_22_EXT | 13 | RO | Clause 22 Extension 0 _B Clause 22 extension not present in package 1 _B Clause 22 extension present in package |
| RES | 12:0 | RO | Reserved Ignore on read. |

| Field | Bits | Type | Description (cont'd) |
|----------------------|------|------|---|
| PMA_PMD_TY PE_SEL | 5:0 | RW | PMA/PMD Type Selection (cont'd) 0 0 1 1 1 1 _B 10BASE-T PMA/PMD 0 0 1 1 1 0 _B 100BASE-TX PMA/PMD 0 0 1 1 0 1 _B Unsupported, defaults to 2.5GBASE-T PMA 0 0 1 1 0 0 _B 1000BASE-T PMA/PMD 0 0 1 0 1 1 _B Unsupported, defaults to 2.5GBASE-T PMA 0 0 1 0 1 0 _B Unsupported, defaults to 2.5GBASE-T PMA 0 0 1 0 0 1 _B Unsupported, defaults to 2.5GBASE-T PMA 0 0 1 0 0 0 _B Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 1 1 1 _B Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 1 1 0 _B Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 1 0 1 _B Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 1 0 0 _B Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 0 1 1 _B Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 0 1 0 _B Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 0 0 1 _B Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 0 0 0 _B Unsupported, defaults to 2.5GBASE-T PMA |

PMA/PMD Status 2 (Register 1.8)

IEEE Standard Register=1.8

PMA_STAT2
PMA/PMD Status 2 (Register 1.8)
Reset Value
8200_H

| | | | | | | | | | | | | | | | |
|-----------------------|------------------|------------------|-----------------|-----------------|---------------------|------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|-----------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DEVICE_PRESENT | TX_FAULT* | RX_FAULT* | TX_FAULT | RX_FAULT | EXT_ABILITY* | PMD_TX_DISABLE* | RMGBT_SR_ABILITY* | RMGBT_LR_ABILITY* | RMGBT_ER_ABILITY* | RMGBT_SR_ABILITY* | RMGBT_LR_ABILITY* | RMGBT_ER_ABILITY* | RMGBT_SR_ABILITY* | RMGBT_LR_ABILITY* | PMA_LOC* |
| ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|------------------|-------|------|--|
| DEVICE_PRESENT | 15:14 | RO | Device Present 00 _B No device responding at this address 01 _B No device responding at this address 10 _B Device responding at this address 11 _B No device responding at this address |
| TX_FAULT_ABILITY | 13 | RO | Transmit Fault Ability 0 _B PMA/PMD is not able to detect a fault condition on the transmit path. 1 _B PMA/PMD is able to detect a fault condition on the transmit path. |
| RX_FAULT_ABILITY | 12 | RO | Receive Fault Ability 0 _B PMA/PMD is not able to detect a fault condition on the receive path. 1 _B PMA/PMD is able to detect a fault condition on the receive path. |
| TX_FAULT | 11 | RO | Transmit Fault 0 _B No fault condition on transmit path 1 _B Fault condition on transmit path |
| RX_FAULT | 10 | RO | Receive Fault 0 _B No fault condition on receive path 1 _B Fault condition on receive path |
| EXT_ABILITIES | 9 | RO | Extended Abilities 0 _B PMA/PMD does not have extended abilities. 1 _B PMA/PMD has extended abilities listed in register 1.11. |
| PMD_TX_DISABLE | 8 | RO | PMD Transmit Disable 0 _B PMD is not able to disable the transmit path. 1 _B PMD is able to disable the transmit path. |
| RMGBT_SR_ABILITY | 7 | RO | MULTIGBASE-SR Ability 0 _B PMA/PMD is not able to perform MULTIGBASE-SR. 1 _B PMA/PMD is able to perform MULTIGBASE-SR. |
| RMGBT_LR_ABILITY | 6 | RO | MULTIGBASE-LR Ability 0 _B PMA/PMD is not able to perform MULTIGBASE-LR. 1 _B PMA/PMD is able to perform MULTIGBASE-LR. |
| RMGBT_ER_ABILITY | 5 | RO | MULTIGBASE-ER Ability 0 _B PMA/PMD is not able to perform MULTIGBASE-ER. 1 _B PMA/PMD is able to perform MULTIGBASE-ER. |

| Field | Bits | Type | Description (cont'd) |
|--------------------|------|------|---|
| RMGBT_LX4_ABILITY | 4 | RO | MULTIGBASE-LX4 Ability 0 _B PMA/PMD is not able to perform MULTIGBASE-LX4. 1 _B PMA/PMD is able to perform MULTIGBASE-LX4. |
| RMGBT_SW_ABILITY | 3 | RO | MULTIGBASE-SW Ability 0 _B PMA/PMD is not able to perform MULTIGBASE-SW. 1 _B PMA/PMD is able to perform MULTIGBASE-SW. |
| RMGBT_LW_ABILITY | 2 | RO | MULTIGBASE-LW Ability 0 _B PMA/PMD is not able to perform MULTIGBASE-LW. 1 _B PMA/PMD is able to perform MULTIGBASE-LW. |
| RMGBT_EW_ABILITY | 1 | RO | MULTIGBASE-EW Ability 0 _B PMA/PMD is not able to perform MULTIGBASE-EW. 1 _B PMA/PMD is able to perform MULTIGBASE-EW. |
| PMA_LOCAL_LOOPBACK | 0 | RO | PMA Local Loopback 0 _B PMA is not able to perform a local loopback function. 1 _B PMA is able to perform a local loopback function. |

PMA/PMD Extended Ability (Register 1.11)

IEEE Standard Register=1.11

PMA_EXT_ABILITY
PMA/PMD Extended Ability (Register 1.11)
Reset Value
41A0_H

| | | | | | | | | | | | | | | | |
|-----|----------|----|-----|----|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 15 | 14 | 13 | | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RES | R2G5_EX* | | RES | | R40G_10* | P2MP_AB* | R10B_ASE* | R100B_AS* | R1000_BA* | R1000_BA* | RMGB_T_K* | RMGB_T_K* | RMGB_T_A* | RMGB_T_L* | RMGB_T_C* |
| | ro | | | | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|-------------------------|------|------|--|
| R2G5_EXT_ABILITIES | 14 | RO | 2.5G/5G Extended Abilities 0 _B PMA/PMD does not have 2.5G/5G extended abilities. 1 _B PMA/PMD has 2.5G/5G extended abilities listed in register 1.21. |
| R40G_100G_EXT_ABILITIES | 10 | RO | 40G/100G Extended Abilities 0 _B PMA/PMD does not have 40G/100G extended abilities. 1 _B PMA/PMD has 40G/100G extended abilities listed in register 1.13. |
| P2MP_ABILITY | 9 | RO | P2MP Ability 0 _B PMA/PMD does not have P2MP extended abilities. 1 _B PMA/PMD has P2MP abilities listed in register 1.12. |
| R10BASE_T_ABILITY | 8 | RO | 10BASE-T Ability 0 _B PMA/PMD is not able to perform 10BASE-T. 1 _B PMA/PMD is able to perform 10BASE-T. |
| R100BASE_TX_ABILITY | 7 | RO | 100BASE-TX Ability 0 _B PMA/PMD is not able to perform 100BASE-TX. 1 _B PMA/PMD is able to perform 100BASE-TX. |
| R1000BASE_KX_ABILITY | 6 | RO | 1000BASE-KX Ability 0 _B PMA/PMD is not able to perform 1000BASE-KX. 1 _B PMA/PMD is able to perform 1000BASE-KX. |
| R1000BASE_T_ABILITY | 5 | RO | 1000BASE-T Ability 0 _B PMA/PMD is not able to perform 1000BASE-T. 1 _B PMA/PMD is able to perform 1000BASE-T. |
| RMGBT_KR_ABILITY | 4 | RO | MULTIGBASE-KR Ability 0 _B PMA/PMD is not able to perform MULTIGBASE-KR. 1 _B PMA/PMD is able to perform MULTIGBASE-KR. |
| RMGBT_KX4_ABILITY | 3 | RO | MULTIGBASE-KX4 Ability 0 _B PMA/PMD is not able to perform MULTIGBASE-KX4. 1 _B PMA/PMD is able to perform MULTIGBASE-KX4. |
| RMGBT_ABILITY | 2 | RO | 10GBASE-T Ability 0 _B PMA/PMD is not able to perform MULTIGBASE-T. 1 _B PMA/PMD is able to perform MULTIGBASE-T. |
| RMGBT_LRM_ABILITY | 1 | RO | MULTIGBASE-LRM Ability 0 _B PMA/PMD is not able to perform MULTIGBASE-LRM. 1 _B PMA/PMD is able to perform MULTIGBASE-LRM. |

| Field | Bits | Type | Description (cont'd) |
|-------------------|------|------|---|
| RMGBT_CX4_ABILITY | 0 | RO | MULTIGBASE-CX4 Ability 0 _B PMA/PMD is not able to perform MULTIGBASE-CX4. 1 _B PMA/PMD is able to perform MULTIGBASE-CX4. |

AN Package Identifier (Register 1.14)

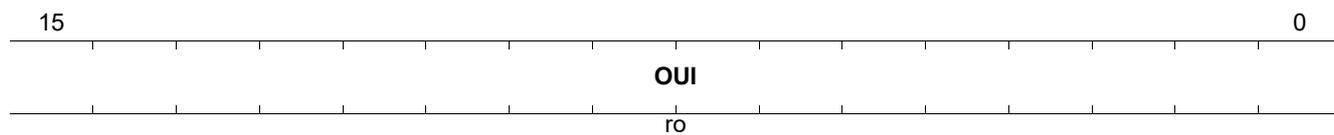
IEEE Standard Register=1.14

PMA_PACKID1

Reset Value

AN Package Identifier (Register 1.14)

C133_H



| Field | Bits | Type | Description |
|-------|------|------|---|
| OUI | 15:0 | RO | Organizationally Unique Identifier Organizationally Unique Identifier Bits 3:18 |

AN Package Identifier (Register 1.15)

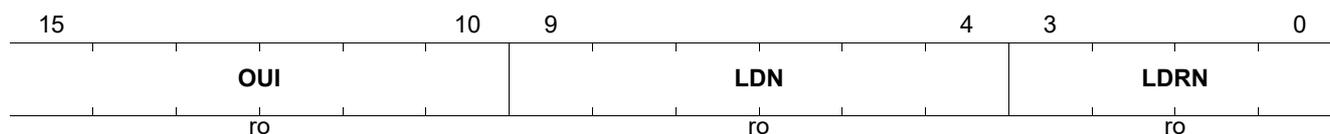
IEEE Standard Register=1.15

PMA_PACKID2

AN Package Identifier (Register 1.15)

Reset Value

5400_H



| Field | Bits | Type | Description |
|-------|-------|------|---|
| OUI | 15:10 | RO | Organizationally Unique Identifier Bits 19:24 |
| LDN | 9:4 | RO | Device Number Specifies the device number ¹⁾ to distinguish between several different products. |
| LDRN | 3:0 | RO | Device Revision Number Specifies the device revision number ¹⁾ to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the [Product Ordering Information](#) chapter.

PMA_PMD Extended Ability (Register 1.21)

Read only. Write from the STA has no effect.

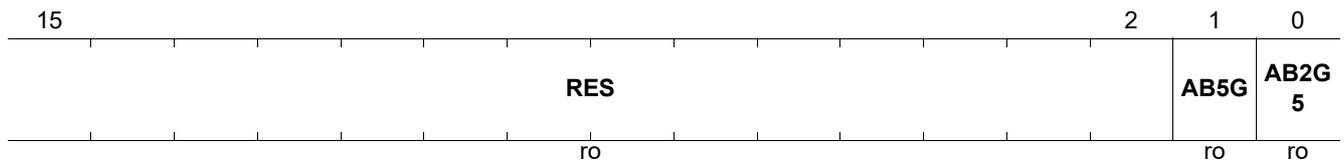
IEEE Standard Register=1.21

PMA_MGBT_EXTAB

PMA_PMD Extended Ability (Register 1.21)

Reset Value

0001_H



| Field | Bits | Type | Description |
|-------|------|------|--|
| RES | 15:2 | RO | Reserved Value always 0 |
| AB5G | 1 | RO | PMA Ability to Perform 5GBASE-T 0 _B UNABLE PMA is not able to perform 5GBASE-T. 1 _B ABLE PMA is able to perform 5GBASE-T. |
| AB2G5 | 0 | RO | PMA Ability to Perform 2.5GBASE-T 0 _B UNABLE PMA is not able to perform 2.5GBASE-T. 1 _B ABLE PMA is able to perform 2.5GBASE-T. |

MULTIGBASE-T Pair Swap and Polarity (Register 1.130)

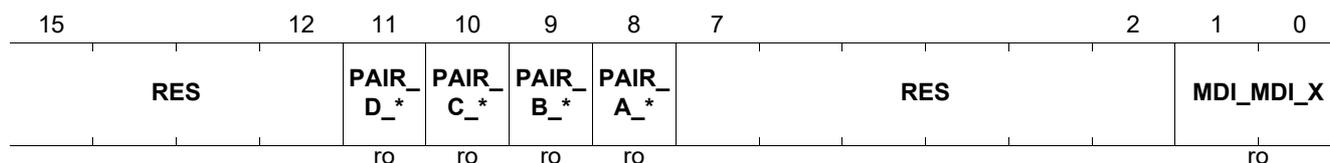
IEEE Standard Register=1.130

PMA_MGBT_POLARITY

Reset Value

MULTIGBASE-T Pair Swap and Polarity (Register 1.130)

0003_H



| Field | Bits | Type | Description |
|-----------------|------|------|--|
| PAIR_D_POLARITY | 11 | RO | Pair D Polarity 0 _B Polarity of pair D is not reversed. 1 _B Polarity of pair D is reversed. |
| PAIR_C_POLARITY | 10 | RO | Pair C Polarity 0 _B Polarity of pair C is not reversed. 1 _B Polarity of pair C is reversed. |
| PAIR_B_POLARITY | 9 | RO | Pair B Polarity 0 _B Polarity of pair B is not reversed. 1 _B Polarity of pair B is reversed. |
| PAIR_A_POLARITY | 8 | RO | Pair A Polarity 0 _B Polarity of pair A is not reversed. 1 _B Polarity of pair A is reversed. |
| MDI_MDI_X | 1:0 | RO | MDI/MDI-X Indicates the status of pair swaps at the MDI / MD-X. 00 _B ABCD CROSS Pair AB and Pair CD crossover 01 _B CD CROSS Pair CD crossover only 10 _B AB CROSS Pair AB crossover only 11 _B NORMAL No crossover |

MULTIGBASE-T Tx Power Backoff and PHY Short Reach Setting (Register 1.131)

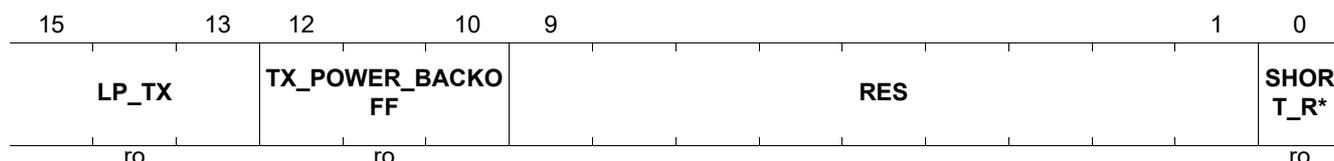
IEEE Standard Register=1.131

PMA_MGBT_TX_PBO

Reset Value

MULTIGBASE-T TX Power Backoff and PHY Short Reach Setting (Register 1.131)

0000_H



| Field | Bits | Type | Description |
|------------------|-------|------|---|
| LP_TX | 15:13 | RO | Link Partner Tx The power backoff setting of the link partner. The bit number assignment order is: 15 14 13 000 _B 0 dB 001 _B 2 dB 010 _B 4 dB 011 _B 6 dB 100 _B 8 dB 101 _B 10 dB 110 _B 12 dB 111 _B 14 dB |
| TX_POWER_BACKOFF | 12:10 | RO | Tx Power Backoff The power backoff of PHY211 PMA. The bit number assignment order is: 12 11 10 000 _B 0 dB 001 _B 2 dB 010 _B 4 dB 011 _B 6 dB 100 _B 8 dB 101 _B 10 dB 110 _B 12 dB 111 _B 14 dB |
| SHORT_REACH_MODE | 0 | RO | Short Reach Mode 0 _B PHY is not operating in short reach mode 1 _B PHY is operating in short reach mode (not supported) |

MULTIGBASE-T Test Mode (Register 1.132)

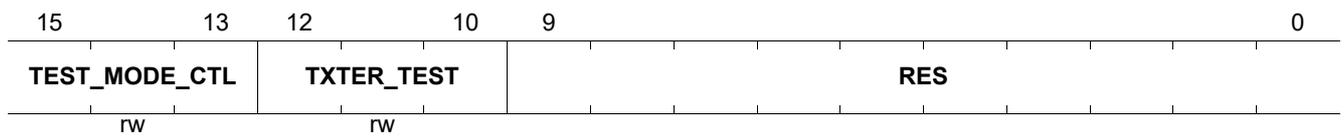
IEEE Standard Register=1.132

PMA_MGBT_TEST_MODE

Reset Value

MULTIGBASE-T Test Mode (Register 1.132)

0000_H



| Field | Bits | Type | Description |
|---------------|-------|------|--|
| TEST_MODE_CTL | 15:13 | RW | Test Mode Control 000 _B Normal operation 001 _B Test mode 1 010 _B Test mode 2 011 _B Test mode 3 100 _B Test mode 4 101 _B Test mode 5 110 _B Test mode 6 111 _B Test mode 7 |
| TXTER_TEST | 12:10 | RW | Transmitter Test Frequencies for tones used in Test Mode 4. 000 _B Reserved 001 _B Dual tone 1 010 _B Dual tone 2 011 _B Reserved 100 _B Dual tone 3 101 _B Dual tone 4 110 _B Dual tone 5 111 _B Reserved |

MULTIGBASE-T SNR Margin Channel A (Register 1.133)

Register 1.133 contains the current SNR operating margin measured at the slicer input for channel A for the MULTIGBASE-T PMA.

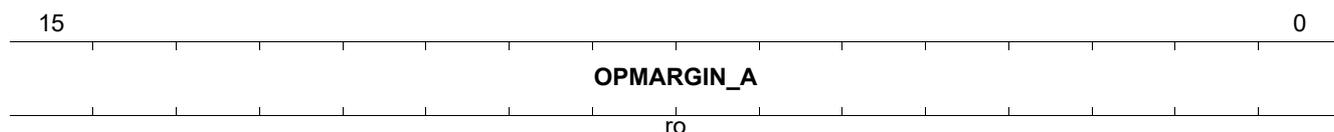
IEEE Standard Register=1.133

PMA_MGBT_SNR_OPMARGIN_A

Reset Value

MULTIGBASE-T SNR Margin Channel A (Register 1.133)

0000_H



| Field | Bits | Type | Description |
|------------|------|------|--|
| OPMARGIN_A | 15:0 | RO | OPMARGIN_A SNR operating margin measured at the slicer input for channel A |

MULTIGBASE-T SNR Margin Channel B (Register 1.134)

Register 1.134 contains the current SNR operating margin measured at the slicer input for channel B for the MULTIGBASE-T PMA.

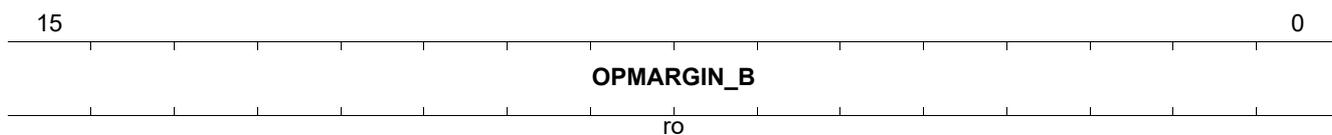
IEEE Standard Register=1.134

PMA_MGBT_SNR_OPMARGIN_B

Reset Value

MULTIGBASE-T SNR Margin Channel B (Register 1.134)

0000_H



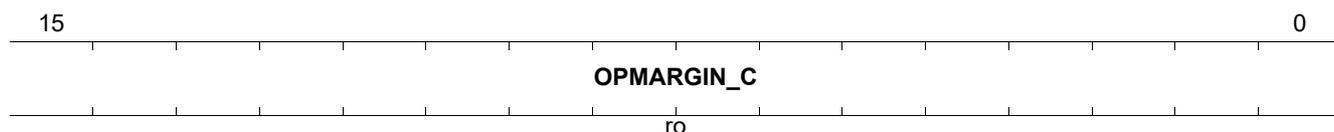
| Field | Bits | Type | Description |
|------------|------|------|--|
| OPMARGIN_B | 15:0 | RO | OPMARGIN_B SNR operating margin measured at the slicer input for channel B |

MULTIGBASE-T SNR Margin Channel C (Register 1.135)

Register 1.135 contains the current SNR operating margin measured at the slicer input for channel C for the MULTIGBASE-T PMA.

IEEE Standard Register=1.135

PMA_MGBT_SNR_OPMARGIN_C **Reset Value**
MULTIGBASE-T SNR Margin Channel C (Register 1.135) **0000_H**



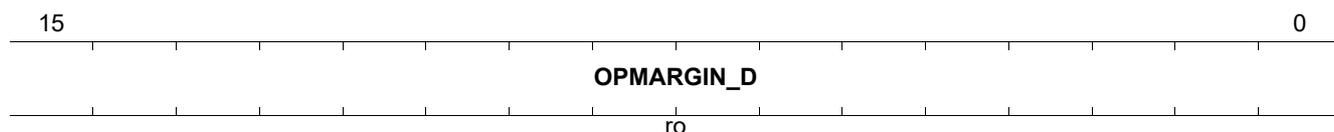
| Field | Bits | Type | Description |
|------------|------|------|--|
| OPMARGIN_C | 15:0 | RO | OPMARGIN_C SNR operating margin measured at the slicer input for channel C |

MULTIGBASE-T SNR Margin Channel D (Register 1.136)

Register 1.136 contains the current SNR operating margin measured at the slicer input for channel D for the MULTIGBASE-T PMA.

IEEE Standard Register=1.136

PMA_MGBT_SNR_OPMARGIN_D **Reset Value**
MULTIGBASE-T SNR Margin Channel D (Register 1.136) **0000_H**



| Field | Bits | Type | Description |
|------------|------|------|--|
| OPMARGIN_D | 15:0 | RO | OPMARGIN_D SNR operating margin measured at the slicer input for channel D |

MULTIGBASE-T SNR Minimum Margin Channel A (Register 1.137)

The minimum margin channel A register contains a latched copy of the lowest value observed in the SNR operating margin channel A register (1.133) since the last read.

IEEE Standard Register=1.137

PMA_MGBT_MINMARGIN_A

Reset Value

MULTIGBASE-T SNR Minimum Margin Channel A (Register 1.137)

0000_H



| Field | Bits | Type | Description |
|-------------|------|------|--|
| MINMARGIN_A | 15:0 | RO | MINMARGIN_A Lowest value observed in the SNR operating margin channel A register (1.133) since the last read |

MULTIGBASE-T SNR Minimum Margin Channel B (Register 1.138)

The minimum margin channel A register contains a latched copy of the lowest value observed in the SNR operating margin channel B register (1.134) since the last read.

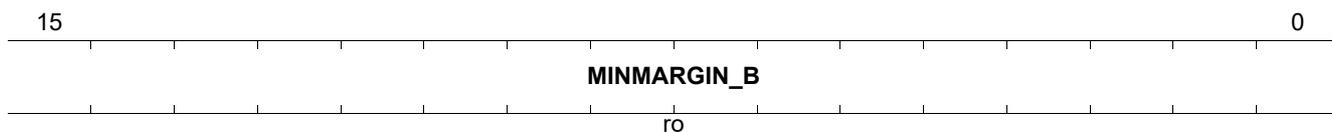
IEEE Standard Register=1.138

PMA_MGBT_MINMARGIN_B

Reset Value

MULTIGBASE-T SNR Minimum Margin Channel B (Register 1.138)

0000_H



| Field | Bits | Type | Description |
|-------------|------|------|--|
| MINMARGIN_B | 15:0 | RO | MINMARGIN_B Lowest value observed in the SNR operating margin channel B register (1.134) since the last read |

MULTIGBASE-T SNR Minimum Margin Chan C (Register 1.139)

The minimum margin channel C register contains a latched copy of the lowest value observed in the SNR operating margin channel C register (1.135) since the last read.

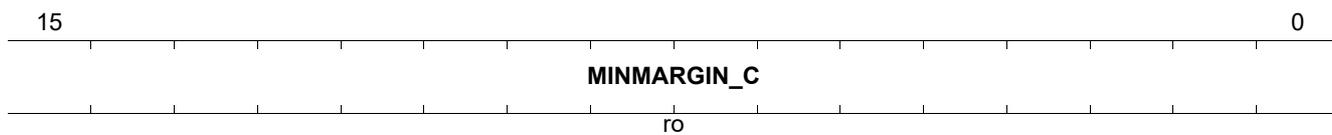
IEEE Standard Register=1.139

PMA_MGBT_MINMARGIN_C

Reset Value

MULTIGBASE-T SNR Minimum Margin Chan C (Register 1.139)

0000_H



| Field | Bits | Type | Description |
|-------------|------|------|--|
| MINMARGIN_C | 15:0 | RO | MINMARGIN_C Lowest value observed in the SNR operating margin channel C register (1.135) since the last read |

MULTIGBASE-T SNR Minimum Margin Chan D (Register 1.140)

The Minimum margin channel D register contains a latched copy of the lowest value observed in the SNR operating margin channel D register (1.136) since the last read.

IEEE Standard Register=1.140

PMA_MGBT_MINMARGIN_D

Reset Value

MULTIGBASE-T SNR Minimum Margin Chan D (Register 1.140)

0000_H

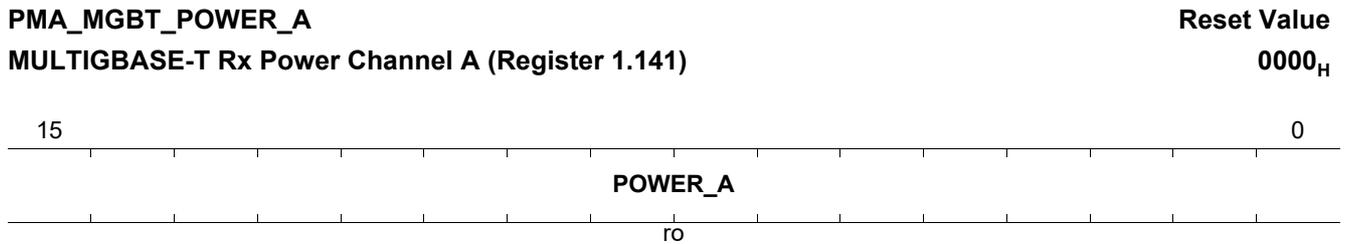


| Field | Bits | Type | Description |
|-------------|------|------|--|
| MINMARGIN_D | 15:0 | RO | MINMARGIN_D Lowest value observed in the SNR operating margin channel D register (1.136) since the last read |

MULTIGBASE-T Rx Power Channel A (Register 1.141)

The Rx signal power channel A register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.141



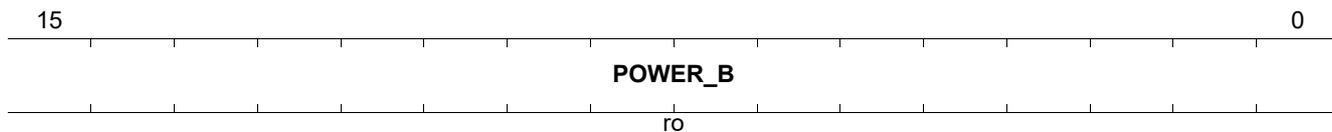
| Field | Bits | Type | Description |
|---------|------|------|--|
| POWER_A | 15:0 | RO | POWER_A Receive signal power measured at the MDI during training |

MULTIGBASE-T Rx Power Channel B (Register 1.142)

The Rx signal power channel B register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.142

PMA_MGBT_POWER_B **Reset Value**
MULTIGBASE-T Rx Power Channel B (Register 1.142) **0000_H**



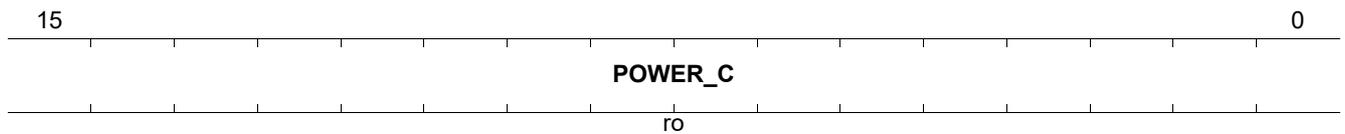
| Field | Bits | Type | Description |
|---------|------|------|--|
| POWER_B | 15:0 | RO | POWER_B Receive signal power measured at the MDI during training |

MULTIGBASE-T Rx Power Chan C (Register 1.143)

The Rx signal power channel C register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.143

PMA_MGBT_POWER_C **Reset Value**
MULTIGBASE-T Rx Power Chan C (Register 1.143) **0000_H**

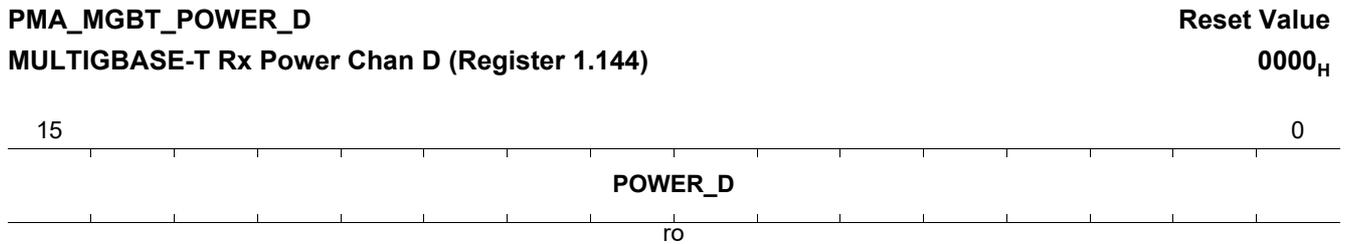


| Field | Bits | Type | Description |
|---------|------|------|--|
| POWER_C | 15:0 | RO | POWER_C Receive signal power measured at the MDI during training |

MULTIGBASE-T Rx Power Chan D (Register 1.144)

The Rx signal power channel D register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.144



| Field | Bits | Type | Description |
|---------|------|------|--|
| POWER_D | 15:0 | RO | POWER_D Receive signal power measured at the MDI during training |

MULTIGBASE-T Skew Delay 0 (Register 1.145)

IEEE Standard Register=1.145

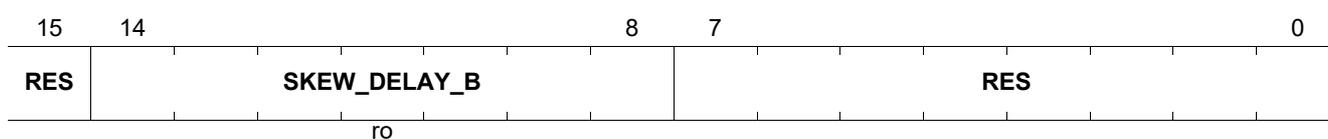
The skew delay reports the current skew delay on each of the pairs with respect to physical pair A. It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. When the delay exceeds the maximum amount represented by the range -80 ns to +78.75 ns, the field displays the maximum value.

PMA_MGBT_SKEW_DELAY_0

Reset Value

MULTIGBASE-T Skew Delay 0 (Register 1.145)

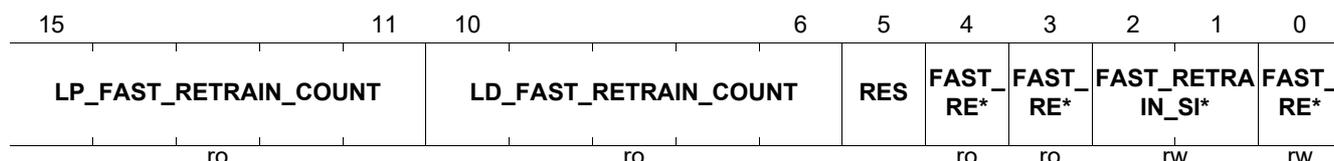
0000_H



| Field | Bits | Type | Description |
|--------------|------|------|--|
| SKEW_DELAY_B | 14:8 | RO | Skew Delay B Skew delay for pair B |

MULTIGBASE-T Skew Delay 2 (Register 1.147)

IEEE Standard Register=1.147

PMA_MGBT_FAST_RETRAIN_STA_CTRL
MULTIGBASE-T Skew Delay 2 (Register 1.147)
Reset Value
0010_H


| Field | Bits | Type | Description |
|-------------------------|-------|------|---|
| LP_FAST_RETRAIN_COUNT | 15:11 | RO | LP Fast Retrain Count Counts the number of fast retrains requested by the link partner. |
| LD_FAST_RETRAIN_COUNT | 10:6 | RO | LD Fast Retrain Count Counts the number of fast retrains requested by the local device. |
| FAST_RETRAIN_ABILITY | 4 | RO | Fast Retrain Ability 0 _B Fast retrain capability is not supported. 1 _B Fast retrain capability is supported. |
| FAST_RETRAIN_NEGOTIATED | 3 | RO | Fast Retrain Negotiated 0 _B Fast retrain capability was not negotiated. 1 _B Fast retrain capability was negotiated. |
| FAST_RETRAIN_SIG_TYPE | 2:1 | RW | Fast Retrain Signal Type 00 _B PHY signals IDLE during fast retrain 01 _B PHY signals local fault during fast retrain 10 _B PHY signals link interruption during fast retrain 11 _B Reserved |
| FAST_RETRAIN_ENABLE | 0 | RW | Fast Retrain Enable 0 _B Fast retrain capability is disabled. 1 _B Fast retrain capability is enabled. |

6.2 Standard PCS Registers

This section describes the PCS registers for MMD device 0x03.

Table 31 Registers Overview- Standard PCS Registers

| Register Short Name | Register Long Name | Reset Value |
|-----------------------------------|--|---------------------------------|
| PCS_CTRL1 | PCS Control 1 (Register 3.0) | 205C _H |
| PCS_STAT1 | PCS Status 1 (Register 3.1) | 0000 _H |
| PCS_DEVID1 | PHY Identifier 1 (Register 3.2) | C133 _H |
| PCS_DEVID2 | PHY Identifier 2 (Register 3.3) | 5400 _H ¹⁾ |
| PCS_SPEED_ABILITY | PCS Speed Ability (Register 3.4) | 0040 _H |
| PCS_DIP1 | PCS Devices in Package 1 (Register 3.5) | 008B _H |
| PCS_DIP2 | PCS Devices in Package 2 (Register 3.6) | C000 _H |
| PCS_CTRL2 | PCS Control 2 (Register 3.7) | 000A _H |
| PCS_STAT2 | PCS Status 2 (Register 3.8) | 9000 _H |
| PCS_PACKID1 | PCS Package Identifier 1 (Register 3.14) | C133 _H |
| PCS_PACKID2 | PCS Package Identifier 2 (Register 3.15) | 5400 _H ¹⁾ |
| PCS_EEE_CAP | PCS EEE Capability (Register 3.20) | 0006 _H |
| PCS_EEE_CAP2 | EEE Control and Capability 2 (Register 3.21) | 0001 _H |
| PCS_EEE_WAKERR | PCS EEE Status Register 1 (Register 3.22) | 0000 _H |
| PCS_2G5_STAT1 | BASE-R and 10GBASE-T PCS Status 1 (Register 3.32) | 0000 _H |
| PCS_2G5_STAT2 | MULTIGBASE-T PCS Status 2 (Register 3.33) | 0000 _H |
| PCS_TIMESYNC_CAP | PCS TimeSync Capability Register (Register 3.1800) | 0000 _H |

1) For the device specific reset value, see the Product and Package Naming table in the [Product Ordering Information](#) chapter.

6.2.1 PCS Register Descriptions

This section describes all the PCS registers in detail.

PCS Control 1 (Register 3.0)

IEEE Standard Register=3.0

PCS_CTRL1

PCS Control 1 (Register 3.0)

Reset Value

205C_H

| | | | | | | | | | | | | |
|-----|----------|-----|-----|------------|--------|-----|---|-----|-----------|----|-----|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 7 | 6 | 5 | 2 | 1 | 0 |
| RST | LOOPBACK | SSL | RES | LOW_POWER* | RXCKST | RES | | SSM | SPEED_SEL | | RES | |
| RW | RW | RW | | RW | RW | | | RW | | RW | | |

| Field | Bits | Type | Description |
|-----------|------|------|---|
| RST | 15 | RW | Reset 0 _B Normal operation 1 _B PCS reset - Self-clearing |
| LOOPBACK | 14 | RW | Loopback 0 _B Disable loopback mode 1 _B Enable loopback mode |
| SSL | 13 | RW | Forced Speed Selection (LSB) This bit is used in conjunction with SPEED_SEL_LSB. The bit assignment order is: MSB LSB 00 _B 10 Mbps 01 _B 100 Mbps 10 _B 1000 Mbps 11 _B Bits [5:2] select the speed |
| LOW_POWER | 11 | RW | Low Power 0 _B Normal operation 1 _B Low-power mode |
| RXCKST | 10 | RW | Clock Stop Enable The MAC sets this bit to active to allow the GPHY to stop the clocking during the LPI_MODE. 0 _B The clock is not stoppable. 1 _B The GPHY stops the (X)GMII clock during LPI. |
| SSM | 6 | RW | Forced Speed Selection (MSB) This bit is used in conjunction with SPEED_SEL_MSB. The bit assignment order is: MSB LSB 00 _B 10 Mbps 01 _B 100 Mbps 10 _B 1000 Mbps 11 _B Bits [5:2] select the speed |

| Field | Bits | Type | Description (cont'd) |
|-----------|------|------|---|
| SPEED_SEL | 5:2 | RW | Forced Speed Selection Values 0 0 0 0 _B Unsupported, defaults to 2.5 Gbps 0 0 0 1 _B Unsupported, defaults to 2.5 Gbps 0 0 1 0 _B Unsupported, defaults to 2.5 Gbps 0 0 1 1 _B Unsupported, defaults to 2.5 Gbps 0 1 0 0 _B Unsupported, defaults to 2.5 Gbps 0 1 0 1 _B Reserved 0 1 1 1 _B 2.5 Gbps 1 1 x x _B Reserved |

PCS Status 1 (Register 3.1)

IEEE Standard Register=3.1

PCS_STAT1

PCS Status 1 (Register 3.1)

Reset Value

0000_H

| | | | | | | | | | | | | | |
|-----|----|----|-------------|-------------|-------------|-------------|-----------|------------|-----|---|--------------|--------------|-----|
| 15 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 3 | 2 | 1 | 0 | |
| RES | | | TX_LP L* | RX_LP L* | TX_LP L* | RX_LP L* | FAUL T | TXCK ST | RES | | PCS_ RX_* | LOW_ POW* | RES |
| | | | ro | ro | ro | ro | ro | ro | | | ro | ro | |

| Field | Bits | Type | Description |
|--------------------|------|------|--|
| TX_LPI_RXD | 11 | RO | Tx LPI Received 0 _B LPI not received 1 _B Tx PCS received LPI |
| RX_LPI_RXD | 10 | RO | Rx LPI Received 0 _B LPI not received 1 _B Rx PCS received LPI |
| TX_LPI_INDICATION | 9 | RO | Tx LPI Indication 0 _B PCS is not currently receiving LPI. 1 _B Tx PCS is currently receiving LPI. |
| RX_LPI_INDICATION | 8 | RO | Rx LPI Indication 0 _B PCS is not currently receiving LPI. 1 _B Rx PCS is currently receiving LPI. |
| FAULT | 7 | RO | Fault 0 _B No fault condition detected 1 _B Fault condition detected |
| TXCKST | 6 | RO | Clock Stop Capable 0 _B The clock is not stoppable. 1 _B The MAC is allowed to stop the clock during LPI. |
| PCS_RX_LINK_STATUS | 2 | RO | PCS Receive Link Status 0 _B PCS receive link down 1 _B PCS receive link up |
| LOW_POWER_ABILITY | 1 | RO | Low Power Ability 0 _B PCS does not support low power mode. 1 _B PCS supports low power mode. |

PHY Identifier 1 (Register 3.2)

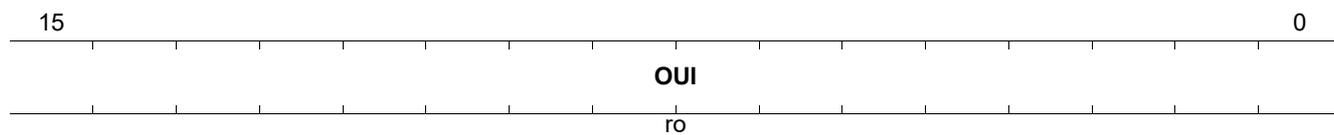
IEEE Standard Register=3.2

PCS_DEVID1

PHY Identifier 1 (Register 3.2)

Reset Value

C133_H



| Field | Bits | Type | Description |
|-------|------|------|--|
| OUI | 15:0 | RO | Organizationally Unique Identifier Bits 3:18 |

PHY Identifier 2 (Register 3.3)

Organizationally Unique Identifier Bits 19:24

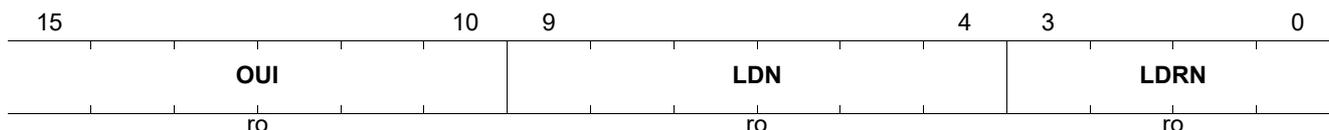
IEEE Standard Register=3.3

PCS_DEVID2

PHY Identifier 2 (Register 3.3)

Reset Value

5400_H



| Field | Bits | Type | Description |
|-------|-------|------|---|
| OUI | 15:10 | RO | Organizationally Unique Identifier Bits 19:24 |
| LDN | 9:4 | RO | Device Number Specifies the device number ¹⁾ to distinguish between several different products. |
| LDRN | 3:0 | RO | Device Revision Number Specifies the device revision number ¹⁾ to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the [Product Ordering Information](#) chapter.

PCS Speed Ability (Register 3.4)

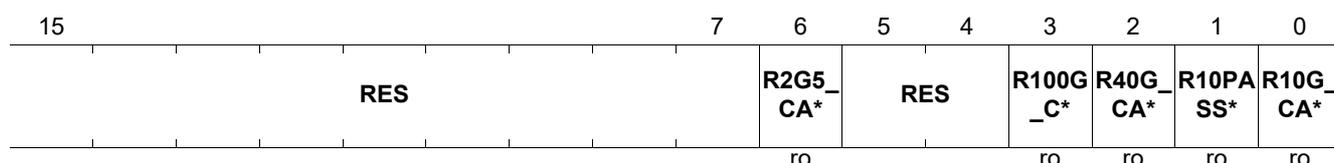
IEEE Standard Register=3.4

PCS_SPEED_ABILITY

PCS Speed Ability (Register 3.4)

Reset Value

0040_H



| Field | Bits | Type | Description |
|---------------------|------|------|---|
| R2G5_CAPABLE | 6 | RO | 2G5 Capable This bit is always set to 1 _B because the PCS is capable of operating at 2.5 Gbps. |
| R100G_CAPABLE | 3 | RO | 100G Capable 0 _B PCS is not capable of operating at 100 Gbps. 1 _B PCS is capable of operating at 100 Gbps. |
| R40G_CAPABLE | 2 | RO | 40G Capable 0 _B PCS is not capable of operating at 40 Gbps. 1 _B PCS is capable of operating at 40 Gbps. |
| R10PASS_TS_2BASE_TL | 1 | RO | 10PASS-TS/2BASE-TL Capable 0 _B PCS is not capable of operating as the 10P/2B PCS. 1 _B PCS is capable of operating as the 10P/2B PCS. |
| R10G_CAPABLE | 0 | RO | 10G Capable 0 _B PCS is not capable of operating at 10 Gbps. 1 _B PCS is capable of operating at 10 Gbps. |

PCS Devices in Package 1 (Register 3.5)

IEEE Standard Register=3.5

PCS_DIP1
Reset Value
PCS Devices in Package 1 (Register 3.5)
008B_H

| | | | | | | | | | | | | | |
|-----|----|--------------|--------------|--------------|--------------|------|----|------------|------------|-----|--------------|-------------|------|
| 15 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RES | | SEPA RAT* | SEP_P MA* | SEPA RAT* | SEPA RAT* | ANEG | TC | DTE_X S | PHY_ XS | PCS | WIS_P RE* | PMD_ PMA | CL22 |
| ro | | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|-----------------|-------|------|---|
| RES | 15:12 | RO | Reserved Ignore on read |
| SEPARATED_PMA_4 | 11 | RO | Separate PMA (4) 0 _B Separate PMA (4) not present in package 1 _B Separate PMA (4) present in package |
| SEP_PMA_3 | 10 | RO | Separate PMA (3) 0 _B Separate PMA (3) not present in package 1 _B Separate PMA (3) present in package |
| SEPARATED_PMA_2 | 9 | RO | Separate PMA (2) 0 _B Separate PMA (2) not present in package 1 _B Separate PMA (2) present in package |
| SEPARATED_PMA_1 | 8 | RO | Separate PMA (1) 0 _B Separate PMA (1) not present in package 1 _B Separate PMA (1) present in package |
| ANEG | 7 | RO | Auto-Negotiation Present 0 _B Auto-negotiation not present in package 1 _B Auto-negotiation present in package |
| TC | 6 | RO | TC Present 0 _B TC not present in package 1 _B TC present in package |
| DTE_XS | 5 | RO | DTE XS Present 0 _B DTE XS not present in package 1 _B DTE XS present in package |
| PHY_XS | 4 | RO | PHY XS Present 0 _B PHY XS not present in package 1 _B PHY XS present in package |
| PCS | 3 | RO | PCS Present 0 _B PCS not present in package 1 _B PCS present in package |
| WIS_PRESENT | 2 | RO | WIS Present 0 _B WIS not present in package 1 _B WIS present in package |

| Field | Bits | Type | Description (cont'd) |
|---------|------|------|--|
| PMD_PMA | 1 | RO | PMD/PMA Present 0 _B PMA/PMD not present in package 1 _B PMA/PMD present in package |
| CL22 | 0 | RO | Clause 22 Registers Present 0 _B Clause 22 registers not present in package 1 _B Clause 22 registers present in package |

PCS Devices in Package 2 (Register 3.6)

IEEE Standard Register=3.6

PCS_DIP2

Reset Value

PCS Devices in Package 2 (Register 3.6)

C000_H

| | | | | | | | | | | | |
|----------------------|----------------------|----------------------|------------|--|--|--|--|--|--|--|---|
| 15 | 14 | 13 | 12 | | | | | | | | 0 |
| VEND OR_* | VEND OR_* | CLAU SE_* | RES | | | | | | | | |
| ro | ro | ro | ro | | | | | | | | |

| Field | Bits | Type | Description |
|--------------------------|------|------|---|
| VENDOR_SPECIFIC_DEVICE_2 | 15 | RO | Vendor-specific Device 2 0 _B Vendor-specific device 2 not present in package 1 _B Vendor-specific device 2 present in package |
| VENDOR_SPECIFIC_DEVICE_1 | 14 | RO | Vendor-specific Device 1 0 _B Vendor-specific device 1 not present in package 1 _B Vendor-specific device 1 present in package |
| CLAUSE_22_EXTENSION | 13 | RO | Clause 22 Extension 0 _B Clause 22 extension not present in package 1 _B Clause 22 extension present in package |
| RES | 12:0 | RO | Reserved Ignore on read. |

PCS Status 2 (Register 3.8)

IEEE Standard Register=3.8

PCS_STAT2
PCS Status 2 (Register 3.8)
Reset Value
9000_H

| | | | | | | | | | | | | | |
|-----------------------|------------|-----------------|-----------------|-----------------|------------|---|---|------------------|------------------|------------------|------------------|------------------|------------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DEVICE_PRESENT | RES | R2G5_CA* | TX_FAULT | RX_FAULT | RES | | | R100G_BA* | R40G_BAS* | R10G_BAS* | R10G_BAS* | R10G_BAS* | R10G_BAS* |
| ro | | ro | ro | ro | | | | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---------------------|-------|------|--|
| DEVICE_PRESENT | 15:14 | RO | Device Present 00 _B No device responding at this address 01 _B No device responding at this address 10 _B Device responding at this address 11 _B No device responding at this address |
| R2G5_CAPABLE | 12 | RO | 2G5BASE-T Capable 0 _B PCS is not able to support 2.5GBASE-T PCS type. 1 _B PCS is able to support 2.5GBASE-T PCS type. |
| TX_FAULT | 11 | RO | Transmit Fault 0 _B No fault condition on transmit path 1 _B Fault condition on transmit path |
| RX_FAULT | 10 | RO | Receive Fault 0 _B No fault condition on receive path 1 _B Fault condition on receive path |
| R100GBASE_R_CAPABLE | 5 | RO | 100GBASE-R Capable 0 _B PCS is not able to support 100GBASE-R PCS type. 1 _B PCS is able to support 100GBASE-R PCS type. |
| R40GBASE_R_CAPABLE | 4 | RO | 40GBASE-R Capable 0 _B PCS is not able to support 40GBASE-R PCS type. 1 _B PCS is able to support 40GBASE-R PCS type. |
| R10GBASE_T_CAPABLE | 3 | RO | 10GBASE-T Capable 0 _B PCS is not able to support 10GBASE-T PCS type. 1 _B PCS is able to support 10GBASE-T PCS type. |
| R10GBASE_W_CAPABLE | 2 | RO | 10GBASE-W Capable 0 _B PCS is not able to support 10GBASE-W PCS type. 1 _B PCS is able to support 10GBASE-W PCS type. |
| R10GBASE_X_CAPABLE | 1 | RO | 10GBASE-X Capable 0 _B PCS is not able to support 10GBASE-X PCS type. 1 _B PCS is able to support 10GBASE-X PCS type. |
| R10GBASE_R_CAPABLE | 0 | RO | 10GBASE-R Capable 0 _B PCS is not able to support 10GBASE-R PCS types. 1 _B PCS is able to support 10GBASE-R PCS types. |

PCS Package Identifier 1 (Register 3.14)

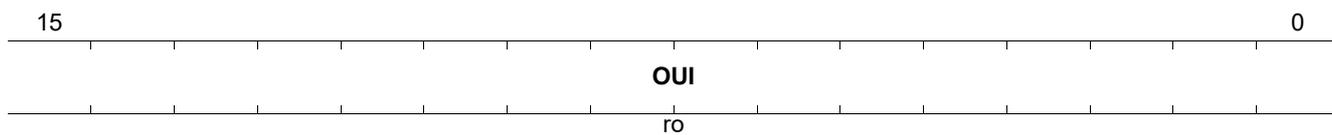
IEEE Standard Register=3.14

PCS_PACKID1

Reset Value

PCS Package Identifier 1 (Register 3.14)

C133_H



| Field | Bits | Type | Description |
|-------|------|------|--|
| OUI | 15:0 | RO | Organizationally Unique Identifier Bits 3:18 |

PCS Package Identifier 2 (Register 3.15)

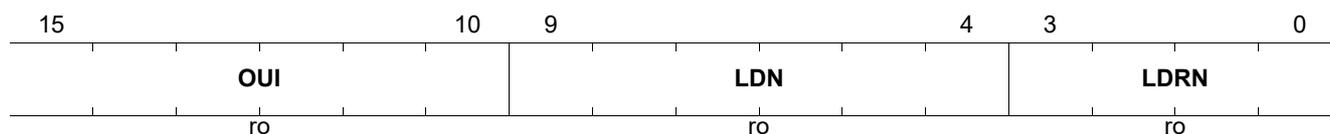
IEEE Standard Register=3.15

PCS_PACKID2

PCS Package Identifier 2 (Register 3.15)

Reset Value

5400_H



| Field | Bits | Type | Description |
|-------|-------|------|---|
| OUI | 15:10 | RO | Organizationally Unique Identifier Bits 19:24 |
| LDN | 9:4 | RO | Device Number Specifies the device number ¹⁾ to distinguish between several different products. |
| LDRN | 3:0 | RO | Device Revision Number Specifies the device revision number to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the [Product Ordering Information](#) chapter.

EEE Control and Capability 2 (Register 3.21)

Read only. Write from the STA has no effect.

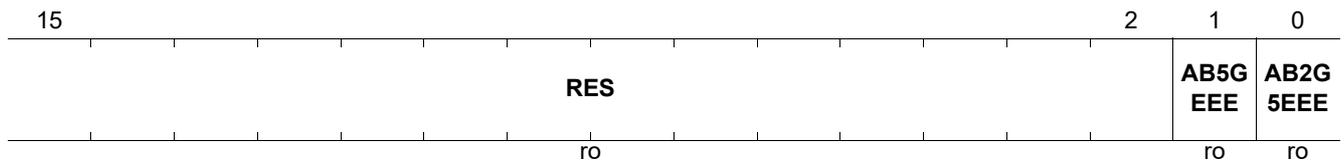
IEEE Standard Register=3.21

PCS_EEE_CAP2

Reset Value

EEE Control and Capability 2 (Register 3.21)

0001_H



| Field | Bits | Type | Description |
|----------|------|------|---|
| RES | 15:2 | RO | Reserved Value always 0. |
| AB5GEEE | 1 | RO | EEE Supported for 5GBASE-T 0 _B UNABLE EEE is not supported for 5GBASE-T. 1 _B ABLE EEE is supported for 5GBASE-T. |
| AB2G5EEE | 0 | RO | EEE Supported for 2.5GBASE-T 0 _B UNABLE EEE is not supported for 2.5GBASE-T. 1 _B ABLE EEE is supported for 2.5GBASE-T. |

PCS EEE Status Register 1 (Register 3.22)

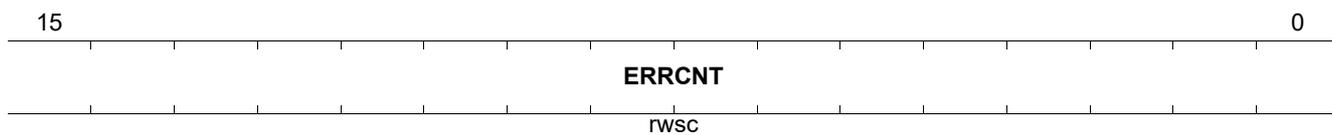
IEEE Standard Register=3.22

PCS_EEE_WAKERR

PCS EEE Status Register 1 (Register 3.22)

Reset Value

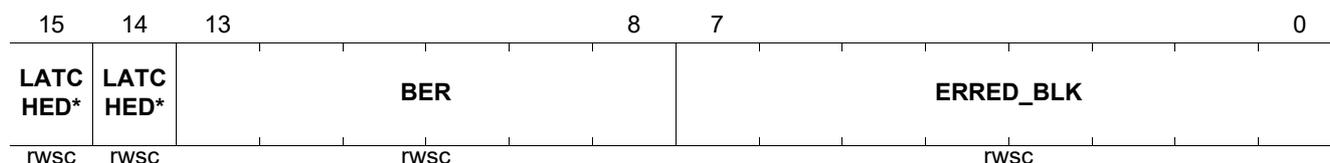
0000_H



| Field | Bits | Type | Description |
|--------|------|------|---|
| ERRCNT | 15:0 | RWSC | <p>EEE Wake Error Counter</p> <p>This is a 16-bit saturating counter indicating the number of times the GPHY PHY fails to wake up within the EEE time. This counter is cleared upon read from the STA.</p> |

MULTIGBASE-T PCS Status 2 (Register 3.33)

PCS_2G5_STAT2 Reset Value
MULTIGBASE-T PCS Status 2 (Register 3.33) 0000_H



| Field | Bits | Type | Description |
|--------------------|------|------|---|
| LATCHED_BLOCK_LOCK | 15 | RWSC | Latched Block Lock 0 _B PCS 2G5 does not have block lock. 1 _B PCS 2G5 has block lock. |
| LATCHED_HIGH_BER | 14 | RWSC | Latched High BER 0 _B PCS 2G5 did not report a high BER. 1 _B PCS 2G5 reported a high BER. |
| BER | 13:8 | RWSC | BER BER counter |
| ERRORED_BLOCKS | 7:0 | RWSC | Errored Blocks Errored blocks counter |

PCS TimeSync Capability Register (Register 3.1800)

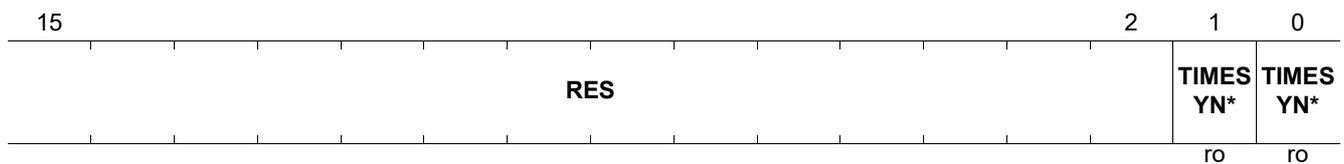
IEEE Standard Register=3.1800

PCS_TIMESYNC_CAP

PCS TimeSync Capability Register (Register 3.1800)

Reset Value

0000_H



| Field | Bits | Type | Description |
|-----------------------------|------|------|---|
| TIMESYNC_TX_PATH_DATA_DELAY | 1 | RO | <p>TimeSync Transmit Path Data Delay</p> <p>0_B PCS does not provide information on transmit path data delay. For the GPHY, the value is always 0.</p> <p>1_B PCS provides information on transmit path data delay in registers 3.1801 through 3.1804.</p> |
| TIMESYNC_RX_PATH_DATA_DELAY | 0 | RO | <p>TimeSync Receive Path Data Delay</p> <p>0_B PCS does not provide information on receive path data delay. For the GPHY, the value is always 0.</p> <p>1_B PCS provides information on receive path data delay in registers 3.1805 through 3.1808.</p> |

6.3 Standard Auto-Negotiation Registers for MMD=0x07

This register file contains the auto-negotiation registers for MMD device 0x07.

Table 32 Registers Overview- Standard Auto-Negotiation Registers

| Register Short Name | Register Long Name | Reset Value |
|------------------------------------|---|---------------------------------|
| ANEG_CTRL | Auto-Negotiation Control (Register 7.0) | 3000 _H |
| ANEG_STAT | Auto-Negotiation Status (Register 7.1) | 0008 _H |
| ANEG_DEVID1 | PHY Identifier 1 (Register 7.2) | C133 _H |
| ANEG_DEVID2 | PHY Identifier 2 (Register 7.3) | 5400 _H ¹⁾ |
| ANEG_DIP1 | Device in Package 1 (Register 7.5) | 008B _H |
| ANEG_DIP2 | Device in Package 2 (Register 7.6) | C000 _H |
| ANEG_PACKID1 | AN Package Identifier (Register 7.14) | C133 _H |
| ANEG_PACKID2 | AN Package Identifier (Register 7.15) | 5400 _H ¹⁾ |
| ANEG_ADV | ANEG Adv. for GPHY (Register 7.16) | 9DE1 _H |
| ANEG_LP_BP_AB | AN Link Partner Base Page Ability (Register 7.19) | 0DE0 _H |
| ANEG_XNP_TX1 | ANEG Local Dev XNP TX1 (Register 7.22) | 0001 _H |
| ANEG_XNP_TX2 | ANEG Local Dev XNP TX2 (Register 7.23) | 0000 _H |
| ANEG_XNP_TX3 | ANEG Local Dev XNP TX3 (Register 7.24) | 0000 _H |
| ANEG_LP_XNP_AB1 | ANEG Link Partner XNP RX (Register 7.25) | 0000 _H |
| ANEG_LP_XNP_AB2 | ANEG Link Partner XNP RX (Register 7.26) | 0000 _H |
| ANEG_LP_XNP_AB3 | ANEG Link Partner XNP RX (Register 7.27) | 0000 _H |
| ANEG_MGBT_AN_CTRL | MULTI GBT AN Control (Register 7.32) | 0082 _H |
| ANEG_MGBT_AN_STA | MultiGBASE-T AN Status (Register 7.33) | 0000 _H |
| ANEG_EEE_AN_ADV1 | EEE Advertisement 1 (Register 7.60) | 0006 _H |
| ANEG_EEE_AN_LPAB1 | EEE Link Partner Ability 1 (Register 7.61) | 0000 _H |
| ANEG_EEE_AN_ADV2 | EEE Advertisement 2 (Register 7.62) | 0001 _H |
| ANEG_EEE_LP_AB2 | EEE Link Partner Ability 2 (Register 7.63) | 0001 _H |
| ANEG_MGBT_AN_CTRL2 | MGBT ANEG Control 2 (Register 7.64) | 0008 _H |

1) For the device specific reset value, see the Product and Package Naming table in the [Product Ordering Information](#) chapter.

6.3.1 ANEG Register Descriptions

This section describes all the ANEG registers in detail.

Auto-Negotiation Control (Register 7.0)

The register controls the main function of auto-negotiation as defined in Clause 45. Refer to IEEE 802.3 45.2.7.1. This register mirrors register STD_CTRL from Clause 22.

IEEE Standard Register=7.0

ANEG_CTRL

Reset Value

Auto-Negotiation Control (Register 7.0)

3000_H

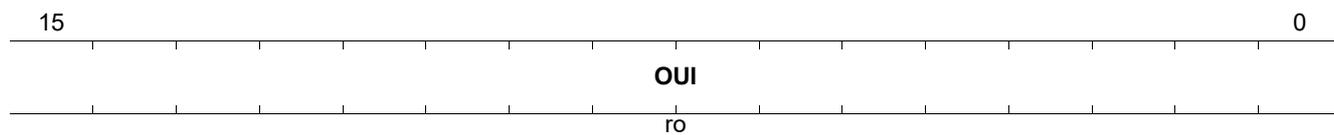
| | | | | | | | | | | | | |
|------------|-------------|------------|-----------------|-------------|----|-----------------|-------------|--|--|--|--|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | | | | 0 |
| RST | RES3 | XNP | ANEG_EN* | RES2 | | ANEG_RE* | RES1 | | | | | |
| RW | RO | RW | RW | RO | | RW | RO | | | | | |

| Field | Bits | Type | Description |
|--------------|-------|------|---|
| RST | 15 | RW | Reset This bit resets the entire PHY to its default state. Active links are terminated. This is a self-clearing bit. The GPHY firmware sets the bit to 0 via the hardware when the reset is completed. 0 _B NORMAL Normal GPHY operation 1 _B RESET GPHY reset |
| RES3 | 14 | RO | Reserved Value always 0, writes ignored. |
| XNP | 13 | RW | Extended Next Page Control 0 _B ZERO Extended next page is disabled. 1 _B ONE Extended next page is enabled. |
| ANEG_ENAB | 12 | RW | Auto-Negotiation Enable This bit enables the ANEG process to determine the link configuration. Bit 7.0.12 is a copy of bit 0.12 in register 0 (STD_CTRL). 0 _B ZERO ANEG process is disabled. 1 _B ONE ANEG process is enabled. |
| RES2 | 11:10 | RO | Reserved Value always zero, writes ignored. |
| ANEG_RESTART | 9 | RW | Restart Auto-Negotiation The ANEG process is restarted by setting bit 7.0.9 to 1. Bit 7.0.9 is a mirror of bit 0.9 in register 0 (STD_CTRL). Completion of ANEG is indicated in bit 0.1.5 and 7.1.5. 0 _B ZERO Normal operation 1 _B RESTART Restarts ANEG process. |
| RES1 | 8:0 | RO | Reserved Value always 0, writes ignored. |

| Field | Bits | Type | Description (cont'd) |
|--------------|------|------|---|
| ANEG_RF | 4 | ROSC | Remote Fault When read as 1, bit 7.1.4 indicates that a remote fault condition was detected. Bit 7.1.4 is a copy of bit 1.4 in register 1, device 0. 0 _B NORMAL No remote fault condition detected 1 _B FAULT Remote fault condition detected |
| ANEG_ABLE | 3 | RO | Auto-Negotiation Ability Bit 7.1.3 is a copy of bit 1.3 in register 1. This is the ANEG ability of the GPHY. 0 _B UNABLE PHY is not able to perform ANEG. 1 _B ABLE PHY is able to perform ANEG. |
| LINKSTA | 2 | RO | Link Status When read as 1 _B , bit 7.1.2 indicates that the PMA/PMD determined that a valid link is established. This bit is a duplicate of the PMA/PMD link status bit in 1.1.2. This bit latches low so it does not represent the current status, but is used to indicate link drop since the last read from the management interface. Reading this bit from the MDIO resets the bit to the current value of the link. 0 _B DOWN Link is down. 1 _B UP Link is up. |
| RES1 | 1 | RO | Reserved Value always 0, write ignored. |
| LP_ANEG_ABLE | 0 | RO | Link Partner Auto-Negotiation Ability 0 _B UNABLE Link partner is not capable of ANEG. 1 _B ABLE Link partner is capable of ANEG. |

PHY Identifier 1 (Register 7.2)

ANEG_DEVID1 **Reset Value**
PHY Identifier 1 (Register 7.2) **C133_H**



| Field | Bits | Type | Description |
|-------|------|------|------------------------------------|
| OUI | 15:0 | RO | Organizationally Unique Identifier |

PHY Identifier 2 (Register 7.3)

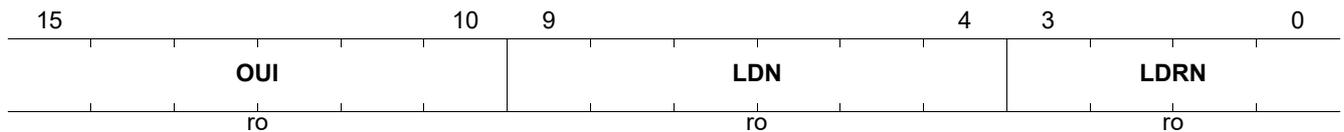
Organizationally Unique Identifier
IEEE Standard Register=7.3

ANEG_DEVID2

PHY Identifier 2 (Register 7.3)

Reset Value

5400_H



| Field | Bits | Type | Description |
|-------|-------|------|---|
| OUI | 15:10 | RO | Organizationally Unique Identifier |
| LDN | 9:4 | RO | Device Number Specifies the device number ¹⁾ to distinguish between several different products. |
| LDRN | 3:0 | RO | Device Revision Number Specifies the device revision number ¹⁾ to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the [Product Ordering Information](#) chapter.

| Field | Bits | Type | Description (cont'd) |
|--------|------|------|--|
| PMAPMD | 1 | RO | PMA PMD Present in Package |
| | | | 0 _B ABSENT PMA PMD registers not present in package |
| | | | 1 _B PRESENT PMA PMD registers present in package |
| CL22 | 0 | RO | Clause 22 Register Present in Package |
| | | | 0 _B ABSENT Clause 22 registers no present in package |
| | | | 1 _B PRESENT Clause 22 registers present in package |

Device in Package 2 (Register 7.6)

IEEE Standard Register=7.6

ANEG_DIP2

Reset Value

Device in Package 2 (Register 7.6)

C000_H

| | | | | | | | | | | | |
|--------------------|--------------------|---------------------|------------|--|--|--|--|--|--|--|---|
| 15 | 14 | 13 | 12 | | | | | | | | 0 |
| VSPE C2 | VSPE C1 | CL22E XT | RES | | | | | | | | |
| ro | ro | ro | ro | | | | | | | | |

| Field | Bits | Type | Description |
|---------|------|------|---|
| VSPEC2 | 15 | RO | Vendor Specific Device 2 Present in Package 0 _B ABSENT Vendor Specific Device 2 not present in package 1 _B PRESENT Vendor Specific Device 2 present in package |
| VSPEC1 | 14 | RO | Vendor Specific Device 1 Present in Package 0 _B ABSENT Vendor Specific Device 1 not present in package 1 _B PRESENT Vendor Specific Device 1 present in package |
| CL22EXT | 13 | RO | Clause 22 Extension Present in Package 0 _B ABSENT Clause 22 extension not present in package 1 _B PRESENT Clause 22 extension present in package |
| RES | 12:0 | RO | Reserved Ignore on read. |

AN Package Identifier (Register 7.14)

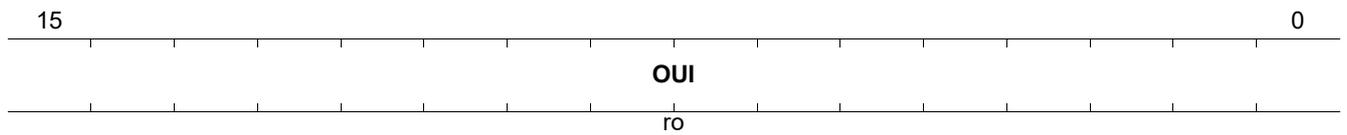
IEEE Standard Register=7.14

ANEG_PACKID1

Reset Value

AN Package Identifier (Register 7.14)

C133_H



| Field | Bits | Type | Description |
|-------|------|------|--|
| OUI | 15:0 | RO | Organizationally Unique Identifier Bits 3:18 |

AN Package Identifier (Register 7.15)

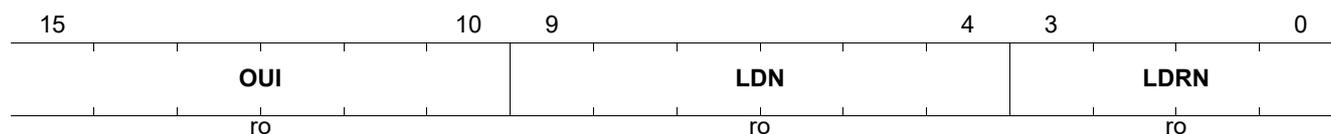
IEEE Standard Register=7.15

ANEG_PACKID2

AN Package Identifier (Register 7.15)

Reset Value

5400_H



| Field | Bits | Type | Description |
|-------|-------|------|---|
| OUI | 15:10 | RO | Organizationally Unique Identifier Bits 19:24 |
| LDN | 9:4 | RO | Device Number Specifies the device number ¹⁾ to distinguish between several different products. |
| LDRN | 3:0 | RO | Device Revision Number Specifies the device revision number ¹⁾ to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the [Product Ordering Information](#) chapter.

ANEG Adv. for GPHY (Register 7.16)

This register is a copy of the ANEG advertisement register (Register 4). A read to the AN advertisement register (7.16) reports the value of the ANEG advertisement register (Register 4). Writes to the AN advertisement register (7.16) cause a write to occur to the ANEG advertisement register (Register 4).

IEEE Standard Register=7.16

ANEG_ADV
Reset Value
ANEG Adv. for GPHY (Register 7.16)
9DE1_H

| | | | | | | | | | | |
|-----------|------------|-----------|------------|------------|--|--|---|-----------|--|---|
| 15 | 14 | 13 | 12 | 11 | | | 5 | 4 | | 0 |
| NP | RES | RF | XNP | TAF | | | | SF | | |
| RW | RO | RW | RW | RW | | | | RW | | |

| Field | Bits | Type | Description |
|-------|------|------|--|
| NP | 15 | RW | Next Page Able 0 _B INACTIVE No next page allowed. 1 _B ACTIVE Additional next page(s) to follow. |
| RES | 14 | RO | Reserved Write as zero, ignore on read. |
| RF | 13 | RW | Remote Fault The remote fault bit allows indication of a fault to the link partner. Refer to IEEE 802.3 28.2.1.2.4. |
| XNP | 12 | RW | Transmission of Extended Next Pages Indicates that the GPHY is able to transmit extended next pages. 0 _B UNABLE GPHY is XNP unable. 1 _B ABLE GPHY is XNP able. |
| TAF | 11:5 | RW | Technology Ability Field The technology ability field is an 8-bit wide field containing information indicating supported technologies. The GPHY supports 10BASE-T (half- and full-duplex), 100BASE-TX (half- and full-duplex), and both symmetric and asymmetric PAUSE. 40 _H PS_ASYM Advertises asymmetric pause 20 _H PS_SYM Advertises symmetric pause 10 _H DBT4 Advertises 100BASE-T4 08 _H DBT_FDX Advertises 100BASE-TX full-duplex 04 _H DBT_HDX Advertises 100BASE-TX half-duplex 02 _H XBT_FDX Advertises 10BASE-T full-duplex 01 _H XBT_HDX Advertises 10BASE-T half-duplex |
| SF | 4:0 | RW | Selector Field This field is always set to 00001 _B because the GPHY only supports the 802.3 Ethernet standard. 00001 _B IEEE8023 IEEE 802.3 technology. |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|---|
| SF | 4:0 | RO | <p>Link Partner Selector Field</p> <p>This selector field represents one of the 32 possible messages with encoding definitions defined in IEEE 802.3 Annex 28A.</p> <p>00_H Reserved</p> <p>01_H IEEE 802.3</p> <p>02_H IEEE 802.9 ISLAN-16T</p> <p>03_H IEEE 802.5</p> <p>04_H IEEE 1394</p> <p>05_H Reserved</p> <p>...</p> <p>1F_H Reserved</p> |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|---|
| MCF | 10:0 | RW | <p>Message Code Field</p> <p>When the Message Page bit is set to 1_B (7.16.1), this field is the Message Code Field of a message page used in a next page exchange. The message codes are described in IEEE 802.3 Appendix 28C. This is used to indicate the type of message in UCF1 and UCF2.</p> <p>00_H Reserved 01_H Null message 02_H One Unformatted Page (UP) with TAF follows 03_H Two UPs with TAF follows 04_H Remote fault details message 05_H OUI message 06_H PHY ID message 07_H 100BASE-T2 message 08_H 1000BASE-T message 09_H MULTIGBASE-T message 0A_H EEE technology capability follows in next UP 0B_H OUI XNP</p> |

ANEG Local Dev XNP TX2 (Register 7.23)

Unformatted code field 1 contains seed information and advertises support of 1 GBT full-duplex and half-duplex. Refer to 28.2.3.4.

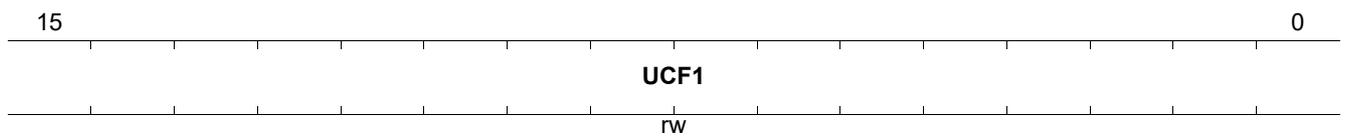
IEEE Standard Register=7.23

ANEG_XNP_TX2

Reset Value

ANEG Local Dev XNP TX2 (Register 7.23)

0000_H



| Field | Bits | Type | Description |
|-------|------|------|---|
| UCF1 | 15:0 | RW | Unformatted Code Field 1 Transmits the master-slave seed bit to facilitate ANEG resolution, port type, and duplex capability. |

ANEG Local Dev XNP TX3 (Register 7.24)

Unformatted code field 2 - Register 7.24

Refer to 28.2.3.4.

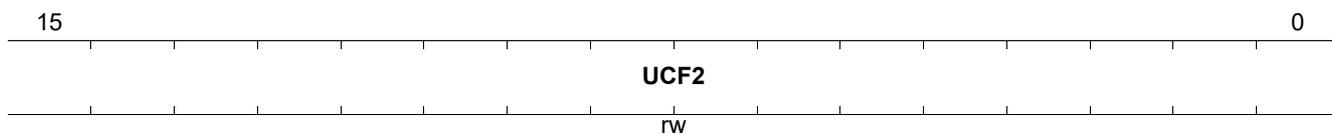
IEEE Standard Register=7.24

ANEG_XNP_TX3

Reset Value

ANEG Local Dev XNP TX3 (Register 7.24)

0000_H



| Field | Bits | Type | Description |
|-------|------|------|--|
| UCF2 | 15:0 | RW | Unformatted Code Field 2 2.5 GBASE-T ability is advertised by default. |

ANEG Link Partner XNP RX (Register 7.25)

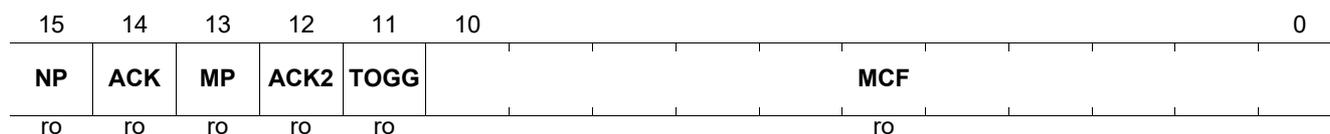
IEEE Standard Register=7.25

ANEG_LP_XNP_AB1

ANEG Link Partner XNP RX (Register 7.25)

Reset Value

0000_H



| Field | Bits | Type | Description |
|-------|------|------|--|
| NP | 15 | RO | Link Partner Next Page Refer to 28.2.3.4.3. The NP bit is used by the next page function to indicate whether or not this is the last next page to be transmitted. 0 _B INACTIVE Last page 1 _B ACTIVE Additional next page(s) to follow |
| ACK | 14 | RO | Link Partner Acknowledge As defined in 28.2.1.2.5. The Acknowledge (Ack) bit is used by the ANEG function to indicate that the GPHY successfully received its link partner's link codeword. |
| MP | 13 | RO | Link Partner Message Page Indicates that the content of MCF is either an unformatted page or a formatted message. 0 _B UNFOR Unformatted page 1 _B MESSG Message page |
| ACK2 | 12 | RO | Link Partner Acknowledge 2 0 _B INACTIVE Device is unable to comply with message. 1 _B ACTIVE Device complies with message. |
| TOGG | 11 | RO | Link Partner Toggle This bit is set to the opposite of the TOGG bit in the previous page. 0 _B ZERO Previous value of the TX LCW was 1 _B . 1 _B ONE Previous value of the TX LCW was 0 _B . |
| MCF | 10:0 | RO | Link Partner Message Code Field This field indicates the type of Message Code. 009 _H MC_2G5BT Message code for 2.5GBASE-T |

ANEG Link Partner XNP RX (Register 7.26)

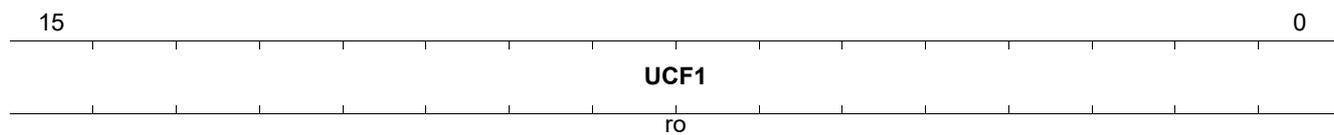
IEEE Standard Register=7.26

ANEG_LP_XNP_AB2

ANEG Link Partner XNP RX (Register 7.26)

Reset Value

0000_H



| Field | Bits | Type | Description |
|-------|------|------|---|
| UCF1 | 15:0 | RO | Unformatted Code Field 1 Refer to 28.2.3.4. |

ANEG Link Partner XNP RX (Register 7.27)

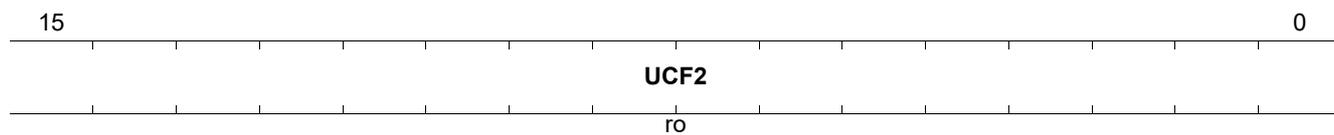
IEEE Standard Register=7.27

ANEG_LP_XNP_AB3

ANEG Link Partner XNP RX (Register 7.27)

Reset Value

0000_H



| Field | Bits | Type | Description |
|-------|------|------|---|
| UCF2 | 15:0 | RO | Unformatted Code Field 2 Refer to 28.2.3.4. |

MULTI GBT AN Control Register (Register 7.32)

This register advertises the GPHY capabilities.

IEEE Standard Register=7.32

ANEG_MGBT_AN_CTRL
Reset Value
MULTI GBT AN Control Register (Register 7.32)
0082_H

| | | | | | | | | | | | | | | | |
|----------------------|-------------|-----------|----------------------|----|-------------|---|---------------------|----------------------|---------------------|----------------------|---|-------------|-------------------|-----------|------------|
| 15 | 14 | 13 | 12 | 11 | | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MS_M AN_* | MSCV | PT | AB_10 GBT | | RES2 | | AB_5 GBT | AB_2 G5BT | FR_5G BT | FR_2G 5BT | | RES1 | LDPM A | FR | LDL |
| rw | rw | rw | ro | | ro | | ro | rw | ro | rw | | ro | rw | rw | rw |

| Field | Bits | Type | Description |
|-----------|------|------|--|
| MS_MAN_EN | 15 | RW | Master Slave Manual Config Enable 0 _B ANEG ANEG is used to determine the master-slave selection. 1 _B MAN Manual configuration. The MSCV bit determines the master-slave selection. |
| MSCV | 14 | RW | Master Slave Config Value 0 _B SLAVE Manual set to SLAVE 1 _B MASTER Manual set to MASTER |
| PT | 13 | RW | Port Type 0 _B MASTER Preference as Master - single port device 1 _B SLAVE Preference as Slave - multi-port device |
| AB_10GBT | 12 | RO | 10GBASE-T Ability Not supported. Value always 0. |
| RES2 | 11:9 | RO | Reserved Value always 0, writes ignored. |
| AB_5GBT | 8 | RO | 5GBASE-T Ability Not supported by the GPHY. 0 _B UNABLE Do not advertise PHY as 5GBASE-T capable. 1 _B ABLE Advertises PHY as 5GBASE-T capable. Not supported. |
| AB_2G5BT | 7 | RW | 2.5GBASE-T Ability 0 _B UNABLE Do not advertise PHY as 2.5GBASE-T capable. 1 _B ABLE Advertises PHY as 2.5GBASE-T capable. |
| FR_5GBT | 6 | RO | 5GBASE-T Fast Retrain Ability Not supported by GPHY. 0 _B UNABLE Do not advertise PHY as 5GBASE-T fast retrain able. 1 _B ABLE Advertises PHY as 5GBASE-T fast retrain capable. Not supported. |
| FR_2G5BT | 5 | RW | 2.5GBASE-T Fast Retrain Ability 0 _B UNABLE Do not advertise PHY as 2.5G fast retrain able. 1 _B ABLE Advertises PHY as 2.5G fast retrain able. |
| RES1 | 4:3 | RO | Reserved Value always 0, writes ignored. |

| Field | Bits | Type | Description (cont'd) |
|-------|------|------|--|
| LDPMA | 2 | RW | <p>GPHY PMA Training Reset Request</p> <p>When this bit is set to 1_B, the GPHY expects the link partner to reset the PMA training PRBS for every PMA training frame.</p> <p>When this bit is set to 0_B, the GPHY expects the link partner to run the PMA training PRBS continuously through every PMA training frame.</p> |
| FR | 1 | RW | Fast Retrain Ability |
| LDL | 0 | RW | GPHY Loop Timing Ability |

EEE Link Partner Ability 1 (Register 7.61)

After the AN process is completed, this register reflects the contents of the link partner's EEE advertisement register. The definitions are the same as for the EEE AN advertisement 1 register.

IEEE Standard Register=7.61

All of the bits in the EEE LP ability 1 register are read only. A write operation to the EEE LP advertisement register has no effect.

ANEG_EEE_AN_LPAB1

Reset Value

EEE Link Partner Ability 1 (Register 7.61)

0000_H

| | | | | | | | | | | | | |
|-----|---|---|---|---|---|--------------|--------------|--------------|--------------|--------------|--------------|-----|
| 15 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | |
| RES | | | | | | EEE_1 0G* | EEE_1 0G* | EEE_1 00* | EEE_1 0G* | EEE_1 00* | EEE_1 00* | RES |
| | | | | | | ro | ro | ro | ro | ro | ro | |

| Field | Bits | Type | Description |
|-----------------|------|------|---|
| EEE_10GBKR | 6 | RO | Support of 10GBASE-KR EEE 0 _B DISABLED This PHY mode is not supported for EEE. 1 _B ENABLE This PHY mode is supported for EEE. |
| EEE_10GBKX 4 | 5 | RO | Support of 10GBASE-KX4 EEE 0 _B DISABLED This PHY mode is not supported for EEE. 1 _B ENABLE This PHY mode is supported for EEE. |
| EEE_1000BKX | 4 | RO | Support of 1000BASE-KX EEE 0 _B DISABLED This PHY mode is not supported for EEE. 1 _B ENABLE This PHY mode is supported for EEE. |
| EEE_10GBT | 3 | RO | Support of 10GBASE-T EEE 0 _B DISABLED This PHY mode is not supported for EEE. 1 _B ENABLE This PHY mode is supported for EEE. |
| EEE_1000BT | 2 | RO | Support of 1000BASE-T EEE 0 _B DISABLED This PHY mode is not supported for EEE. 1 _B ENABLE This PHY mode is supported for EEE. |
| EEE_100BTX | 1 | RO | Support of 100BASE-TX EEE 0 _B DISABLED This PHY mode is not supported for EEE. 1 _B ENABLE This PHY mode is supported for EEE. |

EEE Advertisement 2 (Register 7.62)

EEE advertisement 2 register is a continuation of EEE advertisement 1 register.

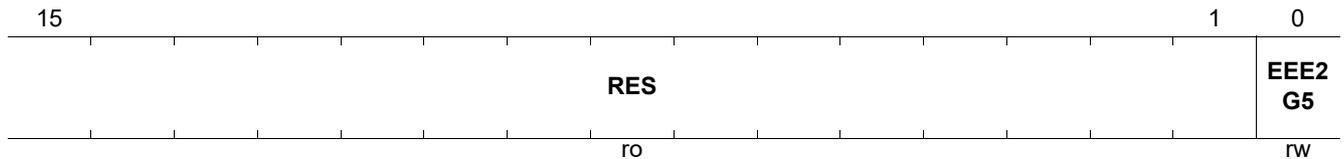
IEEE Standard Register=7.62

ANEG_EEE_AN_ADV2

Reset Value

EEE Advertisement 2 (Register 7.62)

0001_H



| Field | Bits | Type | Description |
|--------|------|------|--|
| RES | 15:1 | RO | Reserved |
| EEE2G5 | 0 | RW | Advertise 2.5GBASE-T EEE Capability 0 _B DISABLED This PHY mode does not advertise 2.5GBASE-T EEE. 1 _B ENABLE This PHY mode advertises 2.5GBASE-T EEE. |

6.4 Vendor Specific 1 Device Registers

This register file contains GPHY-specific registers for MMD=30 (decimal).

Table 33 Registers Overview- Vendor Specific 1 Device Registers

| Register Short Name | Register Long Name | Reset Value |
|---|---|-------------------|
| VSPEC1_LED0 | Configuration for LED Pin 0 (Register 30.1) | 0310 _H |
| VSPEC1_LED1 | Configuration for LED Pin 1 (Register 30.2) | 0320 _H |
| VSPEC1_TXS_SCL_OFFSET | PHY Transmit Amplitude Control Register (Register 30.8) | 0000 _H |
| VSPEC1_NBT_DS_CTRL | NBASE-T Downshift Control Register (Register 30.10) | 0400 _H |
| VSPEC1_NBT_DS_STA | NBASE-T Downshift Status Register (Register 30.11) | 0000 _H |
| VSPEC1_PM_CTRL | Packet Manager Control (Register 30.12) | 3000 _H |
| VSPEC1_TEMP_STA | Temperature Code (Register 30.14) | 0000 _H |
| VSPEC1_IMASK | VSPEC1 Interrupt Mask Register (Register 30.17) | 0000 _H |
| VSPEC1_ISTAT | VSPEC1 Interrupt Mask Register (Register 30.18) | 0000 _H |
| VSPEC1_LANE_ASP_MAP | ASP Mapping to Physical Lanes (Register 30.20) | 00E4 _H |
| VSPEC1_LOW_POWER_ENTRY_TIME | Time to Enter Low Power (Register 30.21) | 0001 _H |
| VSPEC1_FRCTL | Fast Retrain Control and Status (Register 30.22) | 0000 _H |

6.4.1 VSPEC1 Register Descriptions

This section describes all the VSPEC1 registers in detail.

Configuration for LED Pin 0 (Register 30.1)

This register configures the behavior of the LED0 pin depending on predefined states or events the PHY entered into or raised. Since more than one event/state may be active at the same time, more than one function may apply at the same time. The priority from highest to lowest is given by the order: PULSE, BLINKS, BLINKF, and CON. The LED PULSE for the selected activity is only displayed for the link speed selected in CON. When CON is selected as NONE, no PULSE is displayed on the LED for any activity. To avoid the LED being constantly on when it is configured for pulsing alone, set the NO_CON bit in the PULSE field (bit 11).

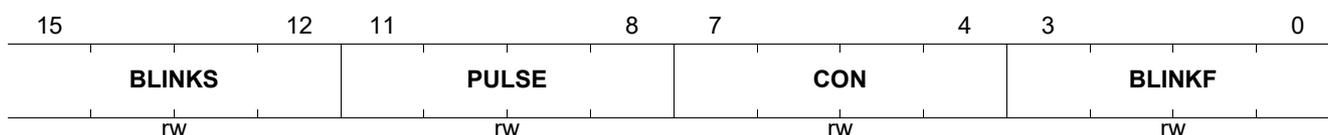
IEEE Standard Register=30.1

VSPEC1_LED0

Configuration for LED Pin 0 (Register 30.1)

Reset Value

0310_H



| Field | Bits | Type | Description |
|--------|-------|------|--|
| BLINKS | 15:12 | RW | <p>Slow Blinking Configuration</p> <p>The BLINKS field selects the PHY states where the LED blinks with the predefined slow frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.</p> <p>0000_BNONE Not active 0001_BLINK10 Blink when link is 10 Mbps. 0010_BLINK100 Blink when link is 100 Mbps. 0100_BLINK1000 Blink when link is 1000 Mbps. 1000_BLINK2500 Blink when link is 2500 Mbps.</p> |
| PULSE | 11:8 | RW | <p>Pulsing Configuration</p> <p>The PULSE field is a mask field that combines certain events, such as TXACT RXACT, to generate a pulse on the LED when such an event is detected.</p> <p>0000_BNONE No pulsing 0001_BTXACT Transmit activity 0010_BRXACT Receive activity 0100_BCOL Collision 1000_BNO_CON Constant on behavior is switched off.</p> |

| Field | Bits | Type | Description (cont'd) |
|--------|------|------|---|
| CON | 7:4 | RW | <p>Constant On Configuration</p> <p>The CON field selects the PHY states where the LED is constantly on. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.</p> <p>0000_BNONE Not active 0001_BLINK10 On when link is 10 Mbps. 0010_BLINK100 On when link is 100 Mbps. 0100_BLINK1000 On when link is 1000 Mbps. 1000_BLINK2500 On when link is 2500 Mbps.</p> |
| BLINKF | 3:0 | RW | <p>Fast Blinking Configuration</p> <p>The BLINKF field selects the PHY states where the LED blinks with the predefined fast frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.</p> <p>0000_BNONE No active 0001_BLINK10 Blink when Link is 10 Mbps. 0010_BLINK100 Blink when Link is 100 Mbps. 0100_BLINK1000 Blink when Link is 1000 Mbps. 1000_BLINK2500 Blink when Link is 2500 Mbps.</p> |

Configuration for LED Pin 1 (Register 30.2)

Configuration register for LED pin 1

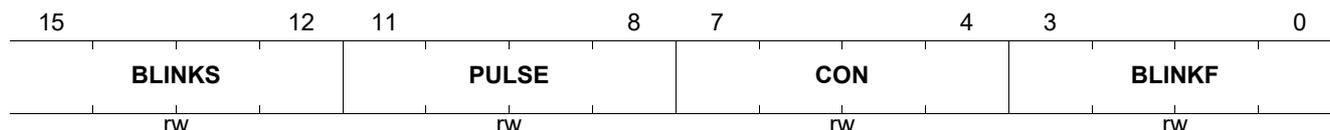
IEEE Standard Register=30.2

VSPEC1_LED1

Reset Value

Configuration for LED Pin 1 (Register 30.2)

0320_H



| Field | Bits | Type | Description |
|--------|-------|------|--|
| BLINKS | 15:12 | RW | <p>Slow Blinking Configuration</p> <p>The BLINKS field selects the PHY states where the LED blinks with the predefined slow frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.</p> <p>0000_BNONE Not active 0001_BLINK10 Blink when link is 10 Mbps. 0010_BLINK100 Blink when link is 100 Mbps. 0100_BLINK1000 Blink when link is 1000 Mbps. 1000_BLINK2500 Blink when link is 2500 Mbps.</p> |
| PULSE | 11:8 | RW | <p>Pulsing Configuration</p> <p>The PULSE field is a mask field that combines certain events, such as TXACT RXACT, to generate a pulse on the LED when such an event is detected.</p> <p>0000_BNONE No pulsing 0001_BTXACT Transmit activity 0010_BRXACT Receive activity 0100_BCOL Collision 1000_BNO_CON Constant on behavior is switched off.</p> |
| CON | 7:4 | RW | <p>Constant On Configuration</p> <p>The CON field selects the PHY states where the LED is constantly on. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.</p> <p>0000_BNONE Not active 0001_BLINK10 On when link is 10 Mbps. 0010_BLINK100 On when link is 100 Mbps. 0100_BLINK1000 On when link is 1000 Mbps. 1000_BLINK2500 On when link is 2500 Mbps.</p> |

| Field | Bits | Type | Description (cont'd) |
|--------|------|------|--|
| BLINKF | 3:0 | RW | <p>Fast Blinking Configuration</p> <p>The BLINKF field selects the PHY states where the LED blinks with the predefined fast frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.</p> <p>0000_BNONE Not active 0001_BLINK10 Blink when link is 10 Mbps. 0010_BLINK100 Blink when link is 100 Mbps. 0100_BLINK1000 Blink when link is 1000 Mbps. 1000_BLINK2500 Blink when link is 2500 Mbps.</p> |

PHY Transmit Amplitude Control Register (Register 30.8)

This register adjusts the transmit amplitude of the PHY.

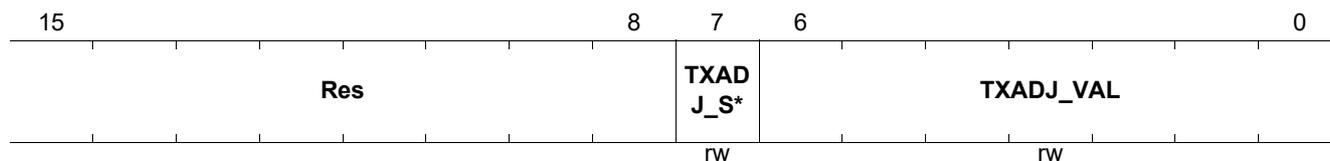
IEEE Standard Register=30.8

VSPEC1_TXS_SCL_OFFSET

Reset Value

PHY Transmit Amplitude Control Register (Register 30.8)

0000_H



| Field | Bits | Type | Description |
|-----------|------|------|---|
| TXADJ_SGN | 7 | RW | Transmit Amplitude Adjustment Sign 0 _B INC Increase transmit amplitude 1 _B DEC Decrease transmit amplitude |
| TXADJ_VAL | 6:0 | RW | Transmit Amplitude Adjustment Value Multiply the transmit amplitude by the following factor. (1 + (1-TXADJ_SGN*2)*TXADJ_VAL/128) The amplitude adjustment takes effect on the next link up. |

NBASE-T Downshift Control Register (Register 30.10)

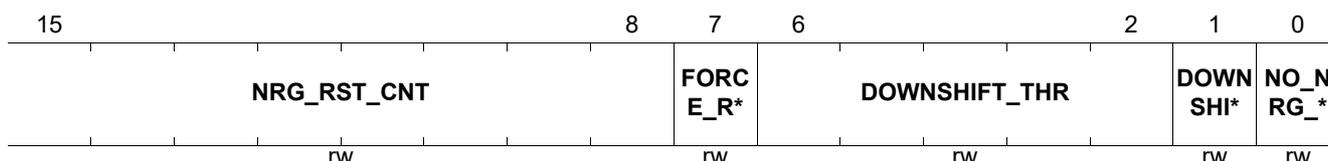
IEEE Standard Register=30.10

VSPEC1_NBT_DS_CTRL

NBASE-T Downshift Control Register (Register 30.10)

Reset Value

0400_H



| Field | Bits | Type | Description |
|---------------|------|------|---|
| NRG_RST_CNT | 15:8 | RW | Timer to Reset the Downshift Process When the energy is zero for a duration equal to NRG_RST_CNT seconds, the ANEG advertised capabilities are reset to the maximum GPHY capabilities. When NRG_RST_CNT is lower than 2, the ADS feature cannot be enabled. Default is 4 seconds. <i>Note: This timer only takes effect when NO_NRG_RST is set.</i> |
| FORCE_RST | 7 | RW | Force Reset of Downshift Process Setting this bit to 1 immediately resets the ANEG advertised capabilities to the maximum GPHY capabilities. |
| DOWNSHIFT_THR | 6:2 | RW | NBASE-T Downshift Training Counter Threshold dsh_thr variable in NBASE-T specification This is a 4-bit counter from 0 to 15 used to control the number of training cycles allowed for linkup, otherwise downshift. |
| DOWNSHIFT_EN | 1 | RW | NBASE-T Downshift Enable dsh_en variable in NBASE-T specification 0 _B DISABLE Disables NBT downshift. 1 _B ENABLE Enables NBT downshift. |
| NO_NRG_RST | 0 | RW | Advertise All Speeds if No Energy Detected When no energy is detected, this resets to advertise all speeds. Energy variable in NBASE-T specification 0 _B DISABLE Do not reset speeds advertised when no energy is detected. 1 _B ENABLE Reset speeds advertised when no energy is detected. |

Packet Manager Control (Register 30.12)

IEEE Standard Register=30.12

Control the Packet Manager Configuration

VSPEC1_PM_CTRL
Reset Value
Packet Manager Control (Register 30.12)
3000_H

| | | | | | | | | | | | | | | | |
|-----------------|----------------------|----|-----------------|------------|------------|---------------|------------|------------------|---|-----------------|-------------------|---------------|-----------|--------------|----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| USXGMII* | USXGMII_REACH | | MDINT_M* | RES | RES | PTP_EN | RES | SYNCE_CLK | | SYNCE_EN | PRE_EMP_EN | PCH_EN | SI | PM_EN | |
| rw | rw | | rw | | | | rw | rw | | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|----------------------|-------|------|--|
| USXGMII_FIX ED2G5 | 15 | RW | Force USXGMII Interface to Remain in 2.5G Speed or TPI Link Speed Irrespective of the TPI link speed, the USXGMII operates at 2.5G speed when this bit is enabled. The GPHY packet manager performs the rate adaptation, and flow control is used to backpressure the MAC SoC when required. 0 _B NO_FORCE The USXGMII speed is reconfigured by the GPHY based on the TPI link speed. 1 _B FORCE The USXGMII speed is forced to the 2.5G speed. |
| USXGMII_REACH | 14:12 | RW | USXGMII Tx and Rx Configuration Based on the loop length between the GPHY and STA connected through USXGMII interface. No action taken if USXGMII interface is not available. 000 _B SHORT Short reach configuration of USXGMII Tx and Rx equalization by firmware 001 _B MEDIUM Medium reach configuration of USXGMII Tx and Rx equalization by firmware 010 _B LONG Long reach configuration of USXGMII Tx and Rx equalization by firmware 011 _B CUSTOM Custom Configuration At start-up default settings available after boot. If custom configuration of USXGMII Tx and Rx equalization required then the parameters can be set with custom values using GPHY API Others: Reserved. |
| MDINT_MODE | 11 | RW | MDIO Interrupt Mode Sets the mode of the MDIO interrupt signal. 0 _B TRI Tristate mode The MDIO interrupt signal is tristate when the interrupt is inactive. It is driven only when the interrupt is active. 1 _B PP Push-pull mode The MDIO interrupt signal is constantly driven. |
| PTP_EN | 8 | rw | 1588 PTP Enable Enable 1588 PTP feature 0 _B DISABLE Disable 1 _B ENABLE Enable |

| Field | Bits | Type | Description |
|------------|------|------|---|
| SYNCE_CLK | 6:5 | RW | Configure the SyncE Clock Frequency Class MaxLinear recommends using the API to configure SyncE. 00 _B PSTN The SyncE clock frequency is PSTN class: 8 kHz. 01 _B EEC1 The SyncE clock frequency is EEC-1 class: 2.048 MHz. 10 _B EEC2 The SyncE clock frequency is EEC-2 class: 1.544 MHz. 11 _B RES Reserved |
| SYNCE_EN | 4 | RW | Enable SyncE Feature SyncE is disabled by default. MaxLinear recommends using the API to enable SyncE. 0 _B DISABLE Disable SyncE 1 _B ENABLE Enable SyncE |
| PRE_EMP_EN | 3 | RW | Enable pre-emption support Not applicable if PM_EN=1 0 _B DISABLE Disable 1 _B ENABLE Enable |
| PCH_EN | 2 | RW | Enable PCH Enable PCH preamble 0 _B DISABLE Disable 1 _B ENABLE Enable |
| SI | 1 | RW | Super Isolate Use in Super Isolate mode. Forces the device into a power down state by pin strapping (SLEEP) in which power consumption is the bare minimum required to still maintain the MII management interface communication. When activating the power down functionality, the PHY terminates active data links. The MII interface is also stopped in power down mode. See also IEEE 802.3-2008 22.2.4.1.5. The SI bit is only used to release the device from Super Isolate mode. Entering Super Isolate mode can only be activated by pin strapping at power up. 0 _B NORMAL Normal operational mode 1 _B SUPER_ISOLATE Super Isolate mode |
| PM_EN | 0 | RW | Enable Packet Manager This field enables LPI generation within the GPHY. The Packet Manager on the GPHY supports the Smart AZ features. This bit is only applicable for port 0, once this bit in port 0 is set, it will apply to all GPHY ports. Resetting this bit back from 1 to 0 is not supported. 0 _B DISABLE PM is bypassed, transparent mode 1 _B ENABLE SmartAZ mode |

Temperature Code (Register 30.14)

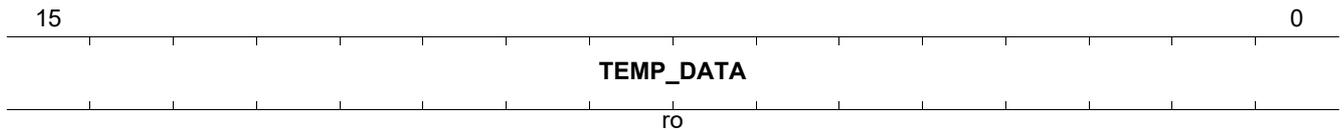
Junction temperature is presented in degrees Celsius
IEEE Standard Register=30.14

VSPEC1_TEMP_STA

Reset Value

Temperature Code (Register 30.14)

0000_H



| Field | Bits | Type | Description |
|-----------|------|------|---|
| TEMP_DATA | 15:0 | RO | <p>Junction Temperature</p> <p>The temperature is represented as a two's complement binary fixed point number, of which the 7 LSBs are fractional. The STA must take the thermal mitigation measures when the junction temperature exceeds the normal operating range if ADS is disabled.</p> <p>TEMP_DATA is invalid when the value is 0000_H.</p> <p>Example T_j Values (Decimal):</p> <ul style="list-style-type: none"> For T_j = -40 degC, TEMP_DATA = EC00_H For T_j = +125 degC, TEMP_DATA = 3E80_H |

VSPEC1 Interrupt Mask Register (Register 30.17)

This register defines the mask for the Interrupt Status Register (ISTAT), which contains the event source for the MDINT interrupt sent from the GPHY to an external chip. The mask is cleared whenever the corresponding interrupt is serviced.

The information about the interrupt source is indicated in the VSPEC1_ISTAT register.

IEEE Standard Register=30.17

VSPEC1_IMASK

Reset Value

VSPEC1 Interrupt Mask Register (Register 30.17)

0000_H

| | | | | | | | |
|-----|---|------|-----|-------------|-----|-----|--------------|
| 15 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RES | | CDET | RES | TS_FI FO | RES | RES | GMAC L_TS |
| | | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|----------|------|------|---|
| CDET | 5 | RW | Cable Detect Interrupt When active, MDINT is activated upon interrupt from detection of energy on the link. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |
| TS_FIFO | 3 | RW | Time Stamp FIFO Interrupt When active, MDINT is activated upon interrupt from either Tx or Rx Time stamp FIFO. 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |
| GMACL_TS | 0 | RW | Status of Interrupt Request GMACL TS When active, MDINT is activated upon GMACL time stamp valid interrupt 0 _B INACTIVE Interrupt is masked out. 1 _B ACTIVE Interrupt is activated. |

ASP Mapping to Physical Lanes (Register 30.20)

This register offers a programmable option to map physical lanes A, B, C, and D of the TPI to the ASPs. Each ASP must be mapped to each lane.

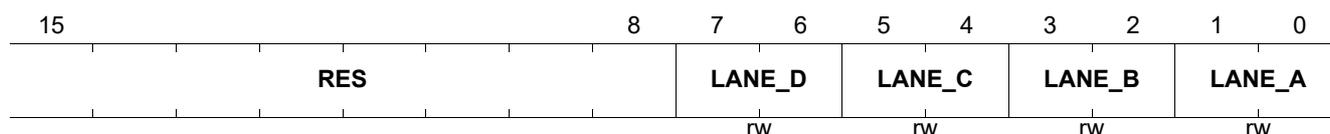
IEEE Standard Register=30.20

VSPEC1_LANE_ASP_MAP

Reset Value

ASP Mapping to Physical Lanes (Register 30.20)

00E4_H



| Field | Bits | Type | Description |
|--------|------|------|---|
| LANE_D | 7:6 | RW | Map Physical Lane-D to the ASP 00 _B ASPA Map Physical Lane-D to the ASP-A 01 _B ASPB Map Physical Lane-D to the ASP-B 10 _B ASPC Map Physical Lane-D to the ASP-C 11 _B ASPD Map Physical Lane-D to the ASP-D |
| LANE_C | 5:4 | RW | Map Physical Lane-C to the ASP 00 _B ASPA Map Physical Lane-C to the ASP-A 01 _B ASPB Map Physical Lane-C to the ASP-B 10 _B ASPC Map Physical Lane-C to the ASP-C 11 _B ASPD Map Physical Lane-C to the ASP-D |
| LANE_B | 3:2 | RW | Map Physical Lane-B to the ASP 00 _B ASPA Map Physical Lane-B to the ASP-A 01 _B ASPB Map Physical Lane-B to the ASP-B 10 _B ASPC Map Physical Lane-B to the ASP-C 11 _B ASPD Map Physical Lane-B to the ASP-D |
| LANE_A | 1:0 | RW | Map Physical Lane-A to the ASP 00 _B ASPA Map Physical Lane-A to the ASP-A 01 _B ASPB Map Physical Lane-A to the ASP-B 10 _B ASPC Map Physical Lane-A to the ASP-C 11 _B ASPD Map Physical Lane-A to the ASP-D |

Time to Enter Low Power (Register 30.21)

Programmable option to delay the time taken to enter low power mode.

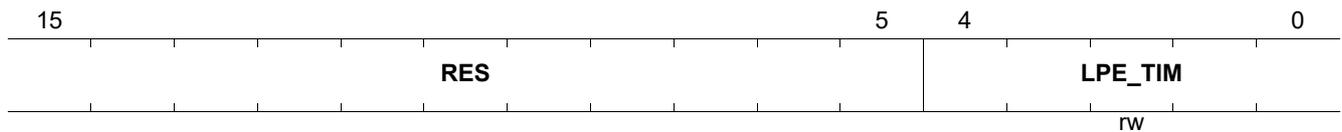
IEEE Standard Register=30.21

VSPEC1_LOW_POWER_ENTRY_TIME

Reset Value

Time to Enter Low Power (Register 30.21)

0001_H



| Field | Bits | Type | Description |
|---------|------|------|---|
| LPE_TIM | 4:0 | RW | Low Power Entry Time This is the time taken from detection of no activity on the line to the low power completion. The granularity is 4 seconds and adds 2.4 seconds to 5.6 seconds on to the initial time. |

Fast Retrain Control and Status (Register 30.22)

This register supports fast retrain (FR) as follows:

1. Configures the FR capability (IEEE, CISCO(THPBYP, TXDIS, EXT) [11]).
2. Records the link partner FR capability.
3. Reports the FW resolution of the FR capability.
4. Defines the maximum allowed number of times to try FR before performing a full link down.

IEEE Standard Register=30.22

VSPEC1_FRCTL

Fast Retrain Control and Status (Register 30.22)

Reset Value

0000_H

| | | | | | | | | | | | | | | | |
|----------|----------|----------|----------|----------|----------|---------|----------|----------|----------|--------|---------|----------|----------|----------|---------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MAX_FR_* | STAT_IE* | STAT_CI* | STAT_TH* | STAT_TX* | STAT_EXT | LP_IEEE | LP_CISCO | LP_THPB* | LP_TXDIS | LP_EXT | CAP_III | CAP_CIS* | CAP_THP* | CAP_TXD* | CAP_EXT |
| RW | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RW | RW | RW | RW | RW |

| Field | Bits | Type | Description |
|--------------|------|------|--|
| MAX_FR_RETRY | 15 | RW | Maximum Number of FR Retries Before Taking Linking Down 0 _B DISABLE Maximum number of retries limited to 4. 1 _B ENABLE Maximum number of retries limited to 8. |
| STAT_IEEE | 14 | RO | Resolved for IEEE FR 0 _B DISABLE Resolved to no IEEE FR. 1 _B ENABLE Resolved to IEEE FR. |
| STAT_CISCO | 13 | RO | Resolved for CISCO FR 0 _B DISABLE Resolved to no CISCO FR 1 _B ENABLE Resolved to CISCO FR |
| STAT_THPBYP | 12 | RO | Resolved Status THP BYP during COEF_EXCH for Either CISCO FR or IEEE FR 0 _B DISABLE Resolved that THP is not BYP for either CISCO FR or IEEE FR 1 _B ENABLE Resolved that THP is BYP during COEF EXCH for either CISCO FR or IEEE FR |
| STAT_TXDIS | 11 | RO | Resolved Status for CISCO FR with TX DISABLE 0 _B DISABLE Resolved that CISCO FR is not followed by TX DISABLE after link fail signaling 1 _B ENABLE Resolved that CISCO FR is followed by TX DISABLE after link fail signaling |
| STAT_EXT | 10 | RO | Resolved Status for CISCO Extended FR Timing 0 _B DISABLE Resolved for no CISCO FR with extended timing 1 _B ENABLE Resolved for CISCO FR with extended timing |
| LP_IEEE | 9 | RO | LP Request for IEEE FR 0 _B DISABLE No advertise for IEEE FR 1 _B ENABLE Advertise capable of doing IEEE FR |

| Field | Bits | Type | Description (cont'd) |
|------------|------|------|--|
| LP_CISCO | 8 | RO | LP Request for CISCO FR 0 _B DISABLE No advertise for CISCO FR 1 _B ENABLE Advertise capable of doing CISCO FR |
| LP_THPBYP | 7 | RO | LP Request for THP BYP During COEF_EXCH for Either CISCO FR or IEEE FR 0 _B DISABLE No request for THP BYP for either CISCO FR or IEEE FR 1 _B ENABLE Request for THP BYP during COEF EXCH for either CISCO FR or IEEE FR |
| LP_TXDIS | 6 | RO | LP Request for CISCO FR with TX DISABLE 0 _B DISABLE No request that CISCO FR is followed by TX DISABLE after link fail signaling 1 _B ENABLE Request that CISCO FR is followed by TX DISABLE after link fail signaling |
| LP_EXT | 5 | RO | LP Request for CISCO Extended FR Timing 0 _B DISABLE No request for CISCO FR with extended timing 1 _B ENABLE Request for CISCO FR with extended timing |
| CAP_IEEE | 4 | RW | Request for IEEE FR 0 _B DISABLE No advertise for IEEE FR 1 _B ENABLE Advertise capable of doing IEEE FR |
| CAP_CISCO | 3 | RW | Capable of Advertising CISCO FR 0 _B DISABLE No advertise for CISCO FR 1 _B ENABLE Advertise capable of doing CISCO FR |
| CAP_THPBYP | 2 | RW | Request LP for THP BYP during COEF_EXCH for Both CISCO FR and IEEE FR 0 _B DISABLE No request to LP for THP BYP for either CISCO FR or IEEE FR 1 _B ENABLE Request LP for THP BYP during COEF EXCH for either CISCO FR or IEEE FR |
| CAP_TXDIS | 1 | RW | Request for CISCO FR with TX DISABLE 0 _B DISABLE No request for CISCO FR with TX DISABLE after link fail signaling 1 _B ENABLE Advertise request that CISCO FR is followed by TX DISABLE after link fail signaling |
| CAP_EXT | 0 | RW | Request for CISCO Extended FR Timing 0 _B DISABLE No request for CISCO FR with extended timing 1 _B ENABLE Advertise request for CISCO FR with extended timing |

6.5 Vendor Specific 2 Device Registers

This register file contains the GPHY-specific registers for MMD=31 (decimal).

Table 34 Registers Overview- Vendor Specific 2 Device Registers

| Register Short Name | Register Long Name | Reset Value |
|----------------------------------|---|-------------------|
| VPSPEC2_WOL_CTL | WoL Control Register (Register 31.3590) | 0000 _H |
| VPSPEC2_WOL_AD01 | WoL Address Byte 0 and 1 (Register 31.3592) | 0000 _H |
| VPSPEC2_WOL_AD23 | WoL Address Byte 2 and 3 (Register 31.3593) | 0000 _H |
| VPSPEC2_WOL_AD45 | WoL Address Byte 4 and 5 (Register 31.3594) | 0000 _H |
| VPSPEC2_WOL_PW01 | WoL SecureON Password Byte 0 (Register 31.3595) | 0000 _H |
| VPSPEC2_WOL_PW23 | WoL SecureON Password Byte 2 and 3 (Register 31.3596) | 0000 _H |
| VPSPEC2_WOL_PW45 | WoL SecureON Password Byte 4 and 5 (Register 31.3597) | 0000 _H |

6.5.1 VSPEC2 Register Descriptions

This section describes all the VSPEC2 registers in detail.

Wake-on-LAN Control Register (Register 31.3590)

This is the Wake-on-LAN control register. Redirected to PCS_PDI_WOL_CTL.

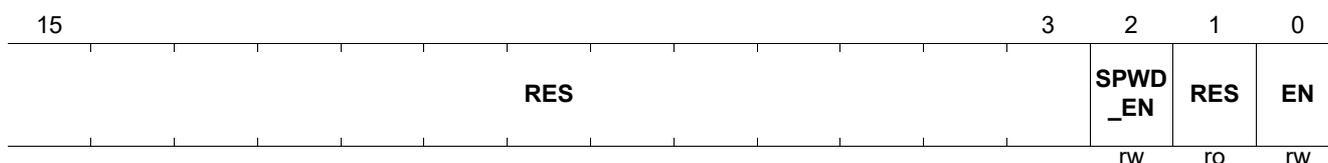
IEEE Standard Register=31.3590

VPSPEC2_WOL_CTL

Wake-on-LAN Control Register (Register 31.3590)

Reset Value

0000_H



| Field | Bits | Type | Description |
|---------|------|------|---|
| SPWD_EN | 2 | RW | Secure-ON Password Enable When this bit is set to enabled, the SecureON password is checked after 16 MAC address repetitions. 0 _B DISABLED Disables the SecureON password check 1 _B ENABLED Enables the SecureON password check |
| RES | 1 | RO | Reserved Must always be written to 0. |
| EN | 0 | RW | Enables the Wake-on-LAN Functionality When WoL is enabled, the PHY scans for the configured magic packet and indicates its reception via the register bit ISTAT. WoL and optionally also via interrupt. 0 _B DISABLED Disables the WoL functionality 1 _B ENABLED Enables the WoL functionality |

Wake-on-LAN Address Byte 0 and 1 (Register 31.3592)

Wake-on-LAN Address Byte 0 and 1. Redirected to PCS_PDI_WOL_AD01.

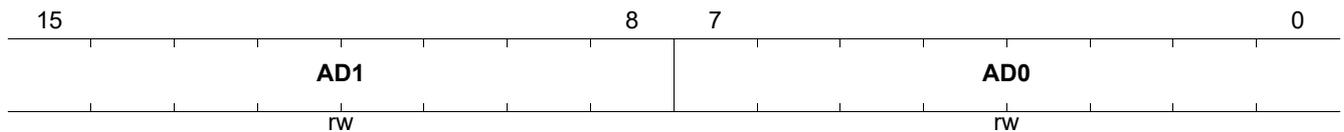
IEEE Standard Register=31.3592

VPSPEC2_WOL_AD01

Reset Value

Wake-on-LAN Address Byte 0 and 1 (Register 31.3592)

0000_H



| Field | Bits | Type | Description |
|-------|------|------|--|
| AD1 | 15:8 | RW | Address Byte 1 Defines byte 1 of the WoL-designated MAC address to which the PHY is sensitive. |
| AD0 | 7:0 | RW | Address Byte 0 Defines byte 0 of the WoL-designated MAC address to which the PHY is sensitive. |

Wake-on-LAN SecureON Password Byte 0 (Register 31.3595)

Wake-on-LAN SecureON Password Byte 0. Redirected to PCS_PDI_WOL_PWD01.

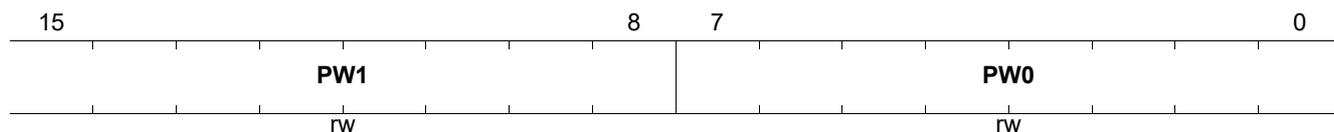
IEEE Standard Register=31.3595

VPSPEC2_WOL_PW01

Reset Value

Wake-on-LAN SecureON Password Byte 0 (Register 31.3595)

0000_H



| Field | Bits | Type | Description |
|-------|------|------|--|
| PW1 | 15:8 | RW | SecureON Password Byte 1 Defines byte 1 of the WoL-designated SecureON password to which the PHY is sensitive. |
| PW0 | 7:0 | RW | SecureON Password Byte 0 Defines byte 0 of the WoL-designated SecureON password to which the PHY is sensitive. |

Wake-on-LAN SecureON Password Byte 2 and 3 (Register 31.3596)

Wake-on-LAN SecureON Password Byte 2 and 3. Redirected to PCS_PDI_WOL_PWD23.

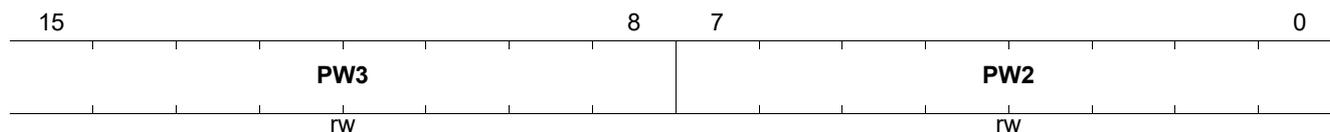
IEEE Standard Register=31.3596

VPSPEC2_WOL_PW23

Reset Value

Wake-on-LAN SecureON Password Byte 2 and 3 (Register 31.3596)

0000_H



| Field | Bits | Type | Description |
|-------|------|------|--|
| PW3 | 15:8 | RW | SecureON Password Byte 3 Defines byte 3 of the WoL-designated SecureON password to which the PHY is sensitive. |
| PW2 | 7:0 | RW | SecureON Password Byte 2 Defines byte 2 of the WoL-designated SecureON password to which the PHY is sensitive. |

Wake-on-LAN SecureON Password Byte 4 and 5 (Register 31.3597)

Wake-on-LAN SecureON Password Byte 4 and 5. Redirected to PCS_PDI_WOL_PWD45.

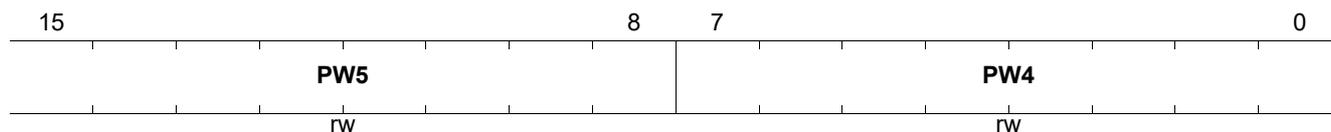
IEEE Standard Register=31.3597

VPSPEC2_WOL_PW45

Reset Value

Wake-on-LAN SecureON Password Byte 4 and 5 (Register 31.3597)

0000_H



| Field | Bits | Type | Description |
|-------|------|------|--|
| PW5 | 15:8 | RW | SecureON Password Byte 5 Defines byte 5 of the WoL-designated SecureON password to which the PHY is sensitive. |
| PW4 | 7:0 | RW | SecureON Password Byte 4 Defines byte 4 of the WoL-designated SecureON password to which the PHY is sensitive. |

7 Electrical Characteristics

This chapter provides the electrical characteristics for the MxL86289C.

7.1 Absolute Maximum Ratings

Table 35 shows the absolute maximum ratings for the MxL86289C.

Table 35 Absolute Maximum Ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|------|-------|------|--|
| | | Min. | Typ. | Max. | | |
| Storage Temperature Limits | T_{STG} | -55.0 | – | 125.0 | °C | – |
| Soldering Temperature | T_{SOL} | – | – | 260.0 | °C | Compliance with lead free re-flow soldering profile as J-STD-020D |
| Moisture Level 3 Temperature Limits | T_{ML3} | – | – | 260.0 | °C | According to IPS J-STD 020 |
| Absolute Junction Temperature | T_{JABS} | -40.0 | – | 125 | °C | The thermal solution must ensure that T_J never exceeds T_{JABS} maximum. The chip resets the device when $T_J > T_{JABS}$ maximum to prevent any damage to occur. |
| DC Voltage Limits on VDD3V3PAD1, VDD3V3PAD2 Pins | V_{DDP3V3} | -0.5 | – | +3.63 | V | Generic ball V_{HIGH} supply |
| DC Voltage Limits on VDDP_PAD Pins when Ball K3 Pin Strap PS_MDIO_VOLTAGE is HIGH | V_{DDP} | -0.5 | – | +3.63 | V | Multi voltage ball V_{HIGH} supply |
| DC Voltage Limits on VDDP_PAD Pins when Ball K3 Pin Strap PS_MDIO_VOLTAGE is LOW | V_{DDP} | -0.5 | – | +1.98 | V | Multi voltage ball supply. 1.8 V supply dedicated to MDIO pins in lower mode |
| DC Voltage Limits on VDDA3V3_0, VDDA3V3_1, VDDA3V3_2, VDDA3V3_3, VDDA3V3_4, VDDA3V3_5, VDDA3V3_6, and VDDA3V3_7 Pins | V_{DDA3V3} | -0.5 | – | +3.63 | V | Chip analog V_{HIGH} supply |
| DC Voltage Limits on VDDA1V8_0, VDDA1V8_1 Pins | V_{DDA1V8} | -0.5 | – | +1.98 | V | Chip analog supply |

Electrical Characteristics
Table 35 Absolute Maximum Ratings (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--|--------|------|--------------------|------|---|
| | | Min. | Typ. | Max. | | |
| DC Voltage Limits on VDDA1V8PORXO, VDDA1V8_PVT, VCC1V8_OTP Pins | $V_{DDA1V8PORXO}$ $V_{DDA1V8PVT}$ $V_{CC1V8OTP}$ | -0.5 | – | +1.98 | V | Chip clocking supply |
| DC Voltage Limits on VPHA1V8_0, VPHA1V8_1, and VDDA1V8_PLL Pins | V_{PH} $V_{DDA1V8PLL}$ | -0.5 | – | +1.98 | V | USXGMII, LJ PLL V_{HIGH} supply |
| DC Voltage Limits on VDDA1V2CDB0, VDDA1V2CDB1 Pins | $V_{DDA1V2CDB}$ | -0.5 | – | +1.32 | V | Chip analog supply |
| DC Voltage Limits on VDDA0V8_0, VDDA0V8_1, VDDD0V8REF, VDDD0V8POST Pins | V_{DDA0V8} $V_{DDD0V8PLL}$ | -0.5 | – | +0.88 | V | Chip analog V_{LOW} supply, LJ PLL V_{LOW} supply |
| DC Voltage Limits on VDDD0V8_COR Pins | V_{DD} | -0.5 | – | +0.88 | V | Chip core supply |
| DC Voltage Limits on VA0V8_0, VA0V8_1 Pins | V_P | -0.5 | – | +0.88 | V | USXGMII V_{LOW} supply |
| DC Voltage Limits on Any Other Pins ¹⁾ with Respect to Ground | V_{DC} | -0.5 | – | $V_{DDP3V3} + 0.5$ | V | Unless specified otherwise |
| XTAL1 Input Voltage | V_{XTAL1} | -0.30 | – | 2.0 | V | – |
| ESD HBM Robustness | $V_{ESD,HBM}$ | – | – | 1000.0 | V | According to ANSI/ESDA/JEDEC JS-001-2014 |
| ESD CDM Robustness | $V_{ESD,CDM}$ | – | – | 250.0 | V | According to ANSI/ESDA/JEDEC JS-002-2014 |

1) Any pin that is not a supply pin out of one of the domains: V_{DDP} , V_{PH} , V_P , V_{DDA3V3} , $V_{DDA1V8PORXO}$, $V_{DDA1V2CDB}$, V_{DDA0V8} , V_{DD} , and V_{DDA1V8} .

Attention: Stresses above the maximum values listed in this table may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.

7.2 Operating Range

Table 36 defines the limit values of voltages and temperature which may be applied to guarantee proper operation of the MxL86289C.

Table 36 Operating Range

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------------------|--------|------|-------|------|---|
| | | Min. | Typ. | Max. | | |
| Ambient Temperature under Bias | T_A | 0 | – | 70 | °C | The thermal design must ensure that the maximum junction temperature is not exceeded. The use of a heat sink may be suitable. |
| Junction Temperature | T_j | – | – | 110.0 | °C | Thermal solution must ensure that T_j remains within operating range and never exceeds maximum absolute ratings (T_{JABS}). |
| Generic Pin Supply Voltage | V_{DDP3V3} | 3.14 | 3.30 | 3.46 | V | Generic pin V_{HIGH} supply |
| Multi Voltage Pin Supply Voltage for MDIO Signals when Ball K3 Pin Strap PS_MDIO_VOLTAGE is HIGH | V_{DDP} | 3.14 | 3.30 | 3.46 | V | Multi voltage pin V_{HIGH} supply |
| Multi Voltage Pin Supply Voltage for MDIO Signals when Ball K3 Pin Strap PS_MDIO_VOLTAGE is LOW | V_{DDP} | 1.71 | 1.80 | 1.89 | V | Multi voltage pin supply. 1.8 V supply dedicated to MDIO pins in lower mode |
| Analog High Supply Voltage | V_{DDA3V3} | 3.14 | 3.30 | 3.46 | V | Chip analog V_{HIGH} supply |
| XO Supply Voltage | $V_{DDA1V8POR}$ XO | 1.71 | 1.80 | 1.89 | V | Chip clocking V_{HIGH} supply |
| Analog Medium Supply Voltage | V_{DDA1V8} | 1.71 | 1.80 | 1.89 | V | Chip analog V_{MED} supply |
| CDB Supply Voltage | $V_{DDA1V2CDB}$ | 1.14 | 1.20 | 1.26 | V | Chip analog supply |
| USXGMII High Supply Voltage | V_{PH} | 1.71 | 1.80 | 1.89 | V | USXGMII V_{HIGH} supply |
| LJ PLL High Supply Voltage | $V_{DDA1V8PLL}$ | 1.71 | 1.80 | 1.89 | V | LJ PLL V_{HIGH} supply |
| Analog Low Supply Voltage | V_{DDA0V8} | 0.76 | 0.8 | 0.84 | V | Chip analog V_{LOW} supply |
| LJ PLL Low Supply Voltage | $V_{DDD0V8PLL}$ | 0.76 | 0.8 | 0.84 | V | LJ PLL V_{LOW} supply |
| Chip Core Supply Voltage | V_{DD} | 0.76 | 0.8 | 0.84 | V | Chip core supply |
| USXGMII Low Supply Voltage | V_P | 0.76 | 0.8 | 0.84 | V | USXGMII V_{LOW} supply |
| Ground | V_{SS} | 0.00 | 0.00 | 0.00 | V | – |

Attention: Operations above the maximum values listed here for extended periods may adversely affect long-term reliability of the device.

7.3 Typical Power Consumption

Table 37 lists the typical power consumption for different modes. Typical power is the power consumed by a nominal process device, nominal supply voltages, at 25°C ambient temperature and a CAT5e link segment.

The conditions for Link-up are full speed and bidirectional, full duplex traffic on all 8 ports. There are 10G links on both SerDes interfaces.

Table 37 Typical Power Consumption

| | 3.3 V V _{HIGH} Domain Current | 1.8 V Domain Current | 1.2 V Domain Current | 0.8 V V _{LOW} Domain Current | 0.8 V V _P Domain Current | Chip Power |
|---------------------------------|--|----------------------------|----------------------------|---|---|---------------|
| Unit | mA | mA | mA | mA | mA | W |
| 2500BASE-T Link-up, 100 m Cable | 393 | 138 | 470 | 3453 | 128 | 5.0 |
| 2500BASE-T Link-up, 30 m Cable | 372 | 136 | 450 | 2930 | 127 | 4.5 |
| 2500BASE-T EEE | 313 | 124 | 138 | 1592 | 124 | 2.8 |
| 1000BASE-T Link-up, 100 m Cable | 306 | 136 | 435 | 1489 | 124 | 3.1 |
| 1000BASE-T EEE | 47 | 126 | 123 | 895 | 126 | 1.3 |
| 100BASE-TX Link-up, 100 m Cable | 91 | 124 | 111 | 694 | 122 | 1.3 |
| 100BASE-TX EEE | 60 | 148 | 120 | 646 | 124 | 1.0 |
| 10BASE-Te Link-up, 100 m Cable | 89 | 127 | 66 | 616 | 117 | 1.2 |
| Cable Unplugged - ANEG | 40 | 127 | 66 | 635 | 123 | 1.0 |
| Cable Unplugged - Low Power | 23 | 121 | 4 | 338 | 123 | 0.7 |
| Reset | 3 | 25 | 0 | 64 | 3 | 0.1 |

7.4 Maximum Thermal Design Power

Table 38 lists the maximum Thermal Design Power (TDP). The TDP is the power consumption for a full traffic load and worst-case process, supply voltage, cable, and temperature conditions. This value is relevant to design the thermal solution.

Table 38 Maximum Power Consumption

| | Maximum Power |
|---|---------------|
| Unit | W |
| Maximum Chip Power at Maximum Operating Range | 7.0 |

Note: With a properly designed thermal solution (heat sink), it is unlikely that T_j exceeds the maximum operating junction temperature. An excess is reported in the MDIO register VSPEC1_TEMP_STA and the STA can initiate a renegotiation to a lower link rate to get T_j back into the operating temperature range if ADS is disabled.

7.5 Maximum Current

Table 39 provides the maximum current to dimension the power supply. It is the maximum current consumption per rail for a full traffic load and worst-case process, supply voltage and temperature conditions that may occur in any operating state of the device. The maximum current can be higher than the steady state current, for instance in training phases of the internal filters.

Electrical Characteristics

Table 39 Maximum Current Per Rail

| 3.3 V Domain Current | 1.8 V Domain Current | 1.2 V Domain Current | 0.8 V V _{LOW} Domain Current | 0.8 V V _P Domain Current |
|----------------------|----------------------|----------------------|---------------------------------------|-------------------------------------|
| mA | mA | mA | mA | mA |
| 477 | 154 | 587 | 6000 | 203 |

7.6 DC Characteristics

These sections document the DC characteristics of the MxL86289C external interfaces.

7.6.1 Digital Interfaces

This section defines the DC characteristics of the GPIO interface as follows:

- General Purpose IO
- MDIO
- QSPI
- UART
- I²C
- Interrupts
- Clock Input and Outputs
- LED
- JTAG
- HRSTN

Table 40 summarizes the DC characteristics for $V_{DDP} = 3.3\text{ V}$.

Table 40 DC Characteristics of the GPIO Interfaces (VDDP = 3.3 V)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------|----------|---------------------|------|---------------------|------|----------------------------------|
| | | Min. | Typ. | Max. | | |
| Input High Voltage | V_{IH} | $0.7 \cdot V_{DDP}$ | – | $V_{DDP} + 0.3$ | V | – |
| Input Low Voltage | V_{IL} | –0.3 | – | $0.3 \cdot V_{DDP}$ | V | – |
| Output High Voltage | V_{OH} | $V_{DDP} - 0.4$ | – | – | V | $I_{OH} = 2, 4, 8, 12\text{ mA}$ |
| Output Low Voltage | V_{OL} | – | – | 0.4 | V | $I_{OL} = 2, 4, 8, 12\text{ mA}$ |

Table 41 summarizes the DC characteristics for $V_{DDP} = 1.8\text{ V}$.

Table 41 DC Characteristics of the GPIO Interfaces (VDDP = 1.8 V)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------|----------|----------------------|------|----------------------|------|----------------------------------|
| | | Min. | Typ. | Max. | | |
| Input High Voltage | V_{IH} | $0.65 \cdot V_{DDP}$ | – | $V_{DDP} + 0.3$ | V | – |
| Input Low Voltage | V_{IL} | –0.3 | – | $0.35 \cdot V_{DDP}$ | V | – |
| Output High Voltage | V_{OH} | $V_{DDP} - 0.4$ | – | – | V | $I_{OH} = 2, 4, 8, 12\text{ mA}$ |
| Output Low Voltage | V_{OL} | – | – | 0.4 | V | $I_{OL} = 2, 4, 8, 12\text{ mA}$ |

7.6.2 Twisted Pair Interface

The TPI conforms to the specifications of 10BASE-Te (Clause 14), 100BASE-TX (Clause 25), 1000BASE-T (Clause 40), and 2.5GBASE-T (Clause 126) given in IEEE 802.3, and ANSI X3.263-1995.

7.6.3 Built-in Temperature Sensor

Table 42 provides the parameters of the integrated temperature sensor.

Table 42 Temperature Sensor Characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------|--------------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Temperature Range | T _{range} | -40 | | 125 | °C | The thermal mitigation measures must ensure that T _j remains within the operating range. When T _j exceeds the maximum ratings, the device performs a self-reset to prevent damage. |
| Resolution | | – | 12 | – | bits | – |
| Accuracy | | -3 | – | +3 | °C | Without calibration |

7.7 AC Characteristics

The AC characteristics of the external interfaces are specified under these operating conditions:

$$T_A = 0 \text{ to } 70^\circ\text{C}$$

$$V_{DDP} = 3.3 \text{ V} \pm 5\%$$

$$V_{SS} = 0 \text{ V}$$

The timing measurements are made at minimum V_{IH} for a logical 1 and at maximum V_{IL} for a logical 0. See [Table 40](#) and [Table 41](#) for more details.

[Figure 17](#) shows the AC testing input/output waveforms. The load capacitors are according to the specific interface standard. All non-specified interfaces use 30 pF as assumed loading.

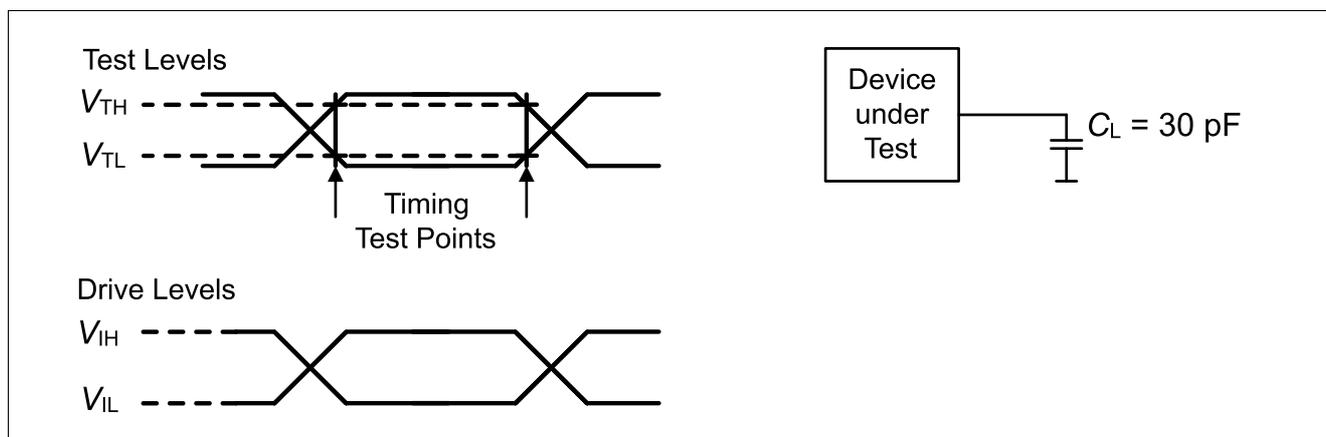


Figure 17 Input/Output Waveform for AC Tests

7.7.1 Power Up Sequence

All V_{HIGH} , V_{PH} , V_{DDA} , V_P , and V_{LOW} are supplied externally.

In this section, for the sake of simplicity:

- All 3.3 V supplies are represented as V_{HIGH} .
- All 1.8 V supplies are represented as V_{PH} .
- All 1.2 V supplies are represented as V_{DDA} .
- The 0.8 V analog supply of SerDes is represented as V_P .
- The rest of the 0.8 V supplies are represented as V_{LOW} .

All the supply domains V_{HIGH} , V_{PH} , V_{DDA} , V_P , and V_{LOW} , and the input reference clock must be stabilized before releasing the reset HRSTN.

There is no known voltage rail power up sequence except that V_{HIGH} must be ramped up and stable before V_{PH} is ramped up, V_{LOW} must be ramped up and stable before V_P is ramped up, and V_{LOW} must be ramped up and stable before V_{PH} is ramped up. MaxLinear recommends implementing the power-up sequence defined in the reference board. Refer to the relevant hardware documentation available at <https://maxlinear.com/myMxL> for more information on the power circuitry.

The MxL86289C supports an asynchronous hardware reset HRSTN. [Table 43](#) lists the timing requirements of the power supply pins. The timings refer to the signal sequence waveforms depicted in [Figure 18](#).

When PS_MDIO_VOLTAGE is low, V_{DDP} is treated as V_{PH} .

When PS_MDIO_VOLTAGE is high, V_{DDP} is treated as V_{HIGH} .

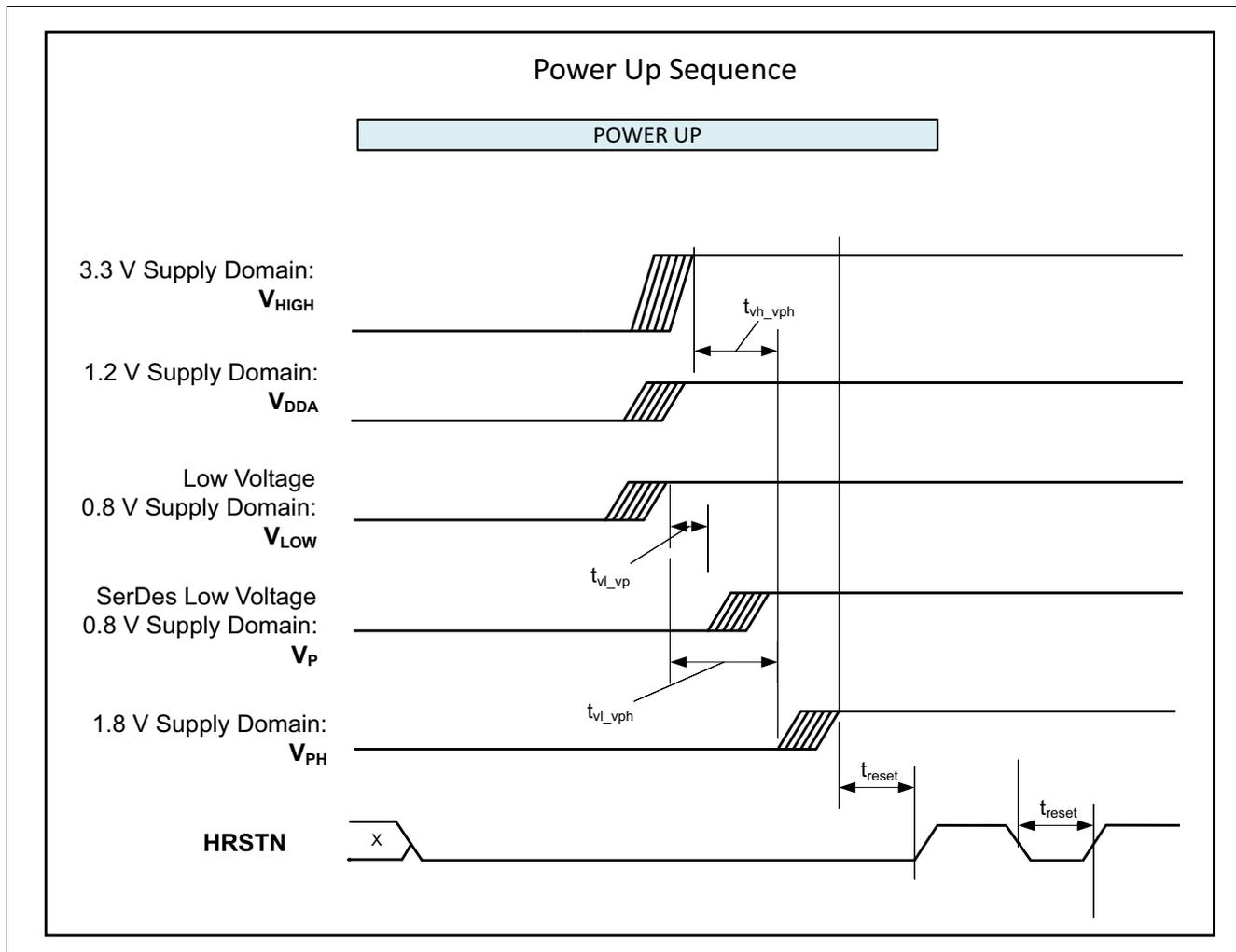


Figure 18 Timing Diagram for the Reset Sequence

Table 43 Power Supply Timings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---------------|--------|------|------|---------|--|
| | | Min. | Typ. | Max. | | |
| Delay between V_{HIGH} and V_{PH} Domains Voltage Ramp Up | t_{vh_vph} | 50 | - | - | μs | The V_{PH} voltage must never be higher than V_{HIGH} voltage |
| Delay between V_{LOW} and V_P Domains Voltage Ramp Up | t_{vl_vp} | 1 | - | - | μs | The V_P voltage must never power up before V_{LOW} voltage. |
| Delay between V_{LOW} and V_{PH} Domains Voltage Ramp Up | t_{vl_vph} | 50 | - | - | μs | The V_{PH} voltage must never power up before V_{LOW} voltage. |
| Reset Time after all Voltage Domains are Stabilized | t_{reset} | 100 | - | - | ns | HRSTN must be released after the power supplies stabilized. |

7.7.2 Input Clock

Table 44 lists the input clock requirements when not using a crystal, for example when an external reference clock is injected into the XTAL1 pin of the MxL86289C, such as nominal frequency, frequency deviation, duty cycle, and signal characteristics. When a crystal is applied to generate the reference clock using the integrated XO, the clock requirements stated here are explicitly met as long as the specification for the crystal is satisfied.

Table 44 AC Characteristics of Input Clock on XTAL1 Pin

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------------------------|--------------|--------|--------|-------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Frequency with 25 MHz Input | f_{clk25} | – | 25.0 | – | MHz | – |
| Frequency with 50 MHz Input | f_{clk50} | – | 50.0 | – | MHz | – |
| Frequency with 156.25 MHz Input | f_{clk156} | – | 156.25 | – | MHz | – |
| Frequency Deviation ¹⁾ | | -50.0 | – | +50.0 | ppm | – |
| Duty Cycle | | 40.0 | 50.0 | 60.0 | % | – |
| Rise/Fall Times with 25 MHz Input | | – | – | 10.0 | ns | 25 MHz |
| Rise/Fall Times with 50 MHz Input | | – | – | 5.0 | ns | 50 MHz |
| Rise/Fall Times with 156.25 MHz Input | | – | – | 1.0 | ns | 156.25 MHz |
| Input Long Term Jitter (Jrms) | | – | – | 2.0 | ps | 1 kHz to 10 MHz |
| Input Voltage Swing | | 300.0 | – | – | mV | Peak to Peak value |
| Input Voltage | | 0 | – | 1.8 | V | – |

1) Including the frequency stability tolerance due to temperature, and aging effects over the product lifetime.

7.7.3 Power Supply Rail Requirements

Table 45 lists the required characteristics of the power supplies. The definitions of the power supply rails are the same as that described in [Section 7.7.1](#).

Table 45 AC Characteristics of the Power Supply

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------------------|-------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Power Supply Ripple on V_P | R_{VP} | – | – | 40.0 | mV | Peak to Peak value Refer to Figure 19 . |
| Power Supply Ripple on V_{LOW} | R_{VLOW} | – | – | 40.0 | mV | Peak to Peak value |
| Power Supply Ripple on V_{DDA} | R_{VDDA} | – | – | 50.0 | mV | Peak to Peak value |
| Power Supply Ripple on V_{HIGH} | R_{VHIGH} | – | – | 50.0 | mV | Peak to Peak value |
| Power Supply Ripple on V_{PH} | R_{VPH} | – | – | 50.0 | mV | Peak to Peak value Max. 18 mV peak to peak for any noise in 200 kHz to 100 MHz range. Refer to Figure 20 . |

7.7.3.1 V_P AC and DC Power Supply Recommendations

This section contains the V_P supply power requirements.

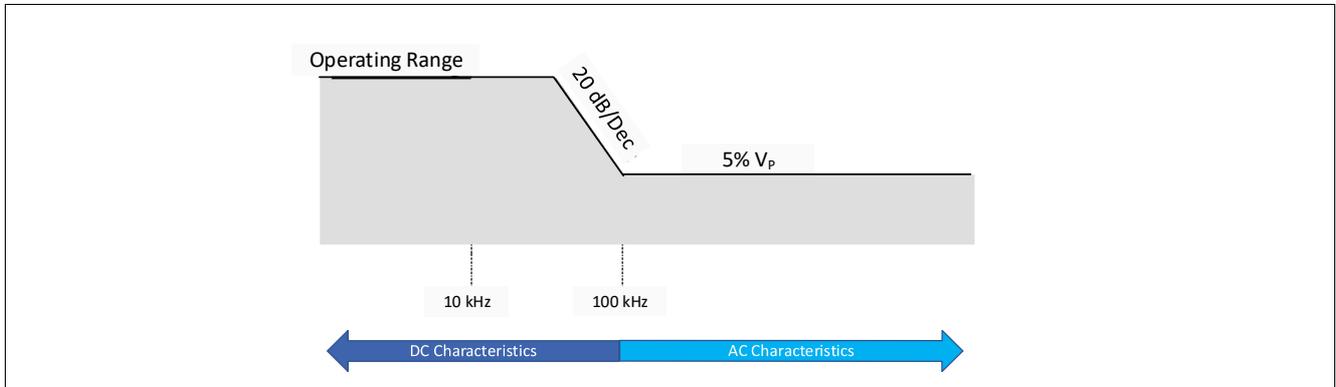


Figure 19 DC and AC Characteristics for V_P Supply

DC Characteristics

- Operating range: Refer to the range of V_P in [Table 36](#)
- Frequency range: 0 to 100 kHz
- Recommendations:
 - The overshoot or undershoot of the low-frequency supply caused by the board filter network should be lower than 100 kHz.
 - The overall DC budget should account for the low frequency overshoot/undershoot in addition to the board plus package IR drop.
 - There is a transition zone between 10 kHz and 100 kHz in which it is possible for the supply noise to increase as the frequency decreases at a rate of 20 dB/Dec up to the maximum of the operating range.

AC Characteristics

- Max 5% (peak-to-peak) of the DC level for all noise greater than 100 kHz
- Recommendations:
 - A switching supply can be used until the overall noise limits (including, the self noise) are met.

7.7.3.2 V_{PH} AC and DC Power Supply Recommendations

This section contains the V_{PH} supply power requirements.

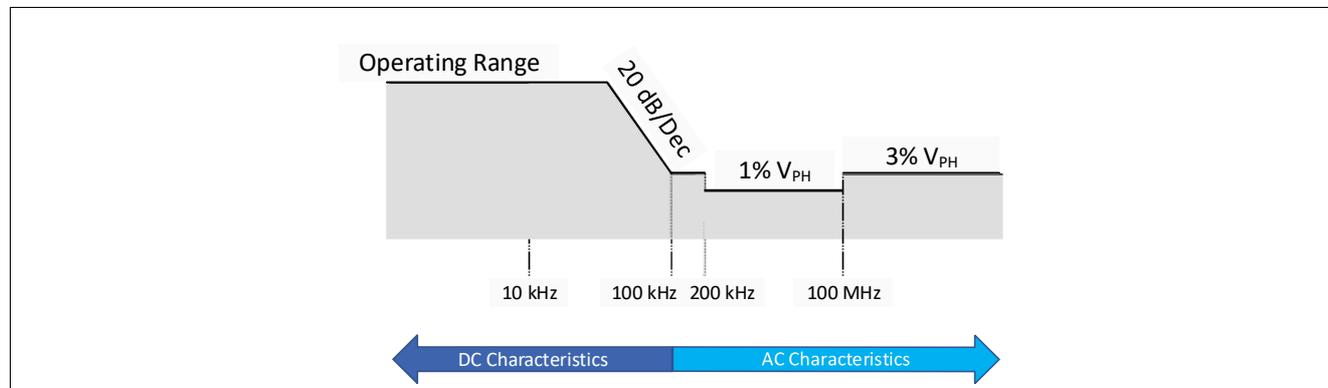


Figure 20 DC and AC Characteristics for V_{PH} Supply

DC Characteristics

- Operating range: Refer to the range of V_{PH} in [Table 36](#)
- Frequency range: 0 to 100 kHz
- Recommendations:
 - The overshoot or undershoot of the low-frequency supply caused by the board filter network should be lower than 100 kHz.
 - The overall DC budget should account for the low frequency overshoot/undershoot in addition to the board plus package IR drop.
 - There is a transition zone between 10 kHz and 100 kHz in which it is possible for the supply noise to increase as the frequency decreases at a rate of 20 dB/Dec up to the maximum of the operating range.

AC Characteristics

- 100 kHz to 200 kHz: A maximum value of 3% ripple (peak-to-peak) of the DC level is allowed for all noise in this region.
- 200 kHz to 100 MHz: A maximum value of 1% ripple (peak-to-peak) of the DC level is allowed in this region.
- 100 MHz and above: A maximum value of 3% ripple (peak-to-peak) of the DC level is allowed for all noise in this region.
- Recommendations:
 - Use an LDO as a switching supply.
 - When using a switching power supply for V_{PH} , ensure that the 200 kHz to 100 MHz ripple requirements are met. Switching power supplies' tone and harmonics typically occur in this region.
 - Do not share this power rail directly with any other noisy circuitry.
 - Follow the relevant hardware documentation available at <https://maxlinear.com/myMxL> on the power circuitry.

7.7.4 MDIO Slave Interface

Figure 21 shows a timing diagram of the MDIO slave interface for a clock cycle in the read, write, and turnaround mode, respectively. The timing measures are annotated. Table 46 summarizes the defined absolute values.

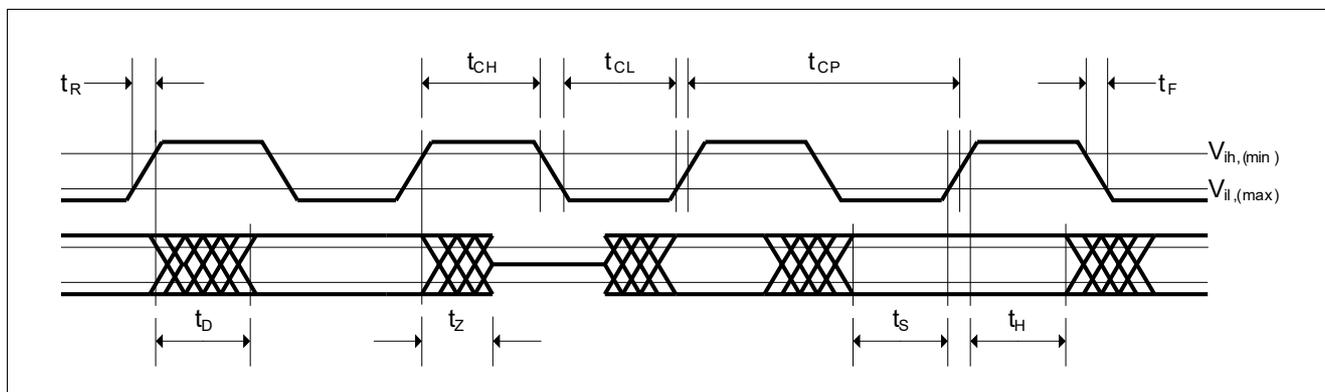


Figure 21 Timing Diagram for the MDIO Slave Interface

Table 46 Timing Characteristics of the MDIO Slave Interface

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|----------|--------|-------|-------|------|---|
| | | Min. | Typ. | Max. | | |
| MDC High Time | t_{CH} | 10.0 | – | – | ns | Given timings are all subject to the MDC at the pin of the MxL86289C. |
| MDC Low Time | t_{CL} | 10.0 | – | – | ns | |
| MDC Clock Period | t_{CP} | 40.0 | 400.0 | – | ns | |
| MDC Clock Frequency ¹⁾ | t_{CP} | – | 2.5 | 25.0 | MHz | |
| MDC Rise Time | t_R | – | – | 5.0 | ns | |
| MDC Fall Time | t_F | – | – | 5.0 | ns | |
| MDIO Input Setup Time Subject to \uparrow MDC | t_S | 10.0 | – | – | ns | MxL86289C Receive |
| MDIO Input Hold Time Subject to \uparrow MDC | t_H | 10.0 | – | – | ns | MxL86289C Receive |
| MDIO Output Delay Time Subject to \uparrow MDC | t_D | 0.0 | – | 10 | ns | MxL86289C Transmit |
| Standard at 2.5 MHz | | | | | | |
| MDIO Output Delay Subject to \uparrow MDC | t_D | 0.0 | – | 300.0 | ns | PHY Transmit |

1) MDC clock supports range of frequencies, up to 25 MHz. Default/typical frequency is 2.5 MHz.

7.7.5 Quad Serial Peripheral Interface (QSPI)

Figure 22 shows the QSPI master timing.

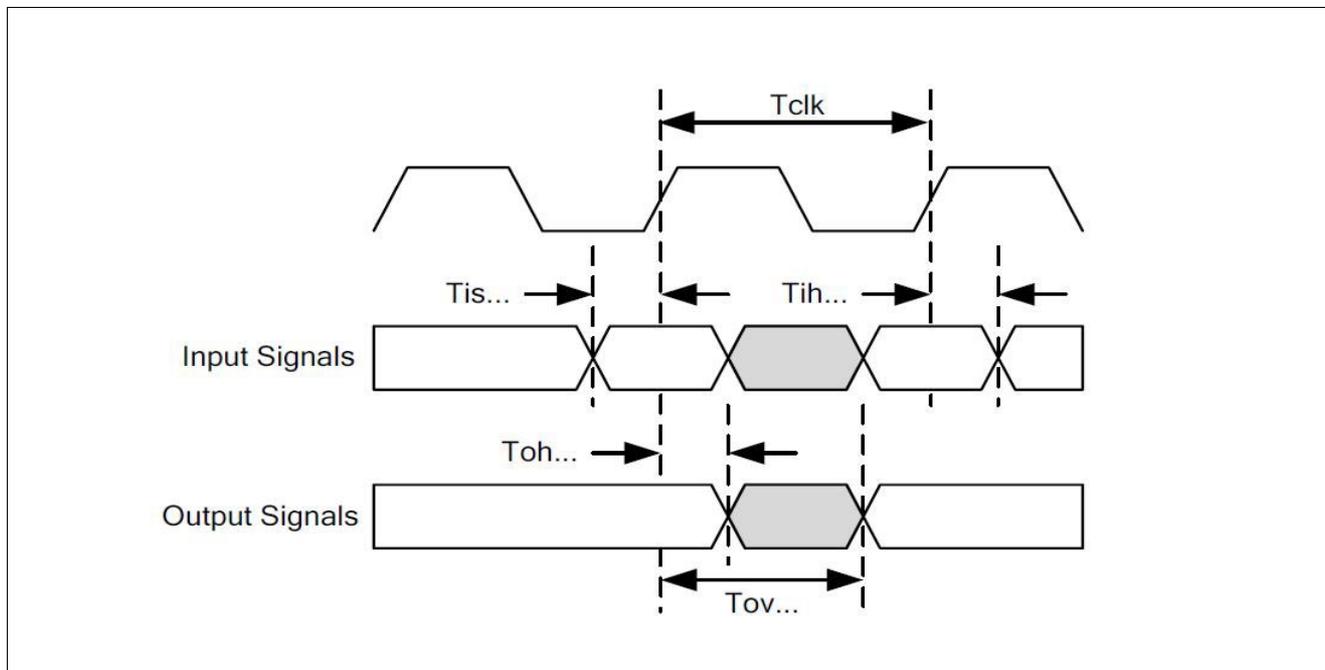


Figure 22 QSPI Master Interface Timing

Table 47 QSPI Interface Timing Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------------|-----------|--------|------|------|------|-------------------------|
| | | Min. | Typ. | Max. | | |
| Master Mode | | | | | | |
| TX Data Output Hold | T_{oh} | 5% | – | – | Tclk | For Tclk = 20 ns |
| Tx Data Output Delay | T_{ov} | 0 | – | 50% | Tclk | For Tclk = 20 ns |
| Rx Data Input Setup time | T_{is} | 35% | – | – | Tclk | For Tclk = 20 ns |
| Rx Data Hold Time | T_{ih} | 5% | – | – | Tclk | For Tclk = 20 ns |
| SPI Clock Period (Master Mode) | T_{clk} | 9.846 | – | – | ns | Maximum 101.5625 MHz |
| SPI Clock Rising | S_7 | 0.1 | – | – | V/ns | – |
| SPI Clock Falling | S_6 | 0.1 | – | – | V/ns | – |

7.7.6 I²C Interface

Figure 23 shows the I²C interface timing.

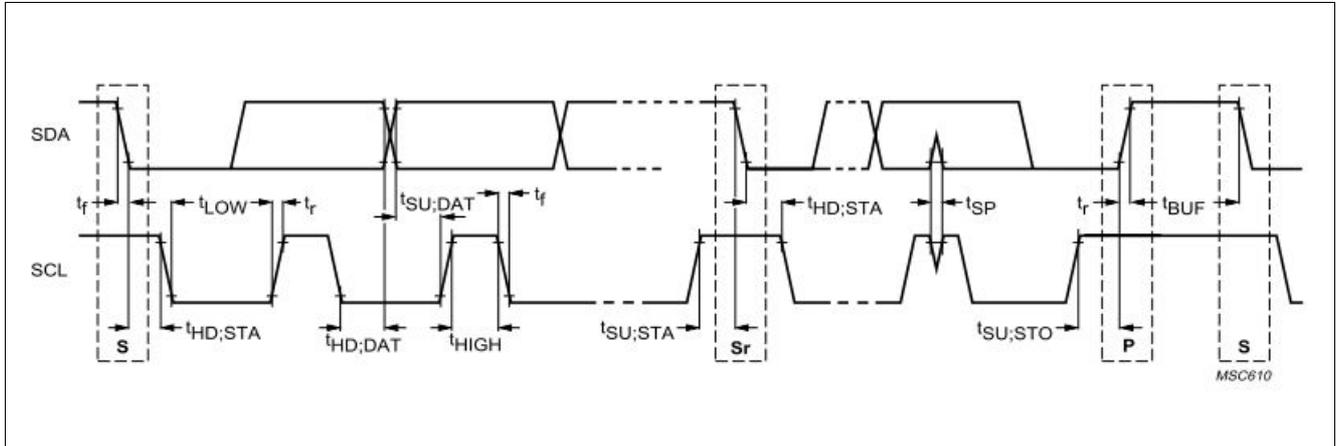


Figure 23 I²C Timing

Table 48 describes the timing values.

Table 48 I²C Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------------------|------------------|--------|------|------|---------|-----------------------|
| | | Min. | Typ. | Max. | | |
| SCL Frequency | f_{SCL} | 0 | – | 100 | kHz | – |
| Setup Time Data to Shift Clock | $t_{SU,DAT}$ | 250 | – | – | ns | – |
| Hold Time Data to Shift Clock | $t_{HD,DAT}$ | 0 | – | 3.45 | μ s | – |
| Setup Time START to Shift Clock | $t_{SU,STA}$ | 4700 | – | – | ns | – |
| Hold Time START, STOP to Shift Clock | $t_{HD,STA/STO}$ | 4.0 | – | – | μ s | – |
| Low Time | t_{LOW} | 4700 | – | – | ns | – |
| High Time | t_{HIGH} | 4000 | – | – | ns | – |
| Rising Time | t_r | – | – | 1000 | ns | – |
| Falling Time | t_f | – | – | 300 | ns | – |
| Bus Free Time | t_{BUF} | 4700 | – | – | ns | – |

7.7.7 JTAG Interface

The JTAG test interface is used for debugging the CPU and boundary scan.

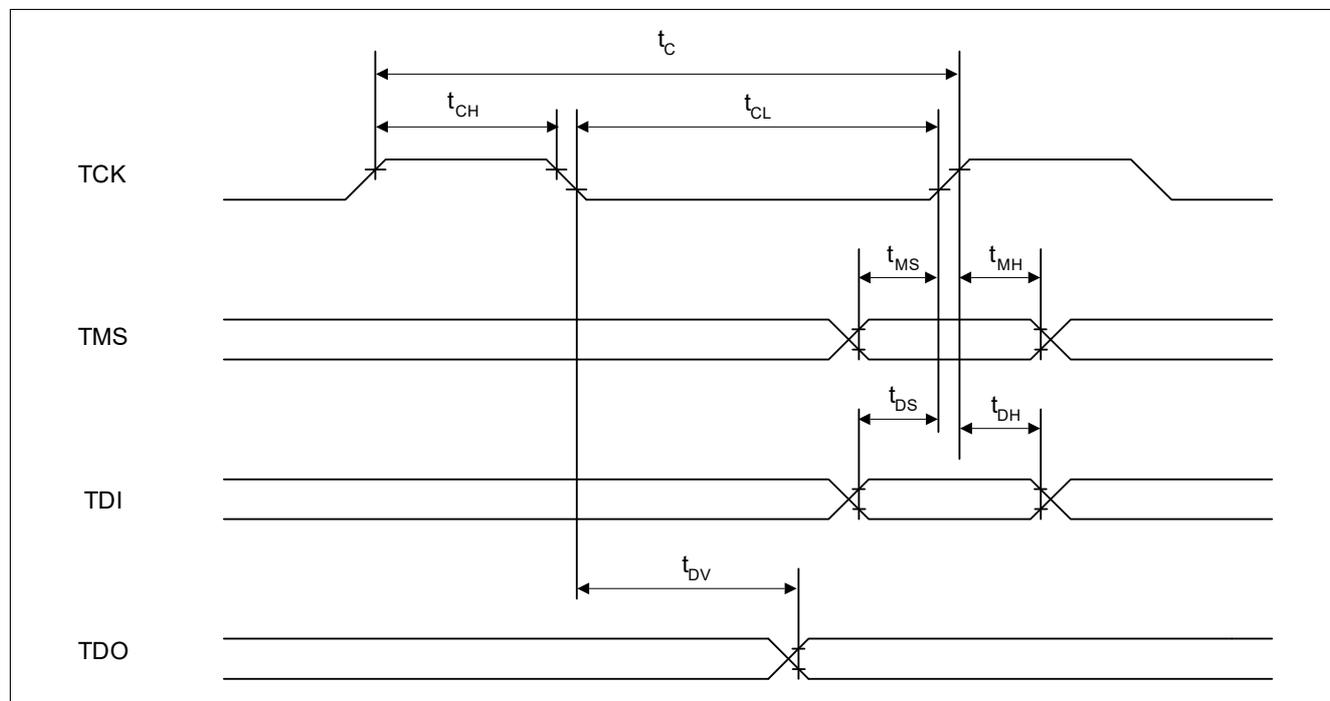


Figure 24 Test Interface Timing

[Table 49](#) and [Table 50](#) describe the timing values for the test interface.

Table 49 Test Interface Clock

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|------------------|----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| TCK Clock Period | t_C | 100 | – | – | ns | – |
| TCK High Time | t_{CH} | 40 | – | – | ns | – |
| TCK Low Time | t_{CL} | 40 | – | – | ns | – |

Table 50 JTAG Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------|----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| TMS Setup Time | t_{MS} | 40 | – | – | ns | – |
| TMS Hold Time | t_{MH} | 40 | – | – | ns | – |
| TDI Setup Time | t_{DS} | 40 | – | – | ns | – |
| TDI Hold Time | t_{DH} | 40 | – | – | ns | – |
| Hold: TRSTN After TCK | t_{HD} | 10 | – | – | ns | – |
| TDO Valid Delay | t_{DV} | – | – | 60 | ns | – |

7.7.8 USXGMII Interface Characteristics

This section describes the AC characteristics of the USXGMII interface on the MxL86289C.

The USXGMII interface characteristics are described in:

- USXGMII transmit characteristics ([Section 7.7.8.1](#))
- USXGMII receive characteristics ([Section 7.7.8.2](#))

7.7.8.1 USXGMII Transmit Characteristics

[Table 51](#) shows the requirements of the USXGMII interface on the MxL86289C.

Table 51 Transmit Characteristics of the USXGMII

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|------------------|--------|------|------|----------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Reference Differential Impedance | Z_d | – | 100 | – | Ω | – |
| Termination Mismatch | R_M | – | – | 5 | % | – |
| DC Common Mode Voltage | V_{cm} | 0 | – | 3.6 | V | – |
| Output Rise and Fall Time | t_{RH}, t_{FH} | 24 | – | – | ps | 20%→80% |
| Output AC Common Mode Voltage | – | – | – | 15 | mV | mV (RMS) |
| Differential Output Return Loss ¹⁾ | SDD22 | 20 | – | – | dB | 0.05-0.1 GHz |
| | | 10 | – | – | dB | 0.1-7.5 GHz |
| | | – | – | – | | 7.5-15 GHz |
| Common Mode Output Return Loss ²⁾ | SCC22 | 6 | – | – | dB | 0.1-15 GHz |

1) Return loss given by equation $SDD22(dB) = 10 - 16.6 \log_{10}(f/7.5)$, with f in GHz.

2) Common mode reference impedance is 25 Ω common mode return loss helps absorb reflections and noise for EMI.

7.7.8.2 USXGMII Receive Characteristics

[Table 52](#) shows the requirements of the USXGMII interface on the MxL86289C.

Table 52 Receive Characteristics of the USXGMII

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------|--------|------|------|----------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Reference Differential Impedance | Z_d | – | 100 | – | Ω | – |
| Termination Mismatch | Z_M | – | – | 5 | % | – |
| AC Common Mode Voltage | – | – | – | 25 | mV | mV (RMS) |
| Differential Output Return Loss ¹⁾ | SDD11 | 20 | – | – | dB | 0.05-0.1 GHz |
| | | 10 | – | – | dB | 0.1-7.5 GHz |
| | | – | – | – | | 7.5-15 GHz |
| Common Mode Input Return Loss ²⁾ | SCC11 | 6 | – | – | dB | 0.1-15 GHz |
| Differential to Common Mode Input Conversion ²⁾ | SCD11 | 12 | – | – | dB | 0.1-15 GHz |

1) Return loss given by equation $SDD11(dB) = 10 - 16.6 \log_{10}(f/7.5)$, with f in GHz.

2) Common mode reference impedance is 25 Ω . SCD11 relates to conversion of differential to common mode and the associated generation of EMI.

7.7.9 Crystal Specification

The 25 MHz crystal must follow the specification given in [Table 53](#).

Table 53 Specification of the Crystal

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------------|-------------|--------|------|------|----------|--|
| | | Min. | Typ. | Max. | | |
| Frequency with 25 MHz Input | f_{clk25} | – | 25.0 | – | MHz | – |
| Total Frequency Stability | – | -50 | – | +50 | ppm | Refers to the sum of all effects: such as general tolerance, aging, and temperature dependency |
| Series Resonant Resistance | – | – | – | 40 | Ω | – |
| Drive Level | – | – | 0.1 | 0.2 | mW | – |
| Load Capacitance | C_L | 16 | – | 26 | pF | – |
| Shunt Capacitance | C_0 | – | – | 7 | pF | – |

7.8 External Circuitry

This section specifies the component characteristics of the external circuitry connected to the TPIs of the MxL86289C.

7.8.1 Twisted-Pair Common-Mode Rejection and Termination Circuitry

Figure 25 shows the external circuitry necessary to properly terminate the common mode of the TPI.

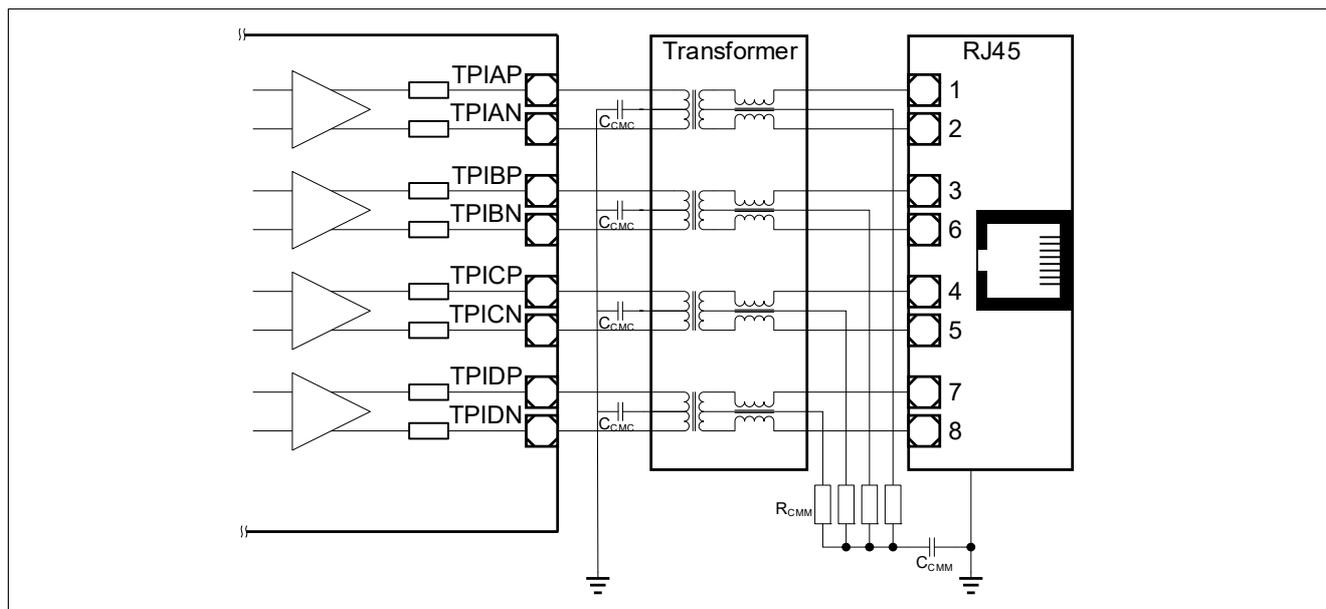


Figure 25 Twisted Pair Common-Mode Rejection and Termination Circuitry

Table 54 defines the component values and their supported tolerances.

Table 54 Electrical Characteristics for Common-Mode Rejection and Termination Circuitry

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Common-Mode Decoupling Capacitance (Media End) | C_{CMM} | 800 | 1000 | 1200 | pF | ±15%, 3 kV |
| Common-Mode Decoupling Capacitance (Chip End) | C_{CMC} | 80 | 100 | 120 | nF | ±15%, 25 V |
| Common-Mode Termination Resistance (Media End) | R_{CMM} | 67.5 | 75 | 82.5 | Ω | ±5% |

7.8.2 Transformer (Magnetics)

This section specifies the required electrical characteristics of the transformer¹⁾ devices that are supported. The specifications listed here guarantee proper operation according to IEEE 802.3 [3].

Figure 26 depicts a typical Gigabit Ethernet capable transformer device.

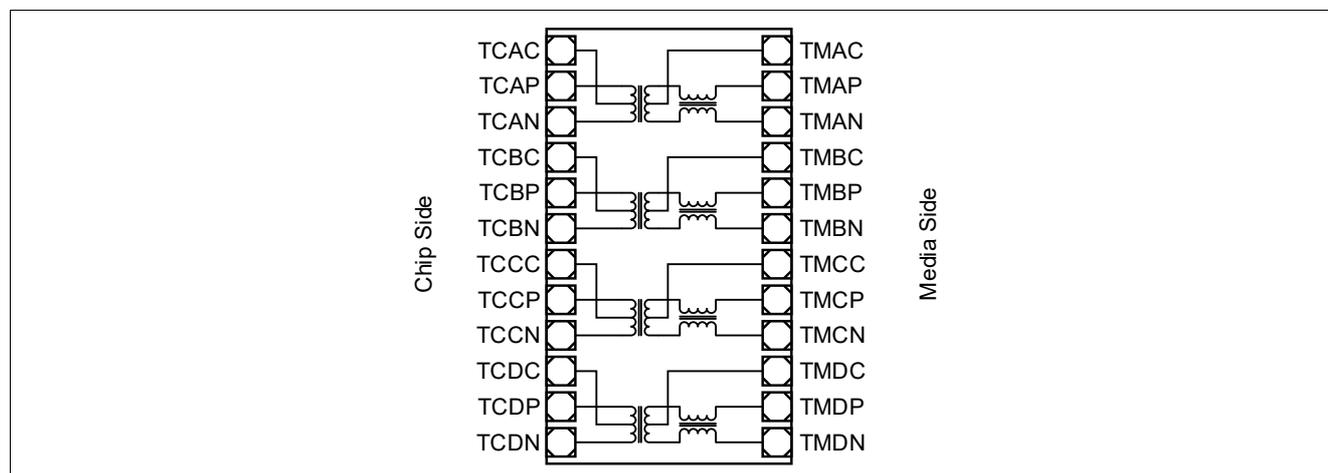


Figure 26 Schematic of an Ethernet Transformer Device

Table 55 lists the characteristics of the supported transformer devices. These characteristics represent the minimum values for achieving standard performance. Since the transformer significantly impacts the link performance, it is possible to increase the loop reach by selecting transformers with improved parameters.

Table 55 Electrical Characteristics for Supported Transformers (Magnetics)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------------------------|--------|--------------------------------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Turns Ratio | 1:tr | 0.95 | 1.00 | 1.05 | | ±5% |
| Differential-to-Common-mode Rejection | DCMR | 40 | – | – | dB | 30 MHz |
| | | 35 | – | – | dB | 60 MHz |
| | | 30 | – | – | dB | 100 MHz |
| Crosstalk Attenuation | CTA | 45 | – | – | dB | 30 MHz |
| | | 40 | – | – | dB | 60 MHz |
| | | 35 | – | – | dB | 100 MHz |
| Insertion Loss | IL | – | – | 1 | dB | 1 MHz ≤ f ≤ 250 MHz |
| Return Loss | RL | 16 | – | – | dB | 1 MHz ≤ f ≤ 40 MHz |
| Return Loss | RL | 16-10*log ₁₀ (f/40) | – | – | dB | 40 MHz ≤ f ≤ 250 MHz |

1) Also often referred to as magnetics.

7.8.3 RJ45 Plug

Table 56 describes the electrical characteristics of the RJ45 plug to be used in conjunction with MxL86289C.

Table 56 Electrical Characteristics for Supported RJ45 Plugs

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------|--------|---------------------------------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Crosstalk Attenuation | CTA | 45 | – | – | dB | 30 MHz |
| | | 40 | – | – | dB | 60 MHz |
| | | 35 | – | – | dB | 100 MHz |
| Insertion Loss | IL | – | – | 1 | dB | $1 \text{ MHz} \leq f \leq 250 \text{ MHz}$ |
| Return Loss | RL | 16 | – | – | dB | $1 \text{ MHz} \leq f \leq 40 \text{ MHz}$ |
| Return Loss | RL | $16 - 10 \cdot \log_{10}(f/40)$ | – | – | dB | $40 \text{ MHz} \leq f \leq 250 \text{ MHz}$ |

8 Package Outline

The product is assembled in a PG-FCLBGA-256 package, which complies with regulations requiring lead free material. [Table 57](#) lists the parameters generated in accordance with JEDEC JESD51 standards [\[6\]](#).

Table 57 JEDEC Thermal Resistance Package Parameter - Compact 2-R Model Network

| Item | Name/Value |
|--|---|
| Thermal Resistance - Junction to Case Top | $R_{th, Jctop} = 0.084 \text{ K/W}$ |
| Minimum Thermal Resistance - Junction to 0 mm from package edge on PCB | $R_{minth, Jbottom} = 3.70 \text{ K/W}$ |
| Maximum Thermal Resistance - Junction to 1 mm from package edge on PCB | $R_{maxth, Jbottom} = 4.25 \text{ K/W}$ |

Figure 10 shows the mechanical drawings for this package. The dimensions are in millimeters.

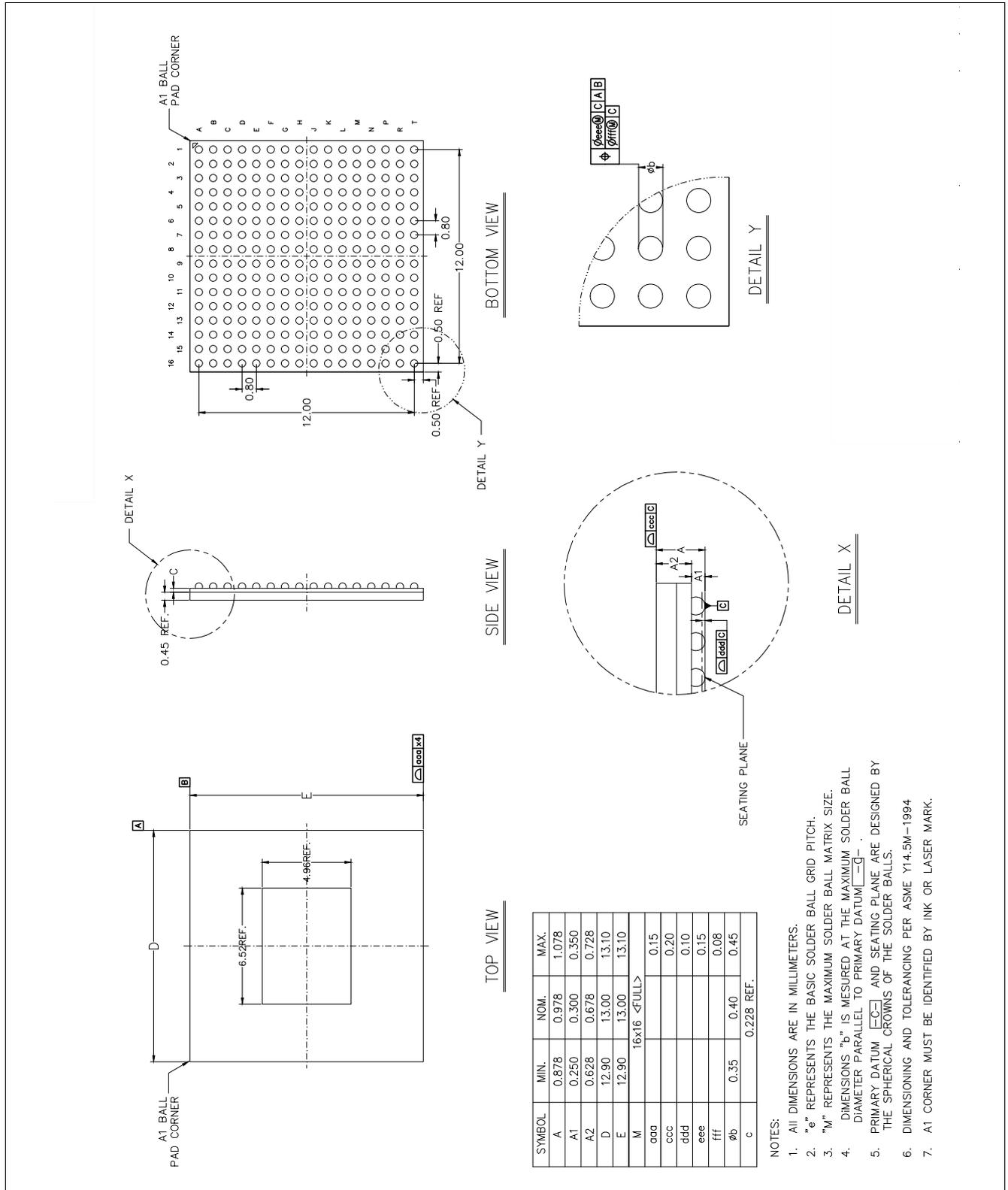


Figure 27 PG-FCLBGA-256 13 mm x 13 mm Package Outline

9 Product Ordering Information

Table 58 provides the product ordering information.

Table 58 Product and Package Naming

| Marketing Part Number | Ordering Part Number | Package | Device Number ¹⁾ | Device Revision Number ²⁾ | PHY Identifier ³⁾ |
|-----------------------|----------------------|---------------|-----------------------------|--------------------------------------|------------------------------|
| MxL86289C | MXL86289C-ABE-R | PG-FCLBGA-256 | 0x14 | 0x8 | 0x5548 |

1) LDN field in CL22 and CL45 registers.

2) LDRN field in CL22 and CL45 registers.

3) PHY Identifier 2 register 16-bit value.

Note: For more information about part numbers, as well as the most up-to-date information and additional information on environmental rating, go to <https://www.maxlinear.com/support/product-change-notification>.

Literature References

- [1] Ethernet PHY MxL862xx API Reference Guide Rev. 1.0 (in preparation)
- [2] Ethernet PHY MxL862xx Configuration User Guide Rev. 1.0 (in preparation)

Attention: Refer to the latest revisions of the documents.

Standards References

- [3] IEEE 802.3-2022: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, IEEE Computer Society, May 2022
<https://standards.ieee.org/ieee/802.3/10422/>
- [4] SyncE Jitter and Wander specification ITU-T G.8262: Timing characteristics of synchronous Ethernet equipment slave clock, Edition 4.0, November 2018
<https://www.itu.int/rec/T-REC-G.8262-201811-I/en>
- [5] IEEE 1588-2008: IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, July 2008
<https://standards.ieee.org/ieee/1588/6825/>
- [6] JEDEC standard, JESD 51: Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device), December 1995
<https://www.jedec.org/standards-documents/docs/jesd-51>
- [7] Universal SXGMII Interface for a Single MultiGigabit Copper Network Port, Revision 2.4, Cisco Systems, July 30th 2019
- [8] Cisco USXGMII Multiport Copper PHY Specification, EDCS-1517762, Version 2.15, May 11th, 2017
- [9] Cisco USXGMII Single-port Copper PHY Specification, EDCS-1150953, Version 2.4, May 23rd 2016
- [10] The I2C-Bus Specification Version 2.1, January 2000
- [11] Negotiated Fast Retrain, Revision 2.0, Cisco Systems, June 10th, 2011
- [12] IEEE 802.1Qbu: Frame Preemption, IEEE 802.1 working group, October 7th 2015
- [13] Microsoft Security Development Lifecycle
<https://www.microsoft.com/en-us/securityengineering/sdl/practices>

Terminology

A

| | |
|------|---------------------------------------|
| ADS | Auto-Downspeed |
| AFE | Analog Front End |
| ANEG | Auto-Negotiation |
| ANSI | American National Standards Institute |
| ASP | Analog Signal Processing |

B

| | |
|----|-----------|
| BW | Bandwidth |
|----|-----------|

C

| | |
|-------|--------------------------|
| Cat 5 | Category 5 Cabling |
| CDB | Clock Distribution Block |
| CDR | Clock and Data Recovery |
| CML | Current Mode Logic |

D

| | |
|------|------------------------------|
| DSP | Digital Signal Processing |
| DWRR | Deficit Weighted Round Robin |

E

| | |
|--------|--|
| EEE | Energy-Efficient Ethernet |
| EEPROM | Electrically Erasable Programmable ROM |
| EMI | Electromagnetic Interference |
| ESD | Electrostatic Discharge |

F

| | |
|-----|--------------------------|
| FCA | Flash Configuration Area |
| FLP | Fast Link Pulse |

G

| | |
|------|-------------------------------------|
| GMII | Gigabit Media-Independent Interface |
| GPIO | General Purpose Input/Output |

H

| | |
|-----|------------------|
| HBM | Human Body Model |
|-----|------------------|

I

| | |
|------------------|--|
| I ² C | Internally Integrated Circuit Interface (also I2C) |
| IC | Integrated Circuit |
| IEEE | Institute of Electrical and Electronics Engineers |

J

| | |
|------|--------------------------|
| JTAG | Joined Test Action Group |
|------|--------------------------|

L

| | |
|-----|----------------------|
| LAN | Local Area Network |
| LED | Light Emitting Diode |

| | |
|----------|-------------------------------------|
| LJPLL | Low Jitter Phase-Locked Loop |
| LPI | Low Power Idle |
| LSB | Least Significant Bit |
| M | |
| MAC | Media Access Controller |
| MDI | Media-Dependent Interface |
| MDIO | Management Data Input/Output |
| MDIX | Media-Dependent Interface Crossover |
| MMD | MDIO Manageable Device |
| MSB | Most Significant Bit |
| N | |
| NLP | Normal Link Pulse |
| O | |
| OSI | Open Systems Interconnection |
| OUI | Organizationally Unique Identifier |
| P | |
| PCB | Printed Circuit Board |
| PCS | Physical Coding Sublayer |
| PD | Power Down |
| PHY | Physical Layer (device) |
| PLL | Phase-Locked Loop |
| PMA | Physical Media Attachment |
| PPS | Pulse Per Second |
| PTP | Precision Time Protocol |
| PTS | Precision Time Stamping |
| Q | |
| QSPI | Quad Serial Peripheral Interface |
| R | |
| Rx | Receive |
| S | |
| SerDes | Serializer-Deserializer |
| SFP | Small Form-Factor Pluggable |
| SMD | Surface Mounted Device |
| SoC | System on Chip |
| STA | Station Management Entity (MAC SoC) |
| SVN | Security Version Number |
| T | |
| TLE | Transformerless Ethernet |
| TPG | Test Packet Generator |
| TPI | Twisted Pair Interface |

| | |
|----------|---|
| Tx | Transmit |
| U | |
| USXGMII | Universal Serial Multi(x) Gigabit Media Independent Interface |
| W | |
| WoL | Wake-on-LAN |
| X | |
| XO | Crystal Oscillator |