MxL7218

Data Sheet

Dual 18A or Single 36A Power Module

General Description

The MxL7218 is a dual channel, 18A step-down power module. It includes a wide 4.5V to 15V input voltage range and supports two outputs each with an output voltage range of 0.6V to 1.8V, set by a single external resistor. The MxL7218 requires only a few input and output capacitors, which simplifies design and shortens time-to-market. The module supplies either two 18A outputs, a single 36A output or up to 216A when paralleled with additional MxL7218 modules. A unique package design where inductors are mounted externally and careful component selection result in higher efficiency and extended operating range relative to devices with the same industry standard pinout.

The complete switch mode DC/DC power supply integrates the control, drivers, bootstrap diodes, bootstrap capacitors, inductors, MOSFETs and HF bypass capacitors in a single package for point-of-load conversions.

The MxL7218 includes a temperature diode that enables device temperature monitoring. It also has an adjustable switching frequency and utilizes a peak current mode architecture which allows fast line and load transient response.

A host of protection features, including overcurrent, over-temperature, output overvoltage and UVLO, help this module achieve safe operation under abnormal operating conditions.

The MxL7218 is available in a space saving 16mm x 16mm x 5.01mm RoHS compliant BGA package.

Features

- Dual 18A or single 36A output
- Input voltage range: 4.5V to 15V
- Output voltage range: 0.6V to 1.8V
- Multiphase current sharing with multiple MxL7218s for up to 216A output
- Frequency synchronization
- Differential remote sense amplifier
- Peak current mode architecture for fast transient response
- Adjustable switching frequency (400kHz to 780kHz)
- Overcurrent protection
- Output overvoltage protection
- Internal temperature monitor and thermal shutdown protection
- Thermally enhanced 16mm x 16mm x 5.01mm BGA package

Applications

- Telecom and Networking Equipment
- Industrial Equipment
- Test Equipment

Ordering Information - page 32

Typical Application

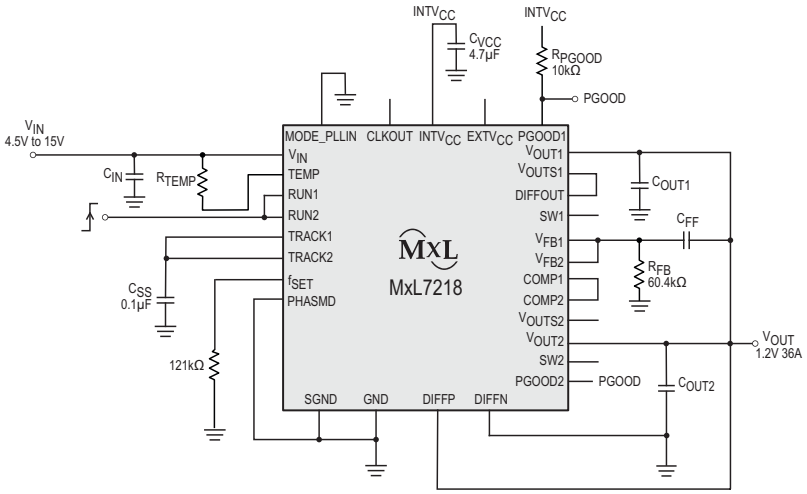

Figure 1: Typical Application: 36A, 1.2V Output DC/DC Power Module

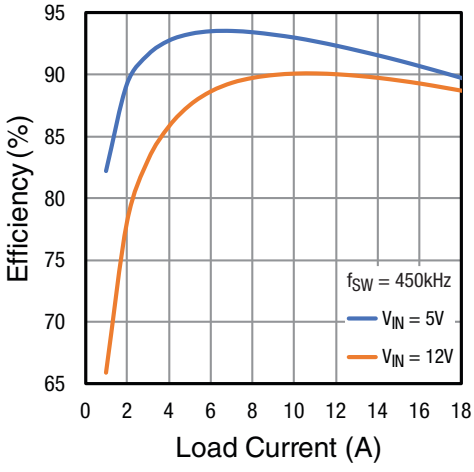

Figure 2: $1.2V_{OUT}$ Efficiency vs I_{OUT}

Revision History

Document No.	Release Date	Change Description
202DSR02	June 9, 2021	**Updated:** ■ "Mechanical Dimensions, BGA" figure. ■ "Recommended Land Pattern and Stencil, BGA" figure. ■ Disclaimer text.
202DSR01	September 29, 2021	Initial release.

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Specifications

Absolute Maximum Ratings

Important: Stress above what is listed in Table 1 may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed in Table 1 or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above what is listed in Table 3 for extended periods of time may affect device reliability. Solder reflow profile is specified in the IPC/JEDEC J-STD-020C standard.

Table 1: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
V_{IN}	-0.3	18	V
V_{SW1}, V_{SW2}	-1	25	V
PGOOD1, PGOOD2, COMP1, COMP2	-0.3	6	V
$INTV_{CC}$, $EXTV_{CC}$	-0.3	6	V
MODE/PLLIN, f_{SET}, TRACK1, TRACK2	-0.3	$INTV_{CC}$	V
DIFFOUT	-0.3	$INTV_{CC}$ - 1.1V	V
PHASMD	-0.3	$INTV_{CC}$	V
V_{OUT1}, V_{OUT2}, V_{OUTS1}, V_{OUTS2}	-0.3	6	V
DIFFP, DIFFN	-0.3	$INTV_{CC}$	V
RUN1, RUN2, V_{FB1}, V_{FB2}	-0.3	$INTV_{CC}$	V
$INTV_{CC}$ Peak Output Current		100	mA
Storage Temperature Range	-65	150	°C
Peak Package Body Temperature		245	°C

ESD Ratings

Table 2: ESD Ratings

Parameter	Limit	Units
HBM (Human Body Model)	2k	V
CDM (Charged Device Model)	500	V

Operating Conditions

Table 3: Operating Conditions

Parameter	Minimum	Maximum	Units
V_{IN}	4.5	15	V
$INTV_{CC}$	4.5	5.5	V
$EXTV_{CC}$	4.7	5.5	V
PGOOD1, PGOOD2	0	5.5	V
Switching Frequency	400	780	kHz
Junction Temperature Range (T_J)	-40	125	°C
Thermal Resistance from Junction to Ambient (Θ_{JA})		7	°C/W
Thermal Resistance from Junction to PCB (Θ_{JB})		1.5	°C/W
Thermal Resistance from Junction to Top of Module Case (Θ_{JCtop})		3.86	°C/W

Electrical Characteristics

Specifications are for Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = 12V and V_{RUN1}, V_{RUN2} = 5V. Per Figure 17.

Table 4: Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DC Specifications							
$V_{IN(DC)}$	Input DC voltage		•	4.5		15	V
$V_{OUT1(RANGE)}$ $V_{OUT2(RANGE)}$	Output DC range		•	0.6		1.8	V
$V_{OUT1\ (DC)}$ $V_{OUT2\ (DC)}$	V_{OUT} total variation with line and load	C_{IN} = 22 µF x 3 C_{OUT} = 100µF MLCC, 470µF POSCAP, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A to 18A	•	1.477	1.5	1.523	V
Input Specifications							
V_{RUN1}, V_{RUN2}	RUN pin on/off threshold	RUN rising		1.1	1.25	1.4	V
$V_{RUN1HYS}$, $V_{RUN2HYS}$	RUN pin ON hysteresis				168		mV
$I_{INRUSH(VIN)}$	Input inrush current at start-up	I_{OUT} = 0A, C_{IN} = 3 x 22µF, C_{SS} = 0.01µF, C_{OUT} = 3 x 100µF, V_{OUT1} = 1.5V, V_{OUT2} = 1.5V, V_{IN} = 12V			1		A
$I_{Q(VIN)}$	Input supply bias current	V_{IN} = 12V, V_{OUT1} = 1.5V, V_{RUN2} = 0V, pulse-skipping mode			4.9		mA
		V_{IN} = 12V, V_{OUT1} = 1.5V, V_{RUN2} = 0V, 500kHz CCM			52		mA
		Shutdown, RUN = 0, V_{IN} = 12V			57		µA
$I_{S(VIN)}$	Input supply current	V_{IN} = 5V, V_{OUT1} = 1.5V, I_{OUT1} = 18A, V_{RUN2} = 0V			6		A
		V_{IN} = 12V, V_{OUT1} = 1.5V, I_{OUT1} = 18A, V_{RUN2} = 0V			2.5		A
Output Specifications							
$I_{OUT1(DC)}$, $I_{OUT2(DC)}$	Output continuous current range(1)	V_{IN} = 12V, V_{OUT} = 1.5V		0		18	A
$\Delta V_{OUT1(LINE)}/V_{OUT1}$ $\Delta V_{OUT2(LINE)}/V_{OUT2}$	Line regulation accuracy	V_{OUT} = 1.5V, V_{IN} from 4.5V to 15V I_{OUT} = 0A for each output	•		0.01	0.025	%/V
$\Delta V_{OUT1(LOAD)}/V_{OUT1}$ $\Delta V_{OUT2(LOAD)}/V_{OUT2}$	Load regulation accuracy(1)	Each output; V_{OUT} = 1.5V, 0A to 18A, V_{IN} = 12V	•		0.5	0.75	%
$V_{OUT1(AC)}$, $V_{OUT2(AC)}$	Output ripple voltage	For each output; I_{OUT} = 0A, C_{OUT} = 100µF x 3 / X7R / ceramic, 470µF POSCAP, V_{IN} = 12V, V_{OUT} = 1.5V, frequency = 450kHz			12		mV_{PP}
f_S (each channel)	Output ripple voltage frequency(2)	V_{IN} = 12V, V_{OUT} = 1.5V, f_{SET} = 1.2V			500		kHz
f_{SYNC} (each channel)	SYNC capture range			400		780	kHz

Table 4: Electrical Characteristics (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$\Delta V_{OUT1START}$ $\Delta V_{OUT2START}$	Turn-on overshoot	C_{OUT} = 100µF / X5R / ceramic, 470µF POSCAP, V_{OUT} = 1.5V, I_{OUT} = 0A, V_{IN} = 12V Each channel			0		mV
t_{START1}, t_{START2}	Turn-on time	C_{OUT} = 100µF / X5R / ceramic, 470µF POSCAP, No load, TRACK/SS with 0.01µF to GND, V_{IN} = 12V Each channel			5		ms
$\Delta V_{OUT(LS)}$ (Each channel)	Peak deviation for dynamic load	Load: 0% to 50% to 0% of full load, C_{OUT} = 22µF x3 / X5R / Ceramic, 470µF POSCAP V_{IN} = 12V, V_{OUT} = 1.5V			30		mV
t_{SETTLE} (Each channel)	Settling time for dynamic load step	Load: 0% to 50% to 0% of full load, V_{IN} = 12V, C_{OUT} = 100µF, 470µF POSCAP			20		µs
$I_{OUT1(PK)}$ $I_{OUT2(PK)}$	Output current limit	V_{IN} = 12V, V_{OUT} = 1.5V Each channel			30		A
Control Section							
V_{FB1}, V_{FB2}	Voltage at V_{FB} pins	I_{OUT} = 0A, V_{OUT} = 1.2V	•	0.592	0.600	0.606	V
I_{FB}	Current at V_{FB} pins				–5	–20	nA
V_{OVL}	Feedback overvoltage lockout		•	0.64	0.66	0.68	V
TRACK1 (I), TRACK2 (I)	Track pin soft-start pull-up current	TRACK1 (I), TRACK2 (I) start at 0V		1	1.25	1.5	µA
UVLO	Undervoltage lockout	V_{IN} falling			3.6		V
		V_{IN} rising			4.2		V
UVLO hysteresis					0.6		V
$t_{ON(MIN)}$	Minimum on-time				90		ns
R_{FBHI1}, R_{FBHI2}	Resistance between V_{OUTS1}, V_{OUTS2} and V_{FB1}, V_{FB2}	Each output		60.05	60.4	60.75	kΩ
$V_{PGOOD1\ LOW}$, $V_{PGOOD2\ LOW}$	PGOOD voltage low	I_{PGOOD} = 2mA			34	300	mV
I_{PGOOD}	PGOOD leakage current	V_{PGOOD} = 5V				5	µA
V_{PGOOD}	PGOOD trip level	V_{FB} with respect to its steady state value V_{FB} ramping negative			–10		%
		V_{FB} with respect to its steady state value V_{FB} ramping positive			10		

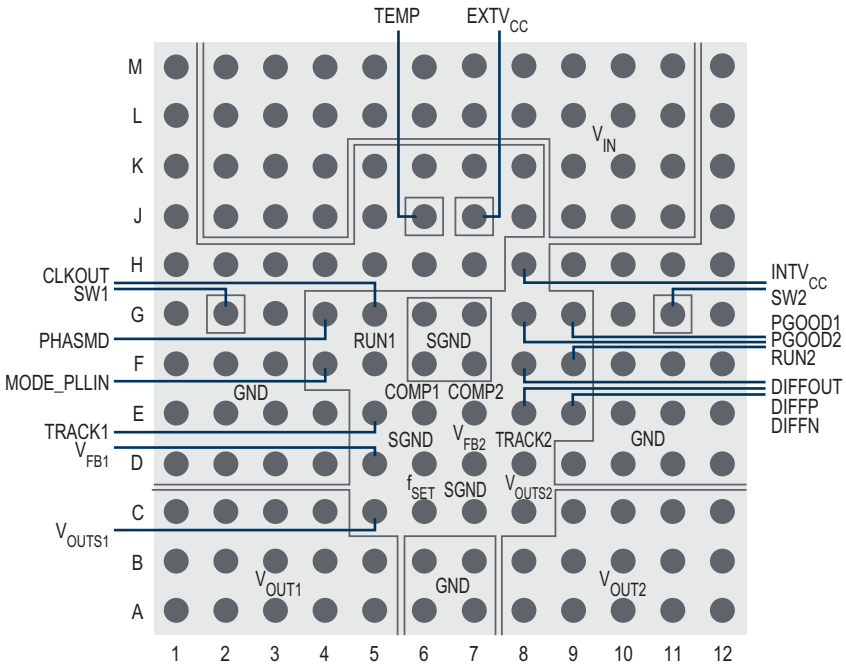
Table 4: Electrical Characteristics (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} voltage	6V < V_{IN} < 15V		4.8	5	5.2	V
V_{INTVCC} load regulation	$INTV_{CC}$ load regulation	I_{CC} = 0mA to 50mA			1	2	%
V_{EXTVCC}	$EXTV_{CC}$ switchover voltage	$EXTV_{CC}$ ramping positive		4.5	4.7		V
$V_{EXTVCC(DROP)}$	$EXTV_{CC}$ dropout	I_{CC} = 20mA, V_{EXTVCC} = 5V			50	100	mV
$V_{EXTVCC(HYST)}$	$EXTV_{CC}$ hysteresis				150		mV
Oscillator and Phase-Locked Loop							
Frequency nominal	Nominal frequency	f_{SET} = 1.2V		450	500	550	kHz
Frequency low	Lowest frequency	f_{SET} = 0V		210	250	290	kHz
Frequency high	Highest frequency	f_{SET} > 2.4V, up to $INTV_{CC}$		700	780	860	kHz
I_{FSET}	Frequency set current			9	10	11	µA
R_{MODE_PLLIN}	MODE_PLLIN input resistance				250		kΩ
CLKOUT	Phase (relative to SW1)	PHASMD = GND			60		Deg
		PHASMD = float			90		Deg
		PHASMD = $INTV_{CC}$			120		Deg
CLK high	Clock High output voltage			2			V
CLK low	Clock Low output voltage					0.2	V
Differential Amplifier							
A_V	Gain				1		V/V
R_{IN}	Input resistance	Measured at DIFFP Input			82		kΩ
V_{OS}	Input offset voltage	V_{DIFFP} = $V_{DIFFOUT}$ = 1.5V, $I_{DIFFOUT}$ = 100µA				3	mV
PSRR	Power Supply Rejection Ratio	5V < V_{IN} < 15V			90		dB
I_{CL}	Maximum Output current				3		mA
$V_{DIFFOUT(MAX)}$	Maximum output voltage	$I_{DIFFOUT}$ = 300µA		$INTV_{CC}$ - 1.4			V
GBW	Gain Bandwidth Product				2.7		MHz
V_{TEMP}	Diode Connected PNP	I = 100µA			0.6		V
TC_{VTEMP}	Temperature Coefficient	I = 25µA	•		–2.1		mV/°C
OT	Thermal shutdown threshold	Rising temperature			145		°C
	Thermal hysteresis				15		°C

1. See output current derating curves for different V_{IN}, V_{OUT} and T_A.
2. The MxL7218 module is designed to operate from 400kHz to 780kHz.

Pin Information

Pin Configuration



BGA, Top View
144-Lead 16mm x 16mm x 5.01mm

Figure 3: Pin Configuration

Pin Description

Table 5: Pin Description

Pin Number	Pin Name	Description
A1, A2, A3, A4, A5, B1, B2, B3, B4, B5, C1, C2, C3, C4	V_{OUT1}	Output of the channel 1 power stage. Connect the corresponding output load from the V_{OUT1} pins to the PGND pins. Direct output decoupling capacitance from V_{OUT1} to PGND is recommended.
A6, A7, B6, B7, D1, D2, D3, D4, D9, D10, D11, D12, E1, E2, E3, E4, E10, E11, E12, F1, F2, F3, F10, F11, F12, G1, G3, G10, G12, H1, H2, H3, H4, H5, H6, H7, H9, H10, H11, H12, J1, J5, J8, J12, K1, K5, K6, K7, K8, K12, L1, L12, M1, M12	GND	Ground for the power stage. Connect to the application's power ground plane.

Table 5: Pin Description (Continued)

Pin Number	Pin Name	Description
A8, A9, A10, A11, A12, B8, B9, B10, B11, B12, C9, C10, C11, C12	V_{OUT2}	Output of the channel 2 power stage. Connect the corresponding output load from the V_{OUT2} pins to the PGND pins. Direct output decoupling capacitance from V_{OUT2} to PGND is recommended.
C5, C8	V_{OUTS1}, V_{OUTS2}	These pins are connected internally to the top of the feedback resistor for each output. Connect this pin directly to its specific output or to DIFFOUT when using the remote sense amplifier. When paralleling modules, connect one of the VOUTS pins to DIFFOUT when remote sensing or directly to VOUT when not remote sensing. These pins must be connected to either DIFFOUT or VOUT. This connection provides the feedback path and cannot be left open.
C6	f_{SET}	This pin is used to set the operating frequency via one of two methods: ■ Connect a resistor from this pin to ground ■ Drive this pin with a DC voltage This pin sources a 10µA current. See Figure 22 for frequency of operation vs. f_{SET} voltage.
C7, D6, G6, G7, F6, F7	SGND	Ground pin for all analog signals and low power circuits. Connect to GND in one place. See layout guidelines in Figure 34.
D5, D7	V_{FB1}, V_{FB2}	Feedback input to the negative side of the error amplifier for each channel. These pins are each internally connected to V_{OUTS1} and V_{OUTS2} via a precision 60.4kΩ resistor. Vary each output voltage by adding a feedback resistor from V_{FB} to SGND. Tie V_{FB1} and V_{FB2} together for parallel operation.
E5, D8	TRACK1, TRACK2	Soft-Start and Output Voltage Tracking pins. Each channel has a 1.25µA pull-up current source. When one channel is configured as a master, adding a capacitor from this pin to ground sets a soft-start ramp rate. The other channel can be set up as the slave and have the master output applied through a voltage divider to the slave's output TRACK pin. For coincidental tracking, this voltage divider is equal to the slave's output feedback divider.
E6, E7	COMP1, COMP2	Current control threshold and error amplifier compensation point for each channel. The current comparator threshold increases with this control voltage. The MxL7218 is internally compensated, however a feed-forward C_{FF} is frequently required. Refer to Figure 17, Table 7 and Stability and Compensation in the Applications Information section. When paralleling both channels, connect the COMP1 and COMP2 pins together.
E8	DIFFP	This pin is the remote sense amplifier's positive input and is connected to the output voltage's remote sense point. If the remote sense amplifier is not used, connect this pin to SGND.
E9	DIFFN	This pin is the remote sense amplifier's negative input and is connected to the remote sense point GND. If the remote sense amplifier is not used, connect this pin to SGND.
F4	MODE_PLLIN	Selects between Forced Continuous Mode or Pulse-Skipping Mode, or connects to an external clock for frequency synchronization. There are three connection options: 1. Connect this pin to SGND to force both channels into Forced Continuous Mode. 2. Connect this pin to $INTV_{CC}$ or leave it floating to enable Pulse-Skipping Mode. 3. Connect this pin to an external clock. Both channels will be synchronized to the clock and operate in Forced Continuous Mode.
F5, F9	RUN1, RUN2	The RUN1 and RUN2 pins each enable and disable their corresponding channel. A voltage above 1.27V on the RUN pin will turn on the corresponding channel. The RUN pin has a hysteresis of about 170mV. There are two supported methods to drive the RUN pin. Either drive it with a logic signal or connect it to a voltage divider whose upper resistor is connected to V_{IN} and lower resistor to ground. See Applications Information for important details.
F8	DIFFOUT	Output of the internal remote sense amplifier. If remote sensing on channel 1, connect to V_{OUTS1}. If remote sensing on channel 2, connect to V_{OUTS2}. When paralleling modules, connect one of the VOUTS pins to DIFFOUT when remote sensing.

Table 5: Pin Description (Continued)

Pin Number	Pin Name	Description
G2, G11	SW1, SW2	Use these pins to access the switching node of each channel. An RC snubber can be connected to reduce switch node ringing. Otherwise, leave these pins floating.
G4	PHASMD	This pin selects the CLKOUT phase as follows: ■ Connect to SGND for 60 degrees ■ Connect to $INTV_{CC}$ for 120 degrees ■ Leave floating for 90 degrees
G5	CLKOUT	This is the clock output. Its phase is set with the PHASMD pin. It is used to synchronize multiple modules so that all channels evenly share load current and operate in a multiphase manner. Refer to the Application Section on Multiphase Operation for more details.
G9, G8	PGOOD1, PGOOD2	Power Good outputs. This open-drain output is pulled low when the V_{OUT} of its respective channel is more than ±10% outside regulation.
H8	$INTV_{CC}$	Internal 5V Regulator Output. This voltage powers the control circuits and internal gate driver. Decouple to GND with a 4.7µF ceramic capacitor. $INTV_{CC}$ is activated when either RUN1 or RUN2 is activated.
J6	TEMP	The internal temperature sensing diode monitors the temperature change with voltage change on V_{BE}. Connect to V_{IN} through a resistor (R_{TEMP}) to limit the current to 100µA. $R_{TEMP} = (V_{IN} - 0.6V) / 100\mu A$
J7	$EXTV_{CC}$	External power input that is connected through an internal switch to $INTV_{CC}$ whenever $EXTV_{CC}$ is > 4.7V. Do not exceed 6V on this input. Connect this pin to V_{IN} when operating V_{IN} on 5V. An efficiency increase that is a function of (V_{IN} - $INTV_{CC}$) multiplied by the power MOSFET driver current occurs when the feature is used. V_{IN} must be applied before $EXTV_{CC}$, and $EXTV_{CC}$ must be removed before V_{IN}.
M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, L2, L3, L4, L5, L6, L7, L8, L9, L10, L11, J2, J3, J4, J9, J10, J11, K2, K3, K4, K9, K10, K11	V_{IN}	Power input pins. Connect input voltage between these pins and GND. Direct input decoupling capacitance from V_{IN} to GND is recommended.

1. Use test points to monitor signal pin connections.

Typical Performance Characteristics

Efficiency

See Figure 17 for typical application schematic.

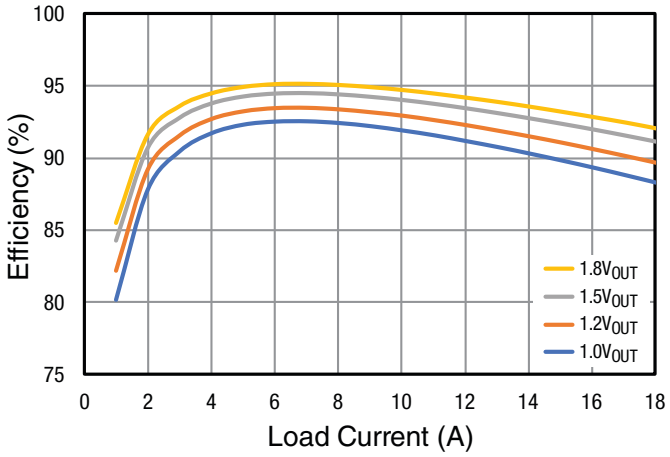


Figure 4: Efficiency: Single Phase, V_{IN} = 5V, 450kHz

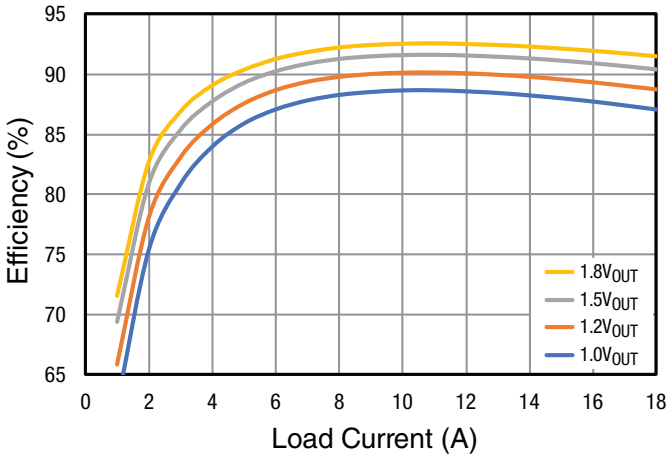


Figure 5: Efficiency: Single Phase, V_{IN} = 12V, 450kHz

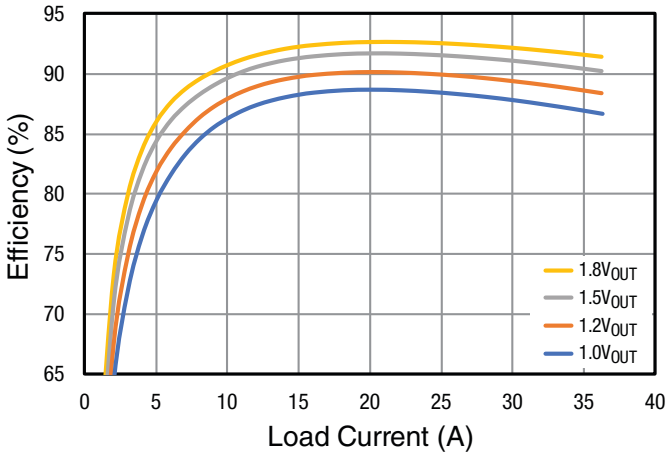


Figure 6: Efficiency: Dual Phase, V_{IN} = 12V, 450kHz

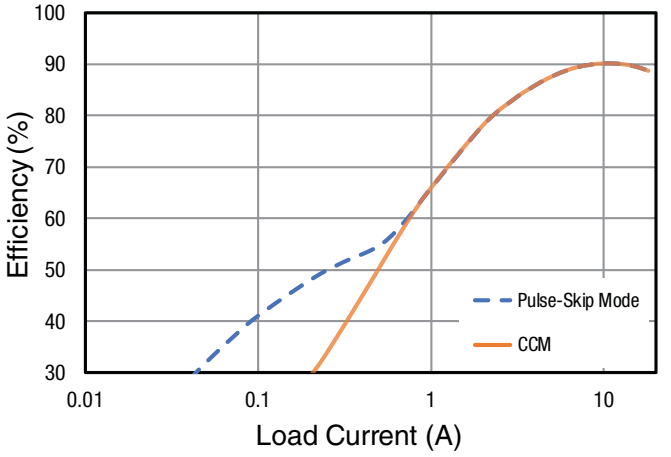
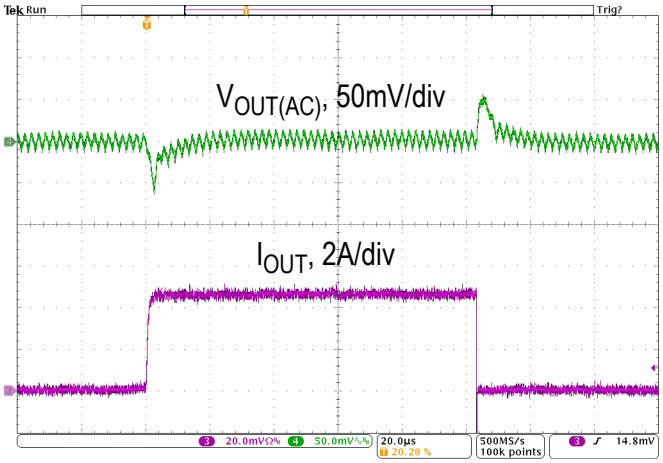


Figure 7: Efficiency: Pulse-Skipping Mode, V_{IN} = 12V, V_{OUT} = 1.2V, 450kHz

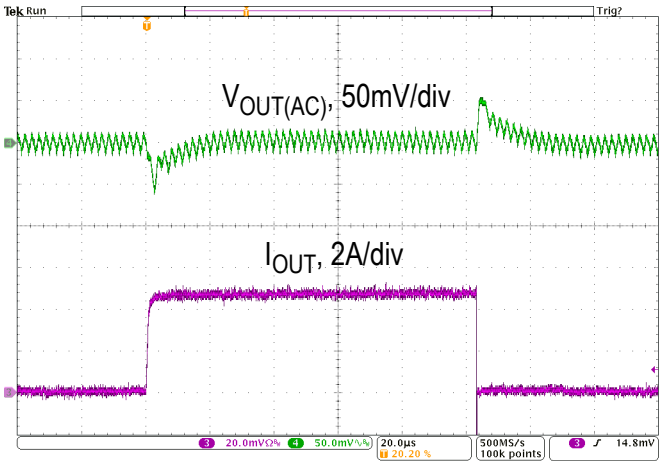
Load Transient Response, Single Phase

See Figure 17 for typical application schematic.



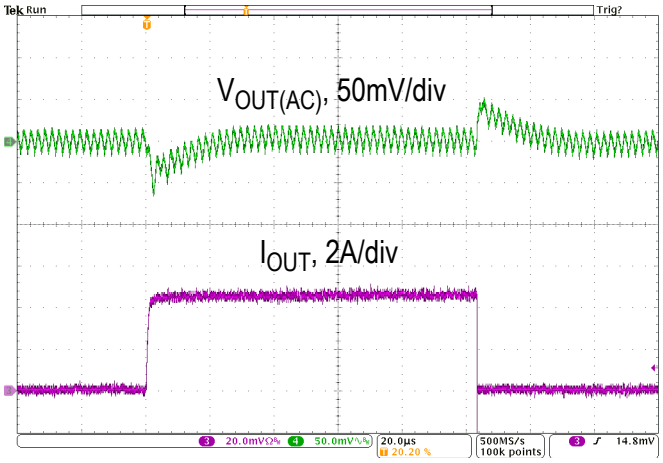
C_{OUT} = 1 x 470µF 4V POSCAP + 1 x 100µF 6.3V Ceramic

Figure 8: 12V to 1V, 450kHz, 4.5A Load Step, 4.5A/µs Step-Up and Step-Down



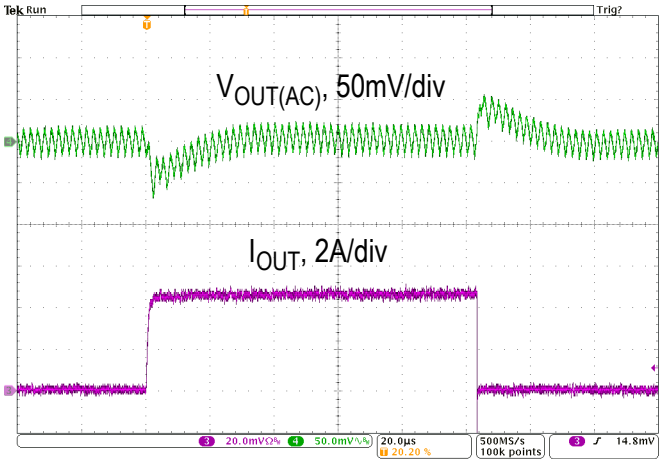
C_{OUT} = 1 x 470µF 4V POSCAP + 1 x 100µF 6.3V Ceramic

Figure 9: 12V to 1.2V, 450 kHz, 4.5A Load Step, 4.5A/µs Step-Up and Step-Down



C_{OUT} = 1 x 470µF 4V POSCAP + 1 x 100µF 6.3V Ceramic

Figure 10: 12V to 1.5V, 450kHz, 4.5A Load Step, 4.5A/µs Step-Up and Step-Down

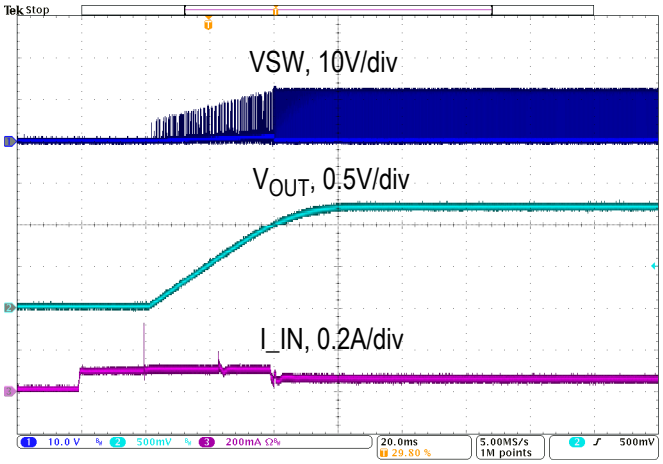


C_{OUT} = 1 x 470µF 4V POSCAP + 1 x 100µF 6.3V Ceramic

Figure 11: 12V to 1.8V, 450kHz, 4.5A Load Step, 4.5A/µs Step-Up and Step-Down

Start-Up, Single Phase

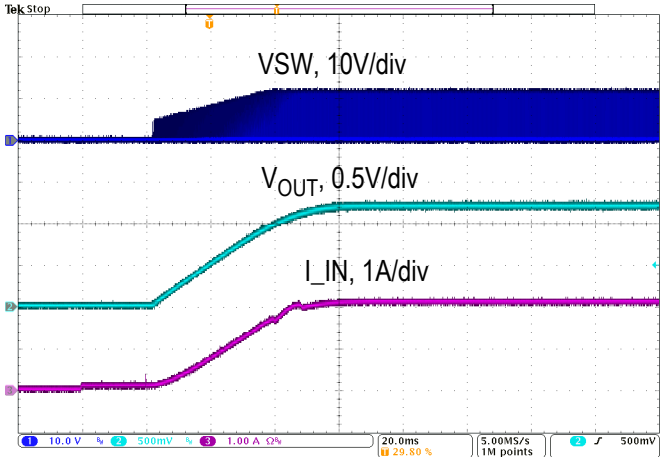
See Figure 17 for typical application schematic.



C_{OUT} = 1 x 470µF POSCAP + 1 x 100µF Ceramic

C_{SS} = 0.1µF

Figure 12: No Load, 12V to 1.2V, 450kHz



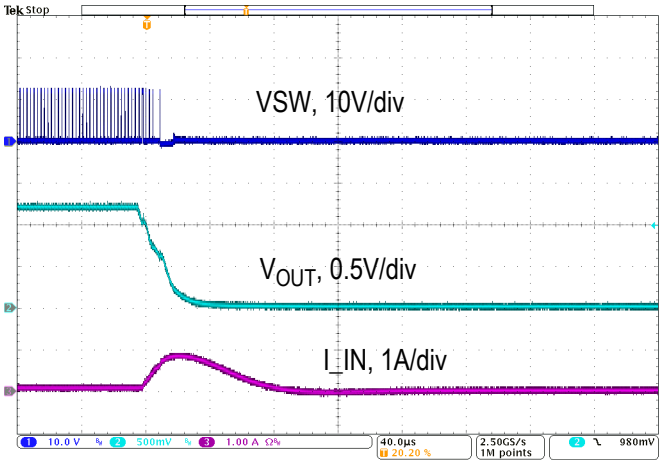
C_{OUT} = 1 x 470µF POSCAP + 1 x 100µF Ceramic

C_{SS} = 0.1µF

Figure 13: 18A, 12V to 1.2V, 450kHz

Short Circuit Protection, Single Phase

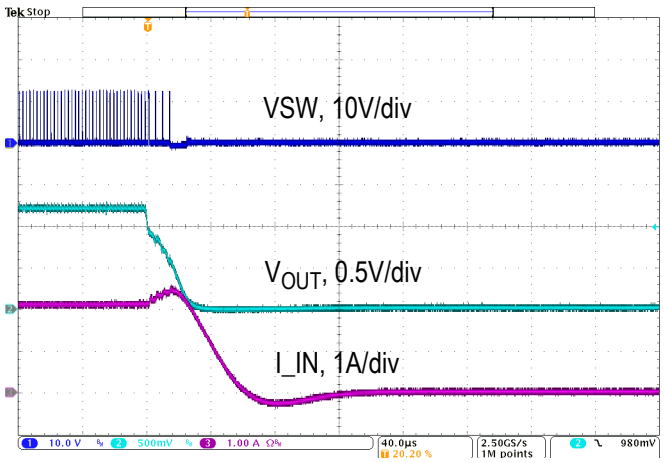
See Figure 17 for typical application schematic.



C_{OUT} = 1 x 470µF POSCAP + 1 x 100µF Ceramic

C_{SS} = 0.1µF

Figure 14: No Load, 12V to 1.2V, 450kHz



C_{OUT} = 1 x 470µF POSCAP + 1 x 100µF Ceramic

C_{SS} = 0.1µF

Figure 15: 18A, 12V to 1.2V, 450kHz

Functional Block Diagram

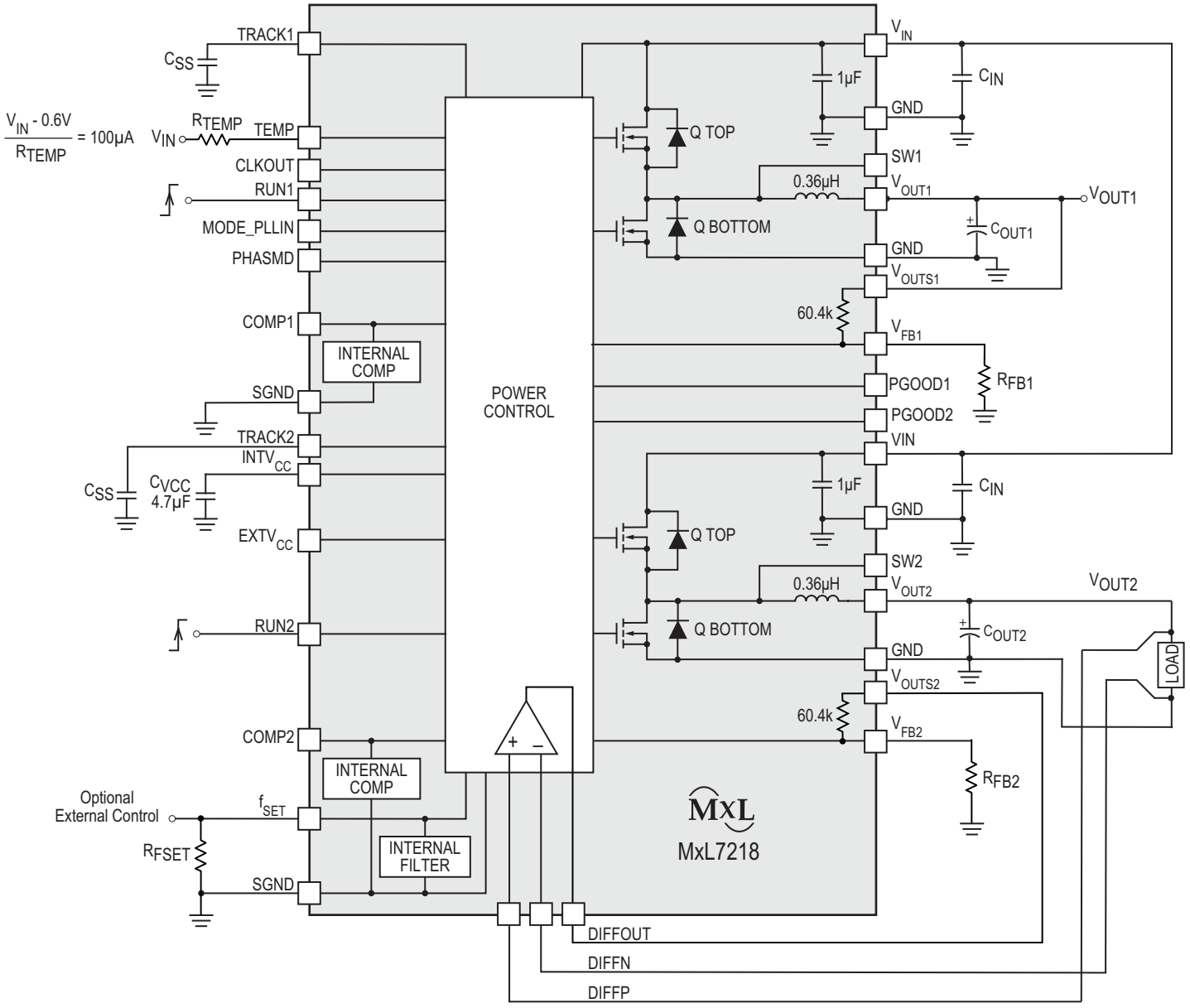


Figure 16: Functional Block Diagram

Operation

Power Module Description

The MxL7218 is a dual-channel, standalone, synchronous step-down power module that provides two 18A outputs or one 36A output. This power module has a continuous input voltage range of 4.5V to 15V and has been optimized for 12V conversions. It provides precisely regulated output voltages from 0.6V to 1.8V that are set by a single external resistor. See the typical application schematic in Figure 17.

The module employs a constant frequency, peak current mode control loop architecture. It also has an internal feedback loop compensation. These features ensure the MxL7218 has sufficient stability margins as well as good transient performance over a wide range of output capacitors, including low ESR ceramic capacitors.

The peak current mode control supports cycle-by-cycle fast current limit and current limit hiccup in overcurrent or output short circuit conditions. The open-drain PGOOD outputs are pulled low when the output voltage exceeds ±10% of its set point. Once the output voltage exceeds +10%, the high side MOSFET is kept off while the low side MOSFET turns on, clamping the output voltage. The overvoltage and undervoltage detection are referenced to the feedback pin.

The RUN1 and RUN2 pins enable and disable the module's two channels. Pulling a RUN pin below 1.1V forces the respective regulator into shutdown mode and turns off both the high side and low side MOSFETs. The TRACK pins are used for either programming the output voltage ramp and voltage tracking during start-up, or for soft-starting the channels.

The MxL7218 includes a differential remote sense amplifier (with a gain of +1). This amplifier can be used to accurately sense the voltage at the load point on one of the module's two outputs or on a single parallel output.

The switching frequency is programmed from 400kHz to 780kHz using an external resistor on the f_{SET} pin. For noise sensitive applications, the module can be synchronized to an external clock.

The MxL7218 module can be configured to current share between channels or can also be set to current share between modules (multiphase or ganged operation). Using the MODE_PLLIN, PHASMD and CLKOUT pins, multiphase operation of up to 12 phases is possible with multiple MxL7218s running in parallel.

Using the MODE_PLLIN pin to operate in pulse-skipping mode results in high efficiency performance at light loads. This light load feature extends battery life.

The $EXTV_{CC}$ pin allows an external 5V supply to power the module and eliminate power dissipation in the internal 5V LDO. $EXTV_{CC}$ has a threshold of 4.7V for activation and a max operating rating of 5.5V. It must sequence on after V_{IN} and sequence off before V_{IN}.

Monitor the internal die temperature by using the TEMP pin. Pull the anode up to V_{IN} through an external resistor to set the bias current in the diode. Thermal simulation has shown that the thermal monitor on the controller die is within 5°C of the MOSFETs.

Applications Information

Typical Application Circuit

The typical MxL7218 application circuit is shown in Figure 17. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 7 for a selection of various design solutions. Additional information about selecting external compensation components can be found in the Stability and Compensation section.

V_{IN} to V_{OUT} Step-Down Ratios

For a given input voltage, there are limitations to the maximum possible V_{IN} and V_{OUT} step-down ratios.

The MxL7218 has a maximum duty cycle of 90% at 500kHz, meaning that the maximum output voltage will be approximately 0.9 x V_{IN}. When running at a high duty cycle, output current can be limited by the power dissipation in the high-side MOSFET. The minimum output voltage from a given input is controlled by the minimum on-time, which is 90ns. The minimum output voltage is either V_{IN} x f_{SW}(MHz) x 0.09µs or 0.6V, whichever is higher. To get a lower output voltage, reduce the switching frequency.

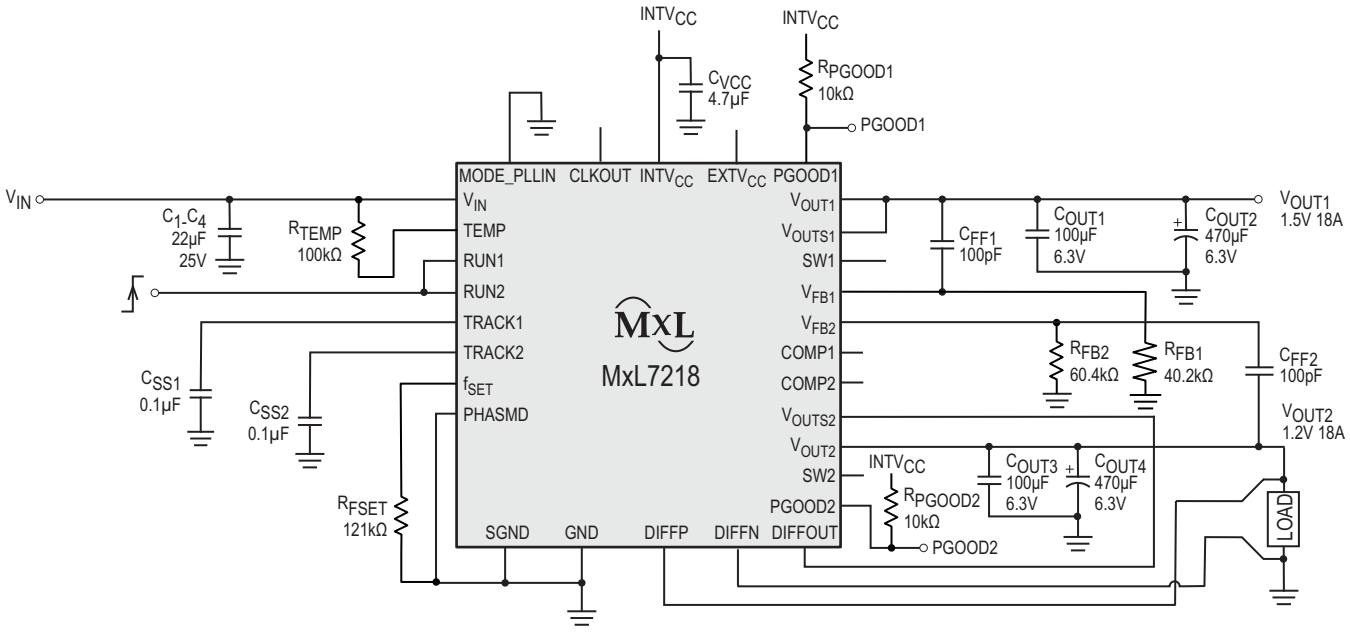


Figure 17: Typical 4.5V_{IN} to 15V_{IN}, 1.5V and 1.2V at 18A Outputs

Output Voltage Programming

The PWM controller has an internal 0.6V reference. A resistor R_{FB} between the V_{FB} and SGND pins programs the output voltage. A 60.4kΩ internal feedback resistor is connected from V_{OUTS1} to V_{FB1} and from V_{OUTS2} to V_{FB2}, as illustrated in the functional block diagram.

R_{FB} values for corresponding standard V_{OUT} values are shown in Table 6. Use the following equation to determine the R_{FB} value for other V_{OUT} levels:

$$R_{FB} = \frac{0.6V \times 60.4k\Omega}{V_{OUT} - 0.6V} \quad \text{Equation 1}$$

In the case of paralleling multiple channels and devices, when all V_{FB} pins are tied together and only one V_{OUTS} pin is connected to the output, a common R_{FB} resistor may be used. Select the R_{FB} as explained above. Note that each V_{FB} pin has an I_{FB} max of 20nA. To reduce V_{OUT} error due to I_{FB}, use an additional R_{FB} and connect the corresponding V_{OUTS} to V_{OUT} as shown in Figure 19.

Table 6: V_{FB} Resistor Table vs. Various Output Voltages

V_{OUT}	0.6V	0.8V	1.0V	1.2V	1.5V	1.8V
R_{FB}	Open	182k	90.9k	60.4k	40.2k	30.2k

Input Capacitors

Use four 22µF ceramic input capacitors to reduce RMS ripple current on the regulator input.

A bulk input capacitor is required if the source impedance is high or the source capacitance is low. For additional bulk input capacitance, use a surface mount 47µF to 100µF aluminum electrolytic bulk capacitor.

Output Capacitors

The output capacitors, denoted as C_{OUT}, need to have low enough equivalent series resistance (ESR) to meet output voltage ripple and transient requirements. The MxL7218 can use low ESR tantalum capacitors, low ESR polymer capacitors, ceramic capacitors or a combination of those for C_{OUT}. Refer to Table 7 for C_{OUT} recommendations that optimize performance for different output voltages.

Pulse-Skipping Mode Operation

The pulse-skipping mode enables the module to skip cycles at light loads which reduces switching losses and increases efficiency at low to intermediate currents. To enable this mode, connect the MODE_PLLIN pin to the $INTV_{CC}$ pin.

Forced Continuous Operation

Forced continuous operation is recommended when fixed frequency is more important than light load efficiency, and when the lowest output ripple is desired. To enable this mode, connect the MODE_PLLIN pin to GND.

Multiphase Operation

Multiphase operation is used to achieve output currents greater than 18A. It can be used with both MxL7218 channels to achieve one 36A output. It can also be used by paralleling multiple MxL7218s and running them out of phase to attain one single high current output, up to 216A. Ripple current in both the input and output capacitors is substantially lower using a multiphase design, especially when the number of phases multiplied by the output voltage is less than the input voltage. Input RMS ripple current and output ripple amplitude is reduced by the number of phases used while the effective ripple frequency is multiplied by the number of phases used. The MxL7218 is a peak current mode controlled device which results in very good current sharing between parallel modules and balances the thermal loading. Figure 18 shows an example of a 2-module, 4-phase, single output regulator that can handle load current up to 70A .

Up to 12 phases can be paralleled by using each MxL7218 channel's PHASMD, MODE_PLLIN and CLKOUT pins. When the CLKOUT pin is connected to the following stage's MODE_PLLIN pin, the frequency and the phase of both devices are locked. Phase difference can be obtained between MODE_PLLIN and CLKOUT of 120 degrees, 60 degrees or 90 degrees respectively by connecting the PHASMD pin to $INTV_{CC}$, SGND or by floating it. Figure 19 shows an example of parallel operation and Figure 20 shows examples of 2-phase, 4-phase and 6-phase designs.

When paralleling multiple channels and devices:

- Tie all V_{FB} pins together.
- Tie all RUN pins together.
- Connect only one of the VOUTS pins to VOUT (or DIFFOUT in the case of remote sensing). In this case, only the R_{FB} corresponding to that VOUTS pin should be populated. Refer to Output Voltage Programming for the calculation of R_{FB}. All other VOUTS pins should be left floating.
- If VOUT offset created by I_{FB} (20nA max per channel) is a concern, additional R_{FB} resistors may be populated to mitigate the effect. In such a configuration, each R_{FB} should be the same resistance value as that in the single R_{FB} case, and the corresponding VOUTS pin should be connected to VOUT (or DIFFOUT in the case of remote sensing).
- If remote sensing, only one differential amplifier should be used.

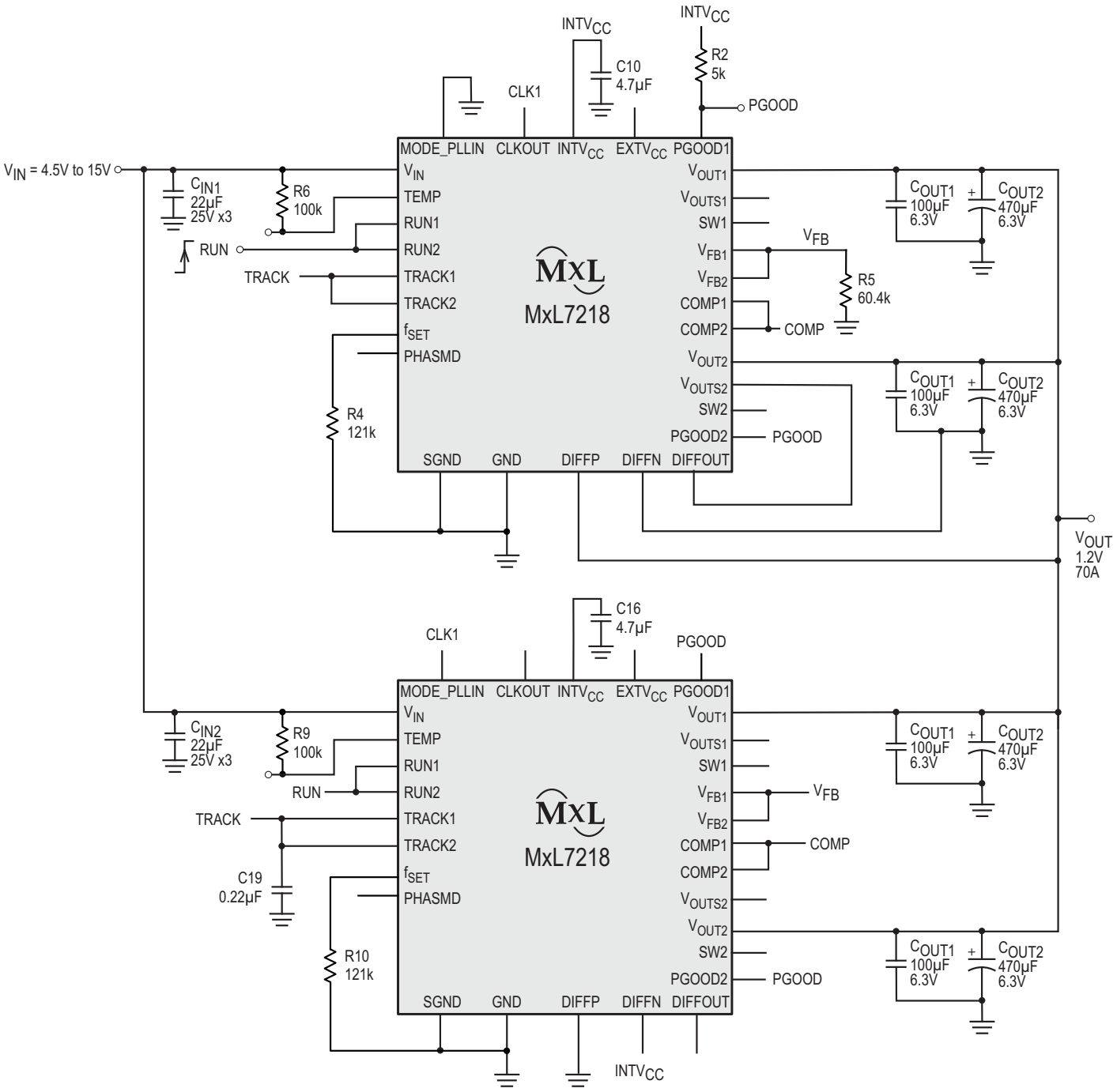


Figure 18: MxL7218 2-Module, 4-Phase, 1.2V, 70A Regulator

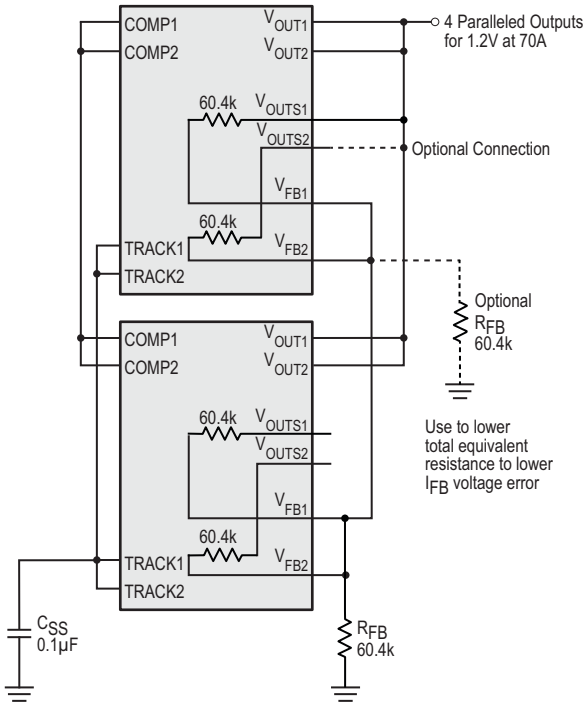
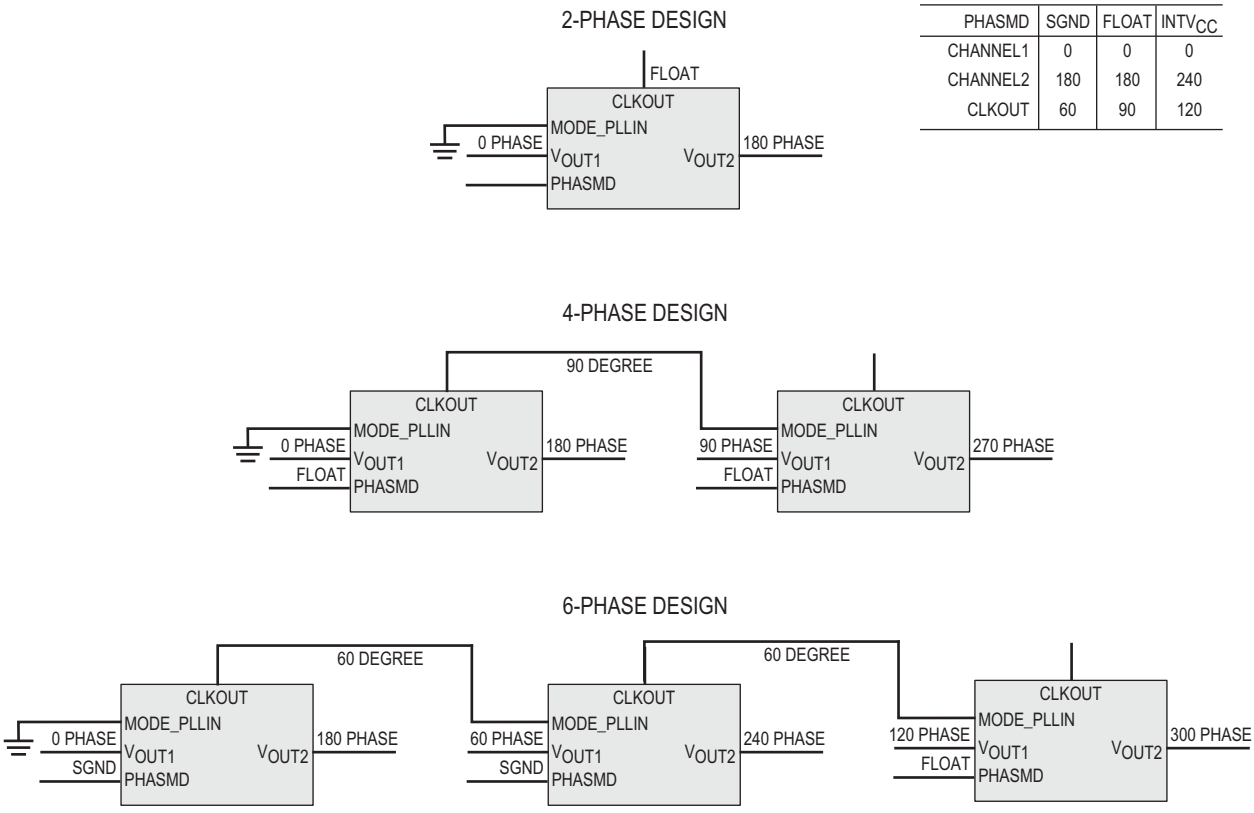


Figure 19: 4-Phase Parallel Configuration



PHASMD	SGND	FLOAT	INTVCC
CHANNEL1	0	0	0
CHANNEL2	180	180	240
CLKOUT	60	90	120

Figure 20: Examples of 2-Phase, 4-Phase and 6-Phase Operation with PHASMD Table

Input Ripple Current Cancellation

Figure 21 illustrates the RMS ripple current reduction that is expected as a function of the number of interleaved phases.

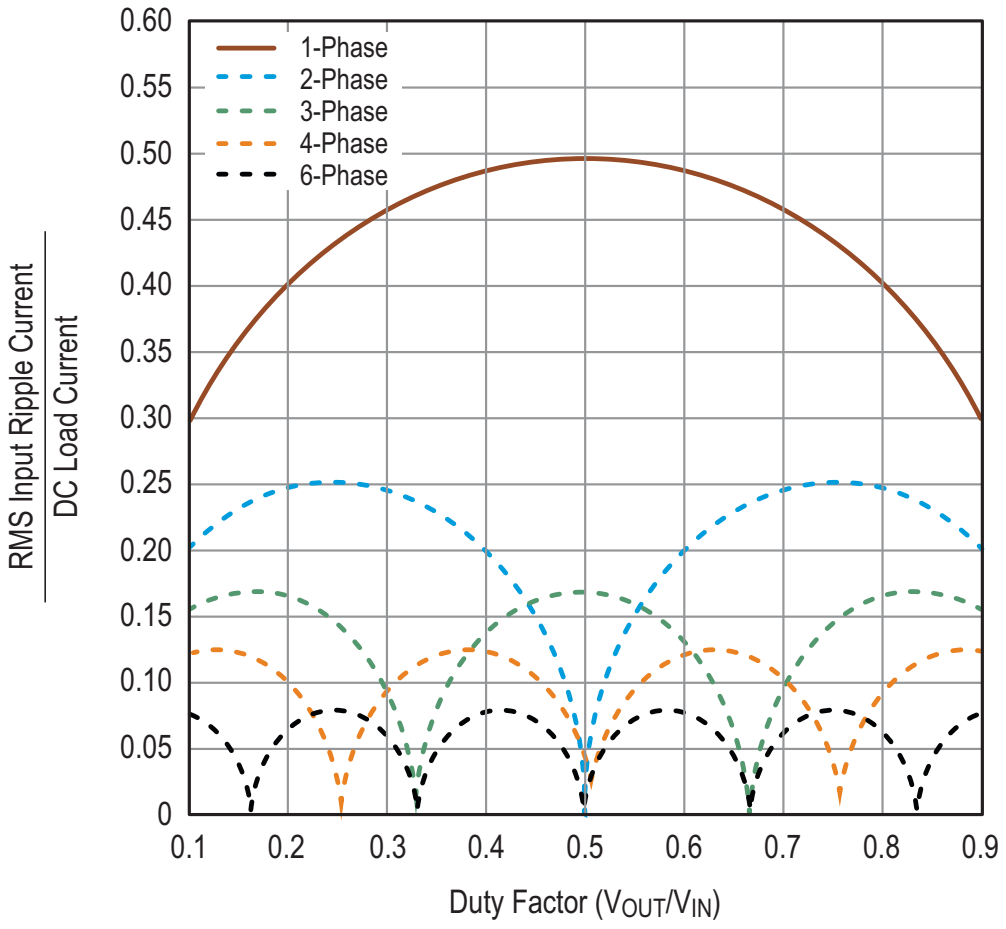


Figure 21: Input RMS Current to DC Load Current Ratio as a Function of Duty Cycle

Frequency Selection and Phase-Locked Loop

To increase efficiency, the MxL7218 works over a range of frequencies. For lower output voltages or duty cycles, lower frequencies are recommended to lower MOSFET switching losses and improve efficiency. For higher output voltages or duty cycles, higher frequencies are recommended to limit inductor ripple current. Refer to the efficiency graphs and their operating frequency conditions. When selecting an operating frequency, keep the highest output voltage in mind.

Use an external resistor between the f_{SET} pin and SGND to set the switching frequency. An accurate 10µA current source into the resistor sets a voltage that programs the frequency. Alternatively, a DC voltage can be applied to f_{SET} to program the frequency. Figure 22 illustrates the operating frequency versus the f_{SET} pin voltage.

An external clock with a frequency range of 400kHz to 780kHz and a voltage range of 0V to $INTV_{CC}$ can be connected to the MODE_PLLIN pin. The high level threshold of the clock input is 1.6V and the low level threshold of the clock input is 1V.

The MxL7218 integrates the PLL loop filter components. Ensure that the initial switching frequency is set with an external resistor before locking to an external clock. Both regulators will operate in continuous mode while being synchronized to an external clock signal.

The PLL phase detector output charges and discharges the internal filter network with a pair of complementary current sources. When an external clock is connected, an internal switch disconnects the external f_{SET} resistor. The switching frequency then locks to the incoming external clock. If no external clock is connected, then the internal switch is on, which connects the external f_{SET} resistor.

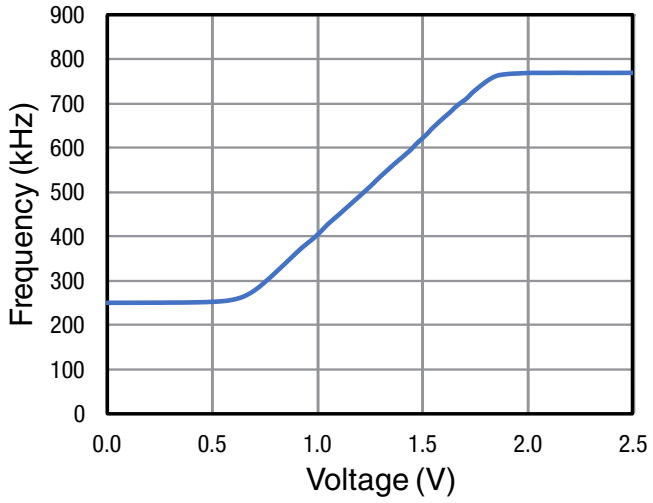


Figure 22: Operating Frequency vs. f_{SET} Pin Voltage

Minimum On-Time

Minimum On-Time $t_{ON(MIN)}$ is the shortest time that the controller can turn on the high-side MOSFET of either channel. Approaching this time may be more of an issue in low duty cycle applications. Use the following equation to make sure the on-time is above this minimum:

$$\frac{V_{OUT}}{V_{IN} \times FREQ} > t_{ON(MIN)} \qquad \text{Equation 2}$$

If the on-time falls below this minimum, the channel will start to skip cycles. In this case, the output voltage continues to regulate, however output ripple increases. Lowering the switching frequency increases on-time. The minimum on-time specified in the electrical characteristics is 90ns.

Soft-Start and Output Voltage Tracking

A capacitor C_{SS} can be connected from the TRACK pin to ground to implement soft-start. The TRACK pin is charged by a 1.25µA current source up to the reference voltage and then on to $INTV_{CC}$. The MxL7218 has a smooth transition from TRACK to V_{OUT} as shown in Figure 23. If the RUN pin is below 1.2V, the TRACK pin is pulled low. The following equation can be used to calculate soft-start time, defined as when PGOOD asserts:

$$t_{SOFTSTART} = \frac{C_{SS}}{1.25\mu A} \times 0.65V \qquad \text{Equation 3}$$

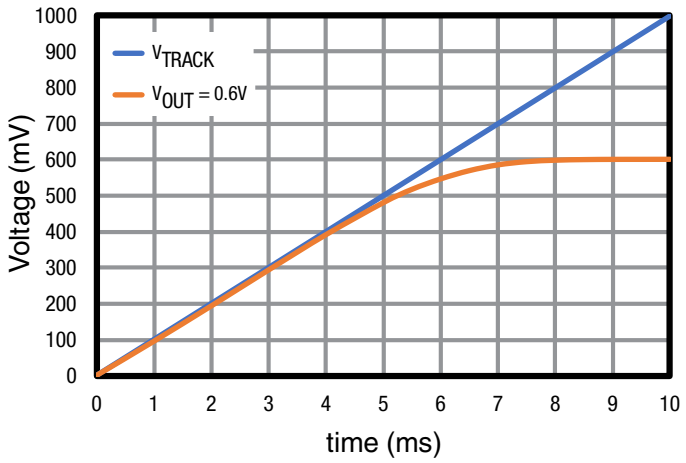


Figure 23: V_{OUT} and V_{TRACK} versus Time

The MODE_PLLIN pin selects between forced continuous mode or pulse-skipping mode during steady-state operation. Regardless of the mode selected, the module channels will always start in the pulse-skipping mode up to TRACK = 0.54V, beyond which point the operation mode will follow the MODE_PLLIN setting.

The TRACK pins can be used to externally program the output voltage tracking. The output may be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. Note that each MxL7218 channel has an internal accurate 60.4kΩ for the top feedback resistor. Refer to the equation below, which is applicable for $V_{TRACK(SLAVE)} < 0.8V$. An example of coincident tracking is shown in Figure 24.

$$V_{OUT(SLAVE)} = \left(1 + \frac{60.4k}{R_{TA}}\right) \times V_{TRACK(SLAVE)} \qquad \text{Equation 4}$$

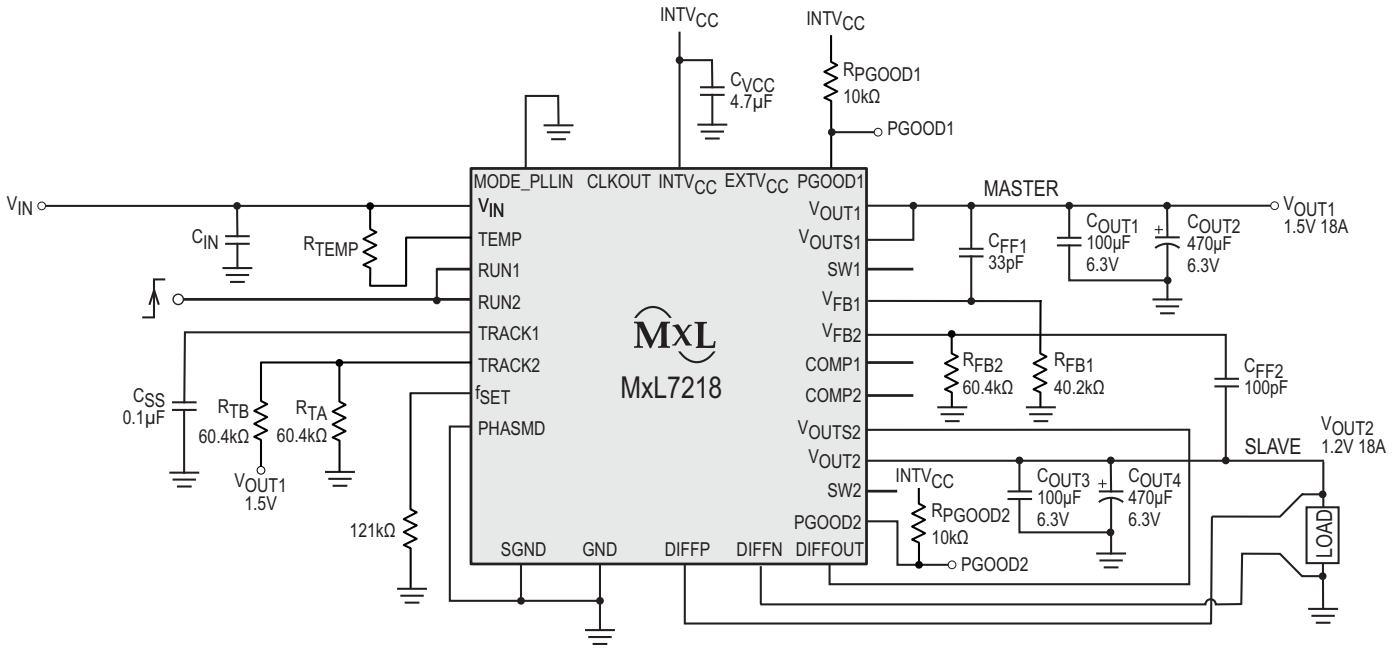


Figure 24: Example of Output Tracking Application Circuit

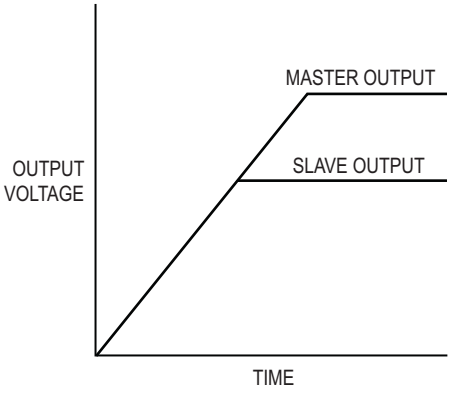


Figure 25: Output Coincident Tracking Waveform

The ramping voltage is applied to the track pin of the slave. Since the same resistor values are used to divide down the output of the master and to set the output of the slave, the slave tracks with the master coincidentally until its final value is achieved. The master continues from the slave's regulation point to its final value. In Figure 24, R_{TA} is equal to R_{FB2} for coincident tracking.

Power Good

Each channel's open drain PGOOD pin can be used to monitor if its respective V_{OUT} is outside ±10% of the set point. The PGOOD pin is pulled low when the output of the corresponding channel is outside the monitoring window, the RUN pin is below its threshold (1.25V), or the MxL7218 is in the soft-start or tracking phase. The PGOOD pin will go high impedance immediately after V_{FB} voltage is within the monitoring window. Note that there is an internal 20µs glitch filtering in PGOOD when V_{FB} voltage goes out of the monitoring window.

If desired, a pullup resistor can be connected from the PGOOD pins to a supply voltage with a maximum level of 6V.

Stability and Compensation

The module is internally compensated for stability over a wide range of operating conditions. Refer to Table 7 for recommended configurations. For other configurations, please consult a Maxlinear Field Applications Engineer.

Enabling Channels

There are two supported methods to enable and disable each channel.

Method 1

Method 1 is to drive the RUNx pin of the channel to be enabled (CHx) with a logic signal as shown in Figure 26.

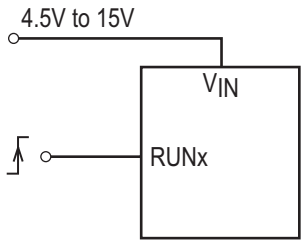


Figure 26: RUNx Pin Driven by a Logic Signal

V_{IN} should be in the operating range (4.5V to 15V) before the logic signal at RUNx goes high. The logic high level must be above 1.3V in order to ensure that the RUNx threshold is crossed. To disable a channel (CHx), the logic signal at the corresponding RUNx pin must be brought down to 1.1V or below.

Method 2

Method 2 is a self-start method. This method uses a resistor divider to divide down V_{IN} and drive the RUNx pin with the divided voltage. The choice of the resistor divider ratio depends on the V_{IN} range.

Figure 27 shows the self-start method for an application where V_{IN} is in the range of 5.5V to 15V.

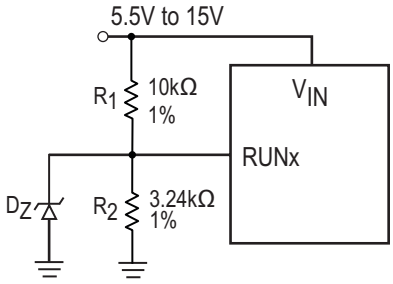


Figure 27: Self-Start for V_{IN} Range of 5.5V to 15V

Resistors R_1 and R_2 divide V_{IN} down and the divided voltage drives the RUNx pin. The R_1 and R_2 values are chosen such that V_{IN} reaches 5V before RUNx crosses the RUN threshold. Equation 5 shows the relationship between R_1, R_2 and $V_{IN(TH)}$ which is the V_{IN} value when the RUNx voltage crosses 1.26V minimum:

$$1 + \frac{R_1}{R_2} = \frac{V_{IN(TH)}}{1.26V} \qquad \text{Equation 5}$$

Select R_1 and R_2 by letting $V_{IN(TH)}$ = 5V.

If the application is for V_{IN} = 12V, the choice of $V_{IN(TH)}$ for Equation 5 can be higher than 5V but less than the minimum of the V_{IN} tolerance band. For example, if V_{IN} is 12V ± 10%, then choose a $V_{IN(TH)}$ between 5V and 10V. A zener diode from RUNx pin to ground is optional for protection of the RUNx pin (to clamp RUNx to 5V) in the event of the R_2 resistor not being connected due to a board level fault.

Figure 28 shows the self-start method for an application where V_{IN} is in the range of 4.5V to 5.5V.

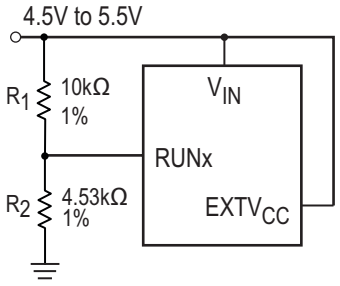


Figure 28: Self-Start for V_{IN} Range of 4.5V to 5.5V

In an application where V_{IN} is the range of 4.5V to 5.5V, it is required to connect V_{IN} to $EXTV_{CC}$. Select R_1 and R_2 based on Equation 5, but use 4V for $V_{IN(TH)}$.

A combination of Method 1 and Method 2 is also recommended where an open drain output drives the RUNx pin with the voltage divider (R_1 and R_2) in place. Criteria for the selection of R_1 and R_2 must be followed as described above.

It is important to note that starting up the channels with RUNx floating is not allowed.

INTV$_{CC}$ and EXTV$_{CC}$

The V_{IN} input voltage powers an internal 5V low dropout linear regulator. The regulator output (INTV$_{CC}$) provides voltage to the control circuitry of the module. Alternatively, the EXTV$_{CC}$ pin allows an external 5V supply to be used to eliminate the 5V LDO power dissipation in power sensitive applications.

Differential Remote Sense Amplifier

The MxL7218's differential remote sense amplifier can be used to accurately sense voltages at the load. This is particularly useful in high current load conditions. The DIFFP and DIFFN pins must be connected properly to the remote load point, and the DIFFOUT pin must be connected to the corresponding V_{OUTS1} or V_{OUTS2} pin. The differential amplifier is able to handle an input up to 3.3V.

If a C_{FF} feed-forward capacitor is desirable in a channel employing the differential amplifier, connect the capacitor between V_{FB} and DIFFP instead of DIFFOUT.

SW Pins

Use the SW pins to monitor the switching node of each channel. These pins are generally used for testing or monitoring. During normal operation, these pins should be unconnected and left floating. However, in conjunction with an external series R-C snubber circuit, these pins can be used to dampen ringing on the switch node caused by LC parasitics in the switched current paths.

Temperature Monitoring (TEMP)

An internal temperature sensing diode / PNP transistor is used to monitor its V_{BE} voltage over temperature, thus serving as a temperature monitor. Its forward voltage and temperature coefficient are shown in the electrical characteristics section and plotted in Figure 29. It is connected to V_{IN} through a pullup resistor R_{TEMP} to limit the current to 100µA. It is recommended to set a 60µA minimum current in applications where V_{IN} varies over a wide range. See Figure 30 for an example on how to use this feature.

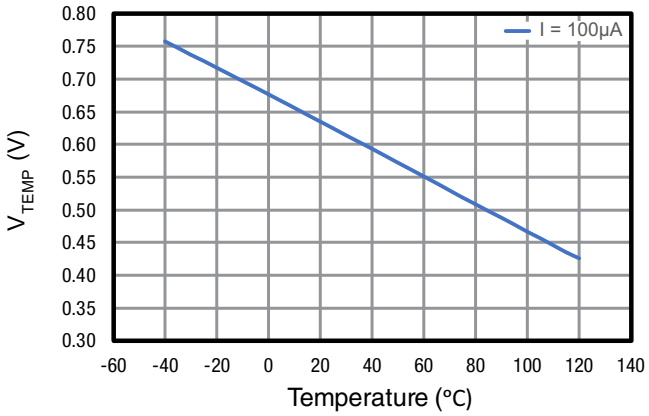


Figure 29: Diode Voltage vs. Temperature

For accurate temperature measurement, the temperature sensing diode should first be characterized in a controlled temperature environment such as an oven. Without powering up the module, push a constant current such as 100µA into the TEMP pin and out the GND. Measure the diode voltage at two extreme temperature points. TEMP voltage vs diode temperature for said current is simply a straight line between those two points.

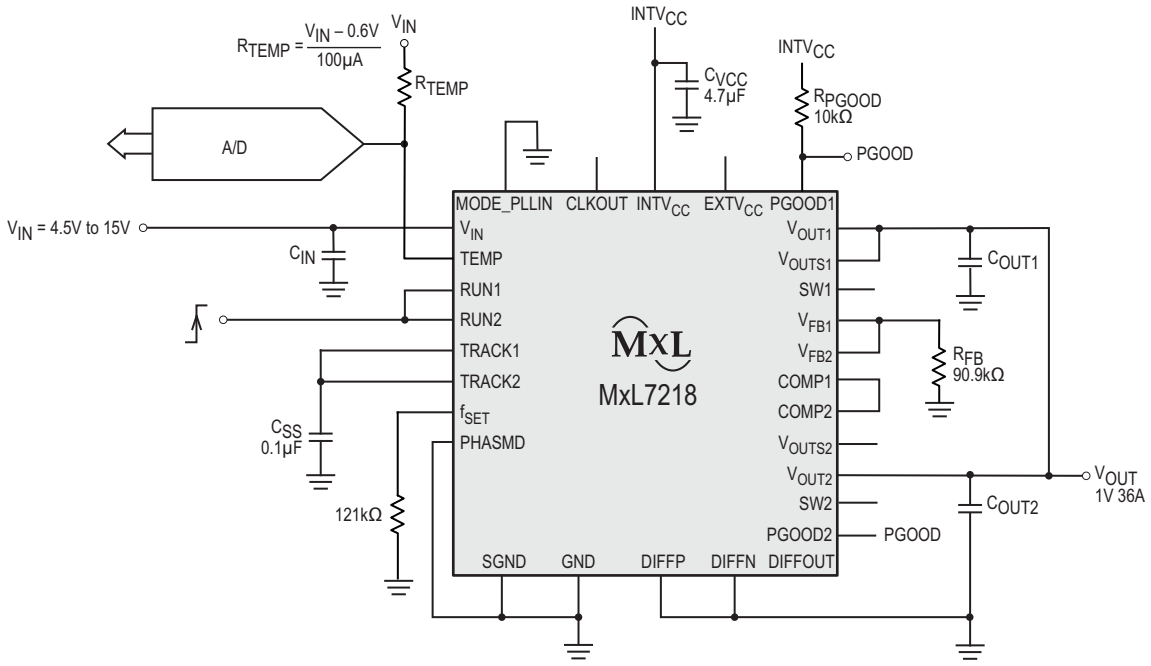


Figure 30: 2-Phase, 1V at 36A with Temperature Monitoring

Fault Protection

The MxL7218 module has built-in overcurrent, output overvoltage, and over-temperature protection.

The overcurrent triggers at a nominal load of 35A. Overcurrent during four consecutive switching cycles initiates a hiccup mode. During hiccup, the high-side and low-side MOSFETs are turned off for 100ms. A soft-start is attempted following the hiccup. If the overcurrent persists, the hiccup will continue.

The overvoltage triggers when the output voltage is 10% above the set-point. In overvoltage mode, the gate-source voltage of the top FET is kept at 0V and the bottom FET is kept on.

The over-temperature triggers at 145°C. In an over-temperature state, both top and bottom FETs are kept off. When the temperature cools down below 130°C, the module soft-starts.

Since an output overvoltage event is likely caused by a top FET that has failed short, in the case of an input supply that is capable of delivering high power, it is recommended that a fuse be used at the input. This is so that the bottom FET when kept on would cause high input current to flow through the fuse and quickly disengage the input supply and therefore de-energize the faulty module, preventing further damage to the end product.

Thermal Considerations and Output Current Derating

The design of the MxL7218 module removes heat from the bottom side of the package effectively. Thermal resistance from the bottom substrate material to the printed circuit board is very low.

Proper thermal design is critical in controlling device temperatures and in achieving robust designs. There are many factors that affect the thermal performance. One key factor is the temperature rise of the devices in the package, which is a function of the thermal resistances of the devices inside the package and the power being dissipated. The thermal resistances of the MxL7218 are shown in the Operating Conditions section of this datasheet. The JEDEC Θ_{JA} thermal resistance provided is based on tests that comply with the JESD51-2A “Integrated Circuit Thermal Test Method Environmental Conditions – Natural Convection” standard. JESD51 is a group of standards whose intent is to provide comparative data based on a standard test condition which includes a defined board construction. Since the actual board design in the final application will be different from the board defined in the standard, the thermal resistances in the final design may be different from those shown.

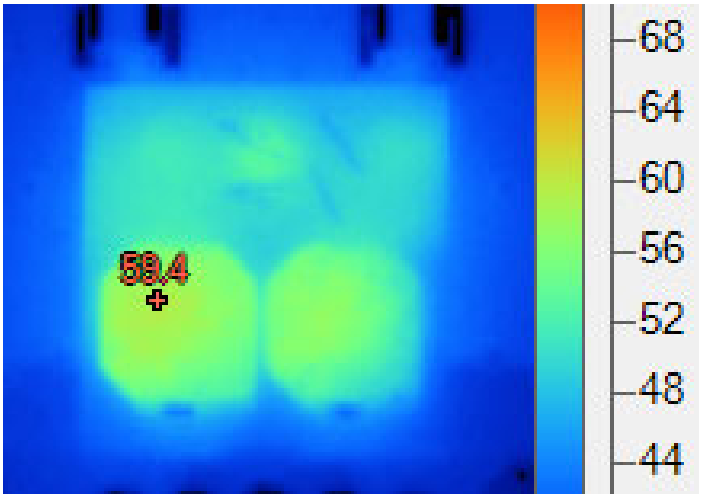


Figure 31: Thermal Image 12V to 1V, 36A with 200LFM(1)

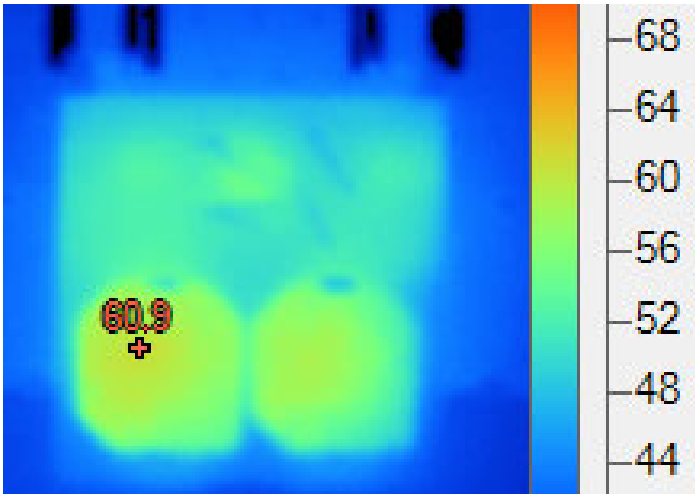


Figure 32: Thermal Image 12V to 1.2V, 36A with 200LFM(1)

1. Based on a 6-layer 3.9" x 5.1" Printed Circuit Board with 2oz copper on the outer layers and 1 oz copper on all internal layers.

Power Derating

The current derating curves in Figure 37 through Figure 40 were acquired with the test setup in Figure 33. The EVK (see details in Figure 31) was placed in a 0.5 cubic feet enclosed space with no forced air flow. The EVK was configured as a dual-phase single-output converter. The EVK was first loaded to 36A at room temperature. Ambient temperature was then gradually elevated until the module's temperature sensing diode reached 125°C. This is where Load Current starts to decrease from 36A in the curves. Beyond this point as ambient temperature increased, Load Current was decreased to maintain the 125°C diode temperature. These curves are accurate for the test setup in Figure 33 and natural convection.

Figure 35 and Figure 36 are the corresponding power dissipation in the module at room temperature.

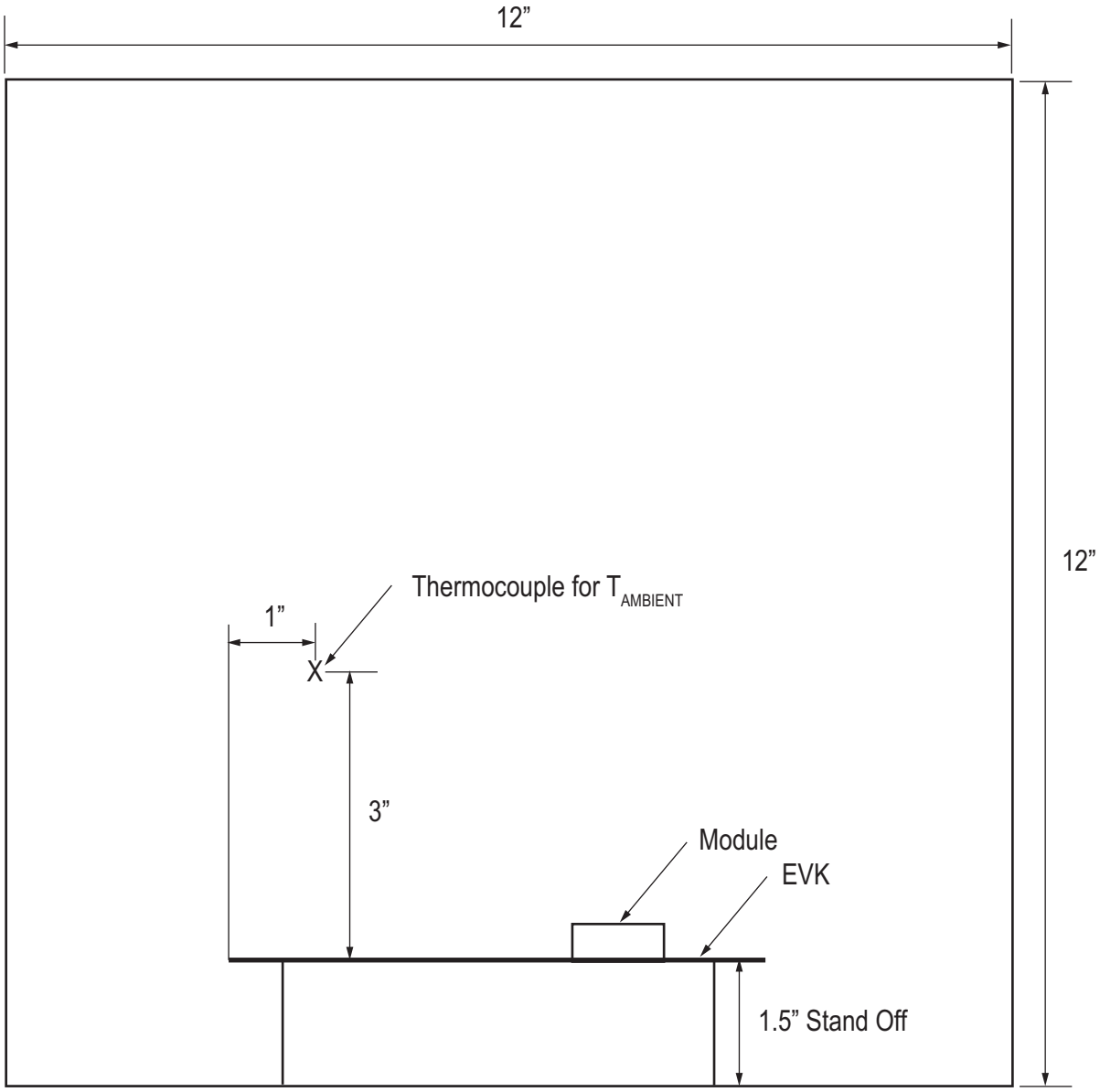


Figure 33: Current Derating Curves Measurement Setup

Table 7: Load Step Response vs. Components, Single Phase (refer to Figure 17)

	C_{IN}			C_{OUT}		
	Vendors	**Part Number**	**Value**	**Vendors**	**Part Number**	**Value**
BULK	Panasonic	25SVPF330M	330µF, 25V	Panasonic	ETPF470M5H	470µF, 2.5V, 5mΩ
CERAMIC	Murata	GRM31CR61E226KE15L	22µF, 25V, 1206, X5R	Murata	GRM32ER60J227M	220µF, 6.3V, 1206, X5R
	Wurth	885012109014	22µF, 25V, 1210, X5R	Wurth	885012109004	100µF, 6.3V, 1210, X5R

25% Load Step (0 to 4.5A, 4.5A/µs), Ceramic Output Capacitor Only Solutions											
V_{IN}	**V_{OUT}**	**C_{IN} (BULK)**	**C_{IN} (Ceramic)**	**C_{OUT} (BULK)**	**C_{OUT} (MLCC)**	**C_{FF} (pF)**	**P-P Deviation (mV)(1)**	**Feedback Loop Bandwidth (kHz)**	**Phase Margin (deg)**	**R_{FB} (kΩ)**	**PWM Freq (kHz)**
5	1	330µF	22µF x 4	None	100µF x 4	150	70	72	48	90.9	450
12	1	330µF	22µF x 4	None	100µF x 4	150	71	62	46	90.9	450
5	1.2	330µF	22µF x 4	None	100µF x 4	150	74	75	57	60.4	450
12	1.2	330µF	22µF x 4	None	100µF x 4	150	78	65	49	60.4	450
5	1.5	330µF	22µF x 4	None	100µF x 4	150	79	68	52	40.2	450
12	1.5	330µF	22µF x 4	None	100µF x 4	150	79	69	58	40.2	450
5	1.8	330µF	22µF x 4	None	100µF x 4	150	82	74	62	30.2	450
12	1.8	330µF	22µF x 4	None	100µF x 4	150	85	70	65	30.2	450

25% Load Step (0 to 4.5A, 4.5A/µs), Bulk + Ceramic Output Capacitor Solutions											
V_{IN}	**V_{OUT}**	**C_{IN} (BULK)**	**C_{IN} (Ceramic)**	**C_{OUT} (BULK)**	**C_{OUT} (MLCC)**	**C_{FF} (pF)**	**P-P Deviation (mV)(1)**	**Feedback Loop Bandwidth (kHz)**	**Phase Margin (deg)**	**R_{FB} (kΩ)**	**PWM Freq (kHz)**
5	1	330µF	22µF x 4	470µF	100µF	None	110	66	63	90.9	450
12	1	330µF	22µF x 4	470µF	100µF	None	118	58	65	90.9	450
5	1.2	330µF	22µF x 4	470µF	100µF	None	114	57	69	60.4	450
12	1.2	330µF	22µF x 4	470µF	100µF	None	119	52	71	60.4	450
5	1.5	330µF	22µF x 4	470µF	100µF	None	123	43	70	40.2	450
12	1.5	330µF	22µF x 4	470µF	100µF	None	123	44	78	40.2	450
5	1.8	330µF	22µF x 4	470µF	100µF	None	130	37	77	30.2	450
12	1.8	330µF	22µF x 4	470µF	100µF	None	131	37	78	30.2	450

1. V_{OUT} peak-to-peak deviation, worst case.

Layout Guidelines and Example

The MxL7218's high level of integration simplifies PCB board design. However, some layout considerations are still recommended for optimal electrical and thermal performance.

- Use large PCB copper areas for high current paths, including V_{IN}, V_{OUT1} and V_{OUT2} and GND to minimize conduction loss and thermal stress in the PCB.
- Use a dedicated power ground layer, placed under the MxL7218.
- Use multiple vias to interconnect the top layer and other power layers to minimize via conduction loss and module thermal stress.
- Cap or plate over any vias that are directly placed on the pad.
- Use a separated SGND ground copper area for components that are connected to the signal pins. The SGND to GND should be connected underneath the module.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, V_{OUT} and PGND pins to minimize high frequency noise.
- When paralleling modules, connect the V_{FB}, V_{OUT}, and COMP pins together closely with an internal layer. For soft-start mode, the TRACK pins may be tied together via a common capacitor.
- Test points can be brought out for monitoring the signal pins. Only bring out signals for testing purposes when absolutely necessary. Keep test points as close as possible to the module, if possible, to minimize chances of noise coupling.
- COMP1 and COMP2 are sensitive nodes. Make every effort to avoid overlapping a COMP trace with a signal that has fast edges, such as the CLKOUT, the synchronization clock, and the SW. If overlapping is unavoidable, place the COMP trace and the fast edge signal on layers that are separated by a ground plane.

An example layout for the top PCB layer for the BGA package is recommended in Figure 34.

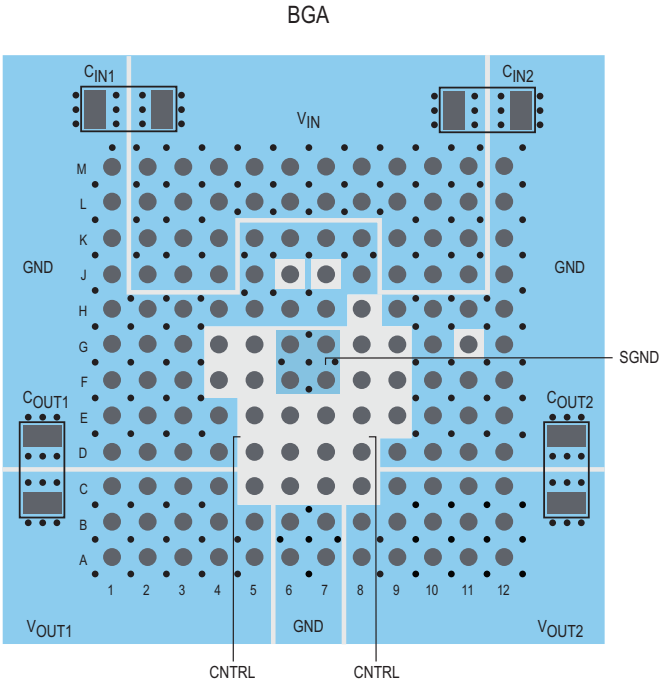


Figure 34: Recommended PCB Layout

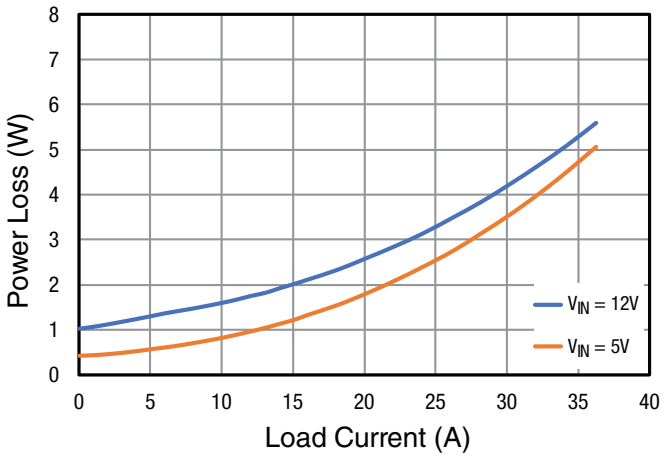


Figure 35: 1V Output Power Loss

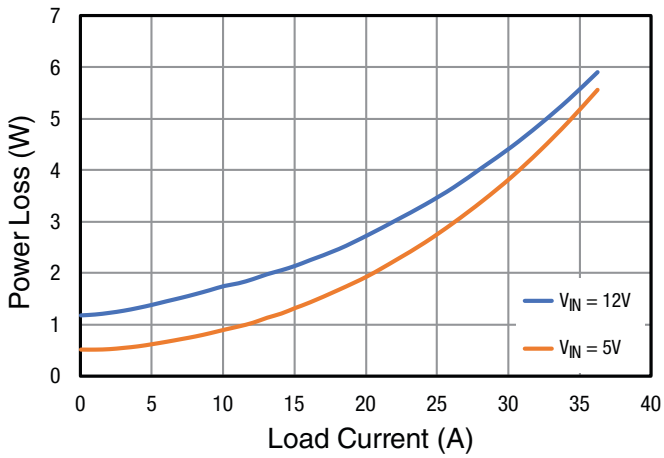


Figure 36: 1.5V Output Power Loss

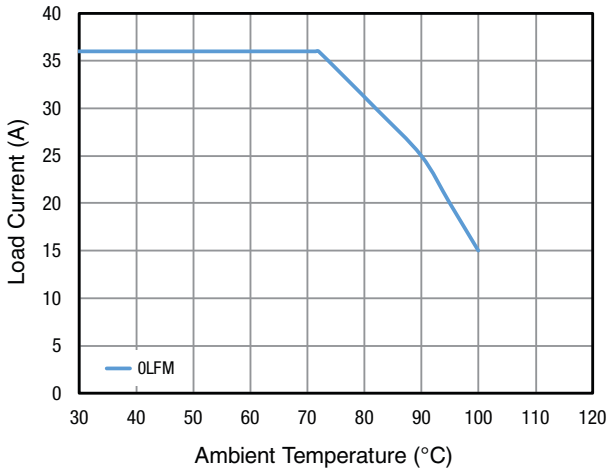


Figure 37: 12V to 1.5V Current Derating

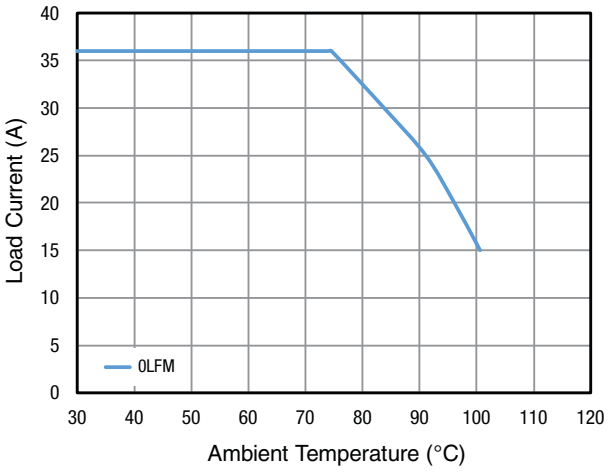


Figure 38: 12V to 1V Current Derating

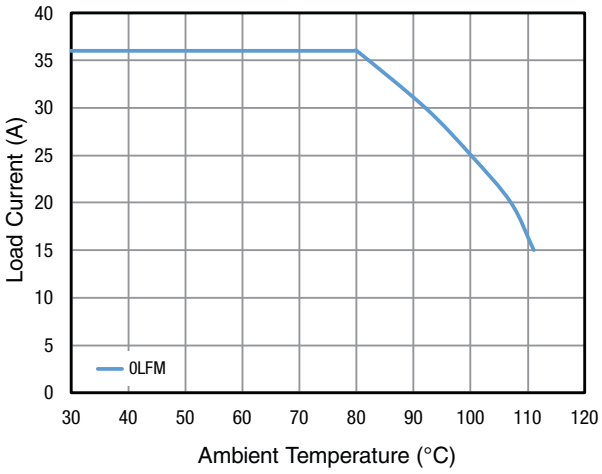


Figure 39: 5V to 1.5V Current Derating

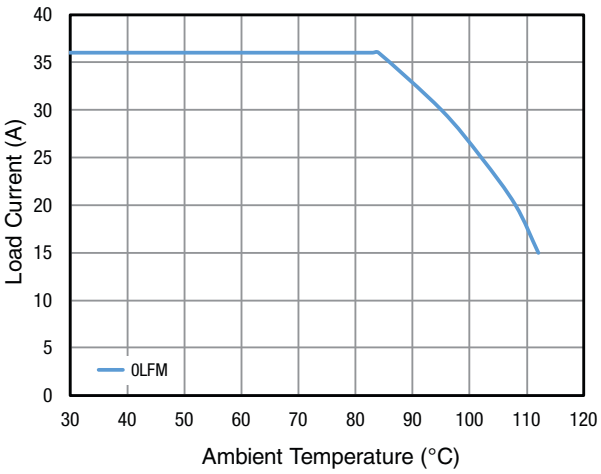
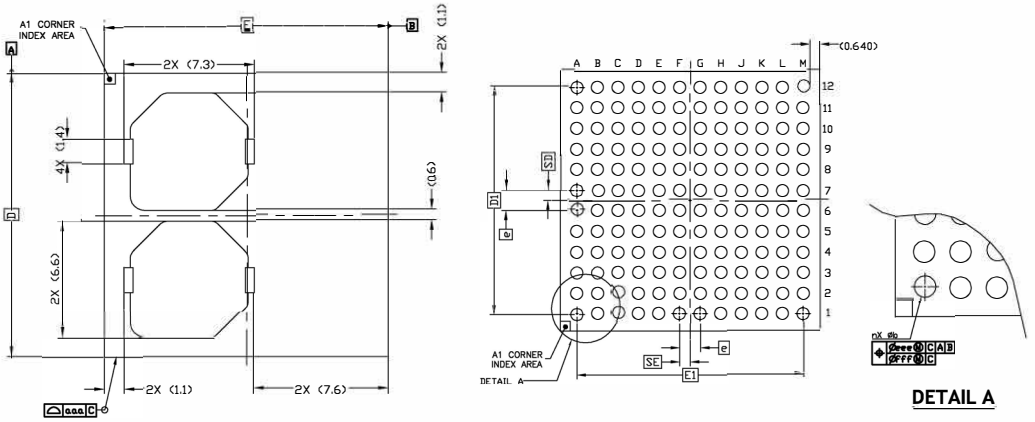


Figure 40: 5V to 1V Current Derating

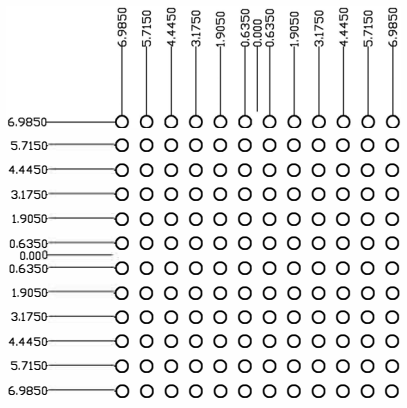
Mechanical Dimensions

16mm x 16mm x 5.01mm BGA



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	---	4.925	5.21
STAND OFF	A1	0.45	---	0.65
SUBSTRATE THICKNESS	A2	0.295	0.345	0.395
MOLD THICKNESS	A3		1.1	REF
BODY SIZE	D		16	BSC
	E		16	BSC
BALL DIAMETER			0.7	
BALL OPENING		0.55	0.6	0.65
BALL WIDTH	b	0.6	---	0.9
BALL PITCH	e		1.27	BSC
BALL COUNT	n		144	
EDGE BALL CENTER TO CENTER	D1		13.97	BSC
	E1		13.97	BSC
BODY CENTER TO CONTACT BALL	SD		0.635	BSC
	SE		0.635	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.25	
COPLANARITY	ddd		0.2	
BALL OFFSET (PACKAGE)	eee		0.3	
BALL OFFSET (BALL)	fff		0.15	

TERMINAL DETAILS



PAD LOCATION

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

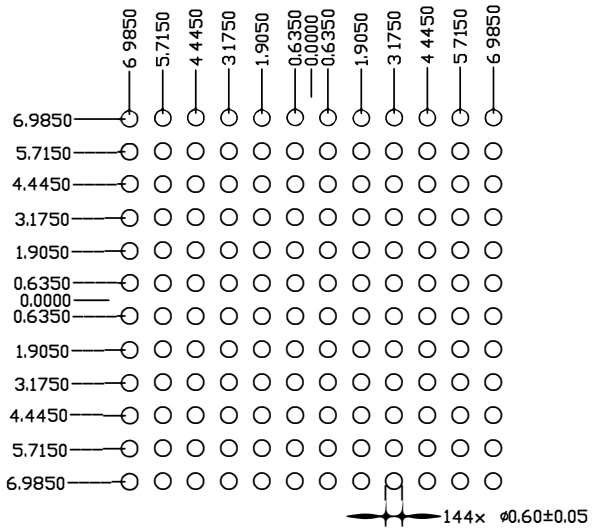
Drawing No.: POD-00000149

Revision: B

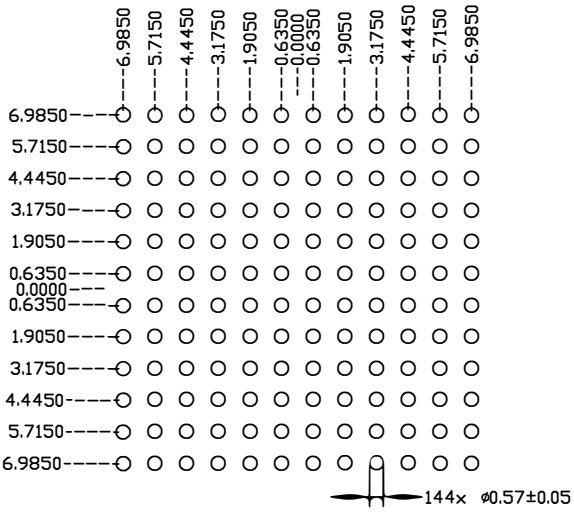
Figure 41: Mechanical Dimensions, BGA

Recommended Land Pattern and Stencil

16mm x 16mm x 5.01mm BGA



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-00000149

Revision: B

Figure 42: Recommended Land Pattern and Stencil, BGA

MxL7218 Component Pinout

Table 8: MxL7218 Component Pinout

Pin ID	Function	Pin ID	Function	Pin ID	Function	Pin ID	Function	Pin ID	Function	Pin ID	Function
A1	V_{OUT1}	B1	V_{OUT1}	C1	V_{OUT1}	D1	GND	E1	GND	F1	GND
A2	V_{OUT1}	B2	V_{OUT1}	C2	V_{OUT1}	D2	GND	E2	GND	F2	GND
A3	V_{OUT1}	B3	V_{OUT1}	C3	V_{OUT1}	D3	GND	E3	GND	F3	GND
A4	V_{OUT1}	B4	V_{OUT1}	C4	V_{OUT1}	D4	GND	E4	GND	F4	MODE_PLLIN
A5	V_{OUT1}	B5	V_{OUT1}	C5	V_{OUTS1}	D5	V_{FB1}	E5	TRACK1	F5	RUN1
A6	GND	B6	GND	C6	f_{SET}	D6	SGND	E6	COMP1	F6	SGND
A7	GND	B7	GND	C7	SGND	D7	V_{FB2}	E7	COMP2	F7	SGND
A8	V_{OUT2}	B8	V_{OUT2}	C8	V_{OUTS2}	D8	TRACK2	E8	DIFFP	F8	DIFFOUT
A9	V_{OUT2}	B9	V_{OUT2}	C9	V_{OUT2}	D9	GND	E9	DIFFN	F9	RUN2
A10	V_{OUT2}	B10	V_{OUT2}	C10	V_{OUT2}	D10	GND	E10	GND	F10	GND
A11	V_{OUT2}	B11	V_{OUT2}	C11	V_{OUT2}	D11	GND	E11	GND	F11	GND
A12	V_{OUT2}	B12	V_{OUT2}	C12	V_{OUT2}	D12	GND	E12	GND	F12	GND
G1	GND	H1	GND	J1	GND	K1	GND	L1	GND	M1	GND
G2	SW1	H2	GND	J2	V_{IN}	K2	V_{IN}	L2	V_{IN}	M2	V_{IN}
G3	GND	H3	GND	J3	V_{IN}	K3	V_{IN}	L3	V_{IN}	M3	V_{IN}
G4	PHASMD	H4	GND	J4	V_{IN}	K4	V_{IN}	L4	V_{IN}	M4	V_{IN}
G5	CLKOUT	H5	GND	J5	GND	K5	GND	L5	V_{IN}	M5	V_{IN}
G6	SGND	H6	GND	J6	TEMP	K6	GND	L6	V_{IN}	M6	V_{IN}
G7	SGND	H7	GND	J7	$EXTV_{CC}$	K7	GND	L7	V_{IN}	M7	V_{IN}
G8	PGOOD2	H8	$INTV_{CC}$	J8	GND	K8	GND	L8	V_{IN}	M8	V_{IN}
G9	PGOOD1	H9	GND	J9	V_{IN}	K9	V_{IN}	L9	V_{IN}	M9	V_{IN}
G10	GND	H10	GND	J10	V_{IN}	K10	V_{IN}	L10	V_{IN}	M10	V_{IN}
G11	SW2	H11	GND	J11	V_{IN}	K11	V_{IN}	L11	V_{IN}	M11	V_{IN}
G12	GND	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND

Ordering Information

Table 9: Ordering Information

Ordering Part Number	Operating Temperature Range	MSL Rating	Lead-Free	Package	Packaging Method
MxL7218-ABA-T	-40°C ≤ T_J ≤ 125°C	3	Yes	BGA144 16x16	Tray
MxL7218-EVK-1	MxL7218 BGA Evaluation Board, Single Device, Dual Output				
MxL7218-EVK-2	MxL7218 BGA Evaluation Board, 4 Devices, Multiphase				

For most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/MxL7218.

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