88LX5152 and 88LX5153

Data Sheet

Wave-2 G.hn Digital Baseband (DBB) Processor

General Description

This data sheet describes the MaxLinear 88LX5152 and 88LX5153 Wave-2 G.hn DBB processor.

The 88LX5152 and 88LX5153 devices are MaxLinear's new-generation DBB processors for wireline communications using existing cables. While the 88LX5152 device is focused on the powerline medium, the 88LX5153 has been designed to cover the powerline, coaxial, phone lines, plastic optical fiber (POF), and optical transceiver (LiFi).

Applications

- Powerline-to-Ethernet Adapter
- Coaxial/phone line-to-Ethernet adapter.
- Multi-medium-to-Ethernet adapter.
- Coaxial/powerline backhauling of WiFi mesh systems.
- Embedded G.hn modem
- G.hn aggregation multiplexer (GAM) for multiple dwelling unit (MDU) phone line access.
- Embedded communication module for industrial applications.
- Fiber extender.
- G.9991 LiFi access point and end point.

Features

- Highest performance PHY data rates
- Reduced BOM cost
- Reliability and robustness
- Automatic mesh networks
- Low-power and sleep mode support
- Security
- Advanced and well-proven algorithms for neighboring domain interference mitigation (NDIM)
- Enhanced hardware support
- Embedded stacks and clients
- Rich set of interfaces
- Available in commercial and industrial temperature range.

Supported Standards

- Code of Conduct on Energy Consumption of Broadband Equipment Version 5.0, European Commission
- ITU-T G.9960: Unified high-speed wireline-based home networking transceivers—system architecture and physical layer specification (referenced as ITU-T G.9960)
- ITU-T G.9961: Unified high-speed wire-line based home networking transceivers—data link layer specification (referenced as ITU-T G.9961)
- ITU-G.9962: Unified high-speed wire-line based home networking transceivers—management specification (referenced as ITU-T G.9962)
- ITU-T G.9963: Unified high-speed wireline-based home networking transceivers—multiple input/multiple output specification (referenced as ITU-T G.9963).
- ITU-T G.9964: Unified high-speed wire-line based home networking transceivers—power spectral density specification
- ITU-T G.9991: High speed indoor visible light communication transceiver—System architecture, physical layer and data link layer specification

Revision History

Document No.	Release Date	Change Description
072-5253DSR05	July 14, 2020	**Updated:** ■ Confidentiality protection removed.
072-5253DSR04	April 21, 2020	**Updated:** ■ "General" section. ■ "Description" section. ■ "Applications" section. ■ "Supported Standards" section. ■ "Introduction" section. ■ "Chipset Combinations for Typical Applications" table. ■ "Required Operating Conditions" table. ■ General document review. **Added:** ■ "G.9991 LiFi Access Point and End Point" section. ■ "Embedded Communication Module for Industrial Applications" section.
072-5253DSR03	August 28, 2020	**Added:** ■ "Chipset Combinations for Typical Applications" table. ■ "88LX5153A Package Marking and Pin 1 Location" Figure. **Updated:** ■ "Applications." ■ "Features." ■ "Introduction." ■ "Embedded G.hn Modem." ■ "88LX5152/5153 186-Pin TFBGA Package" figure. ■ "Signal Pin List Sorted Alphabetically" table. ■ "Power Pin List Sorted Alphabetically" table. ■ "RGMII/MII." ■ "Power and Ground" table. ■ "Other Pins" table. ■ "Power and Ground" table. ■ "Required Operating Condition" table. ■ "SerDes Specification" table. ■ "88LX5152/5153 Part Order Options" table. ■ "88LX515X Commercial Package Marking and Pin 1 Location" figure.
053DSR02	September 13, 2017	Initial release.

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Introduction

The MaxLinear 88LX5152 and 88LX5153 devices are second-generation G.hn DBB processors for wireline communications using existing cables. While the 88LX5152 device is focused on the powerline medium the 88LX5152 and 88LX5153 covers the powerline, coaxial, phone cables, POF, and LiFi.

The devices implement the ITU-T G.hn standard, doubling the speed achieved in the previous product generation by providing up to 2Gbps. The 88LX5152 and 88LX5153 devices include optimized MIMO (2 × 2) and advanced MIMO (3 × 2) technology for the powerline medium. The 88LX5152 and 88LX5153 devices provide enhanced 200MHz bandwidth modulation to support superior throughput in coaxial, phone lines, POF, and LiFi. The 88LX5153 also incorporates the possibility to bond two phone line channels when they are available to be used.

Both devices contain industry-leading features and best in-class security, directly interface to companion AFE devices (MaxLinear 88LX2720, 88LX2730, and 88LX2740), and are highly-integrated devices that are adapted to powerline, coaxial, phone line, POF, and LiFi media.

The 88LX5153A is a variant of the 88LX5153 that supports an industrial temperature range. The 88LX5153A is intended for infrastructure and smart grid applications such as G.hn aggregation multiplexers (GAMs), G.hn distribution point units (DPUs), smart meter modules, demand management units, and lighting control devices. In all of these cases the 88LX5153A requires the industrial 88LX2741.

The 88LX5152 and 88LX5153 devices are low-cost integrated circuits optimized to enable high-speed video and data communications over coaxial, phone, POF, LiFi, or powerlines. The devices' high performance and low-power consumption make them ideally suited for stand-alone GbE adapters and embedded communication solutions in devices such as gateways and STBs, as well as in combination with existing WiFi access points.

IC Block Diagram

The following figure shows a functional block diagram of the 88LX5152 and 88LX5153 devices.

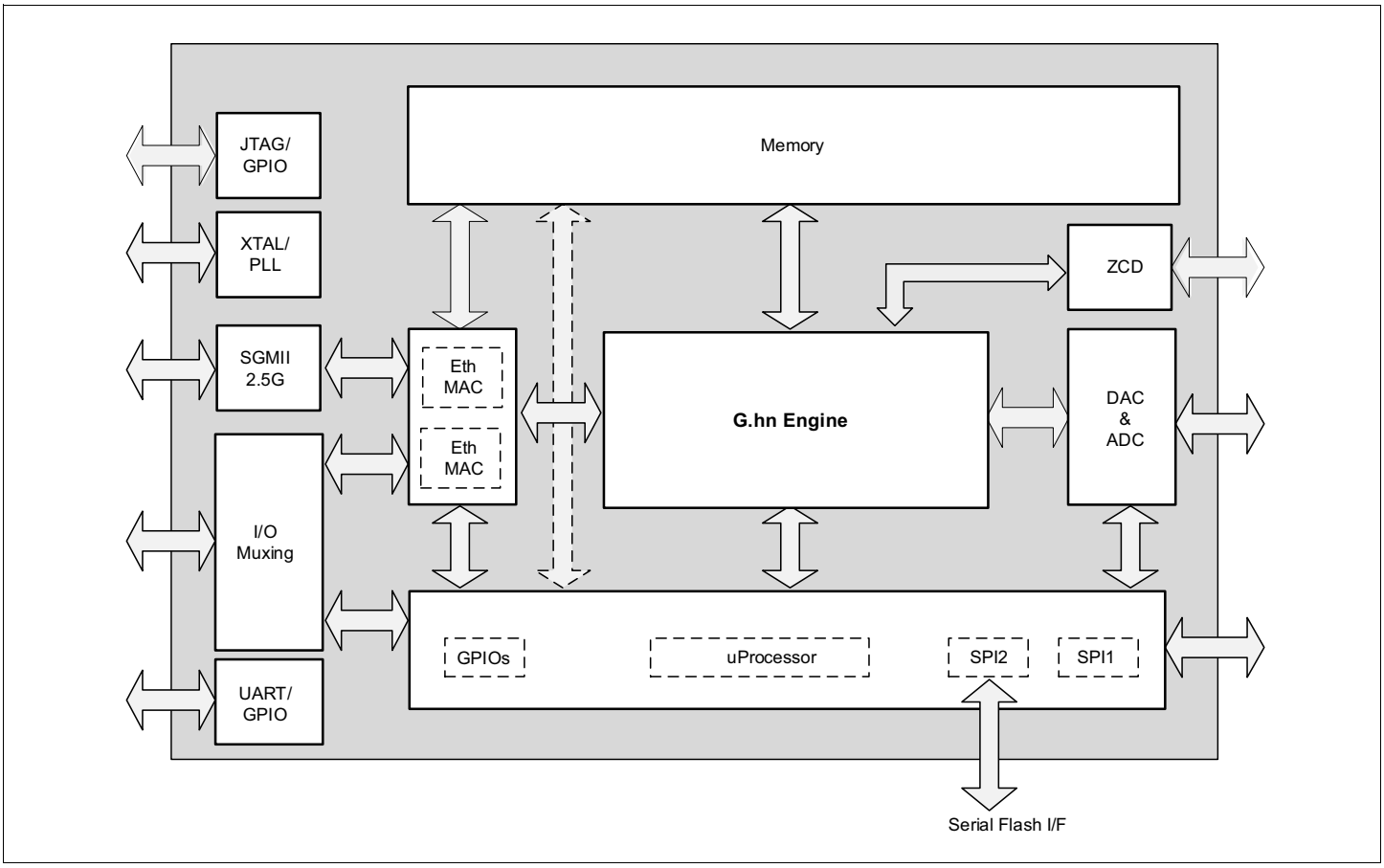

Figure 1: 88LX5152 and 88LX5153 Block Diagram

The devices include:

- A G.hn data path, which implements a G.hn PHY as specified in ITU-T G.9960 and ITU-T G.9963.
- Hardware functions of the G.hn DLL layers specified in ITU-T G.9961, including the AES-128 encryption engine.

The external AFE devices are in charge of amplification, filtering, and driving the corresponding line signal.

The 88LX5152 and 88LX5153 G.hn DBB processors contain an embedded microcontroller subsystem to implement the software functions of the MAC and DLL layers, as well as management functions as specified by ITU-T G.9962. This subsystem includes peripherals such as timers, interrupt controller, and a set of serial UART and SPI controllers (in addition to the CPU and processor memory).

On one side of the data path, there are two GbE MACs that can be connected to external 10/100/1000Mbps PHYs using both the MII/RGMII and SGMII buses.

On the other side of the data path, the ADC and DAC converters act as the interface between the G.hn engine and the external MaxLinear AFE device.

For more information refer to the following documents:

- 88LX2720 Wave-2 G.hn AFE Data Sheet (073-2720DS)
- 88LX2730 Wave-2 G.hn AFE Data Sheet (073-2730DS).
- 88LX2740 Wave-2 G.hn AFE Data Sheet (073-2740DS).
- 88LX2741 Wave-2 G.hn Industrial AFE Data Sheet (073-2741DS).

Developers can use the microcontroller for value-adding applications. MaxLinear provides a rich set of communication and management applications with the Spirit firmware, as well as a flexible API that developers can use to build their own applications.

The 88LX5152 and 88LX5153 integrates a memory block to minimize BOM costs and complexity of the board where they are mounted. Access to the internal memory by all these elements is governed by an embedded memory controller.

Highest Performance PHY Data Rates

- Up to 2Gbps PHY rate.
- SISO, optimized (2 × 2), and advanced (3 × 2) MIMO over powerlines.
- Two 100MHz channel bonding over phone lines (only 88LX5153).
- Support for all G.hn BB band plans:
  - 25MHz, 50MHz, and 100MHz for powerline.
  - Programmable notching and dynamic notching capability.
- Support for BB frequency of 200MHz for coaxial, phone lines, and POF (only 88LX5153).

Integrated DDR Memory

- Memory block is integrated into the 88LX5152 and 88LX5153 to reduce board size, complexity, and cost.

Reliability and Robustness

- LDPC FEC provides enhanced FEC over all wire media.
- Enhanced selective repeat ARQ-based ACK for improved integrity in noisy channels.
- Robust Communication Mode (RCM) for high-noise environments.

Automatic Mesh Networks

- Relaying between nodes that cannot connect directly (subject to enabling firmware availability).

Low-Power and Sleep Mode Support

- Enables Energy-related Products (ErP) compliant standby mode devices with reactivation by an external button or Ethernet activity.

  Note: Per the EU directive on the low-power mode for ErP.

- Enables compliance with *European Code of Conduct on Energy Consumption of Broadband Equipment, Version 6.0*.

Security

- 128-bit AES CCMP encryption.
- End-to-end encryption pair-wise keys.
- Strict authentication rules.

Neighboring Domain Interference Mitigation (NDIM)

- Isolate or coordinate neighboring networks in powerlines to optimize aggregated performance in multi-dwelling environments.

Enhanced Hardware Support

- Enhanced traffic handling:
  - Hardware-driven packet inspection for IPv4 IGMP snooping and IPv6 MLD.
  - Hardware-based bandwidth limitation.
  - Eight levels of packet-prioritized QoS.
  - Strict priority QoS
- Power management.
- Traffic generator for self-diagnostics.
- Line impedance sensing.

Embedded Stacks and Clients

- Dual TCP/IP with IPv4/IPv6 stacks built-in.
- Native TR-069 and TR-111 (part 1 and part 2) clients.
- HTTP server for remote configuration management.
- DHCP, DNS, NTP, and FTP clients for remote firmware management and access.

Rich Set of Interfaces

- SGMII (1Gbps/2.5Gbps).
- MII/RGMII.
- 2 × SPI.
- UART.
- JTAG.

Note:

- The RGMII/MII and SGMII cannot be used simultaneously. Check with MaxLinear's Customer Technical Support if a specific user case is supported.
- The feature set may vary depending on the firmware version.

Typical Applications

The G.hn chipset (88LX5152 and 88LX5153, and 88LX27x0) can be used in stand-alone or embedded applications. This section describes the typical applications.

Table 1: Chipset Combinations for Typical Applications

Application	BBP	AFE	Reference Design
MIMO PLC Home Networking	88LX5152	2 × 88LX2720	DW920
SISO PLC Home Networking	88LX5152	1 × 88LX2720	-
Coaxial Home Networking	88LX5153	1 × 88LX2730	DCP962C
MIMO Phone Line Home Networking	88LX5153	2 × 88LX2730	DCP962P
Multi-Medium MIMO PLC and Coaxial Home Networking	88LX5153	2 × 88LX2740	Refer to the *Multi-Medium G.hn Ethernet Adapter Application Note (071AN)*.
N-channel MIMO Phone Line Aggregation Multiplexer for MDU	N × 88LX5153	2 × N x 88LX2730	-
N-channel Coaxial Line Aggregation Multiplexer for MDU	N × 88LX5153	1 × N × 88LX2730	
PLC Smart Grid Module with Industrial Temperature Range	88LX5153A	1 × 88LX2741	Refer to the *G.hn Wave-2PLC DE910 Embedded Module Customer Notice* (002CN)
PLC Smart Grid Head End with Industrial Temperature Range	88LX5153A	2 × 88LX2741	-
N-channel Coaxial/Phone Line Aggregation Multiplexer for MDU with Industrial Temperature Range	N × 88LX5153A	1 × N × 88LX2741	-
G.9991 LiFi Access Point and End Point	1 × 88LX5153	1 × 88LX2730	-

Powerline-to-Ethernet Adapter

The powerline-to-Ethernet adapter is a stand-alone application containing the G.hn chipset (88LX5152 and 88LX5153, and 88LX2720), power supply, and Ethernet interface in a single wall-plug box. MaxLinear provides reference designs implementing this application, including GbE (Gigabit Ethernet) and PLC MIMO modes, in which two 88LX2720 devices are used. This design can also be modified to use SISO only. In this case only one 88LX2720 device is needed.

The following figure shows the block diagram of the powerline-to-Ethernet MIMO implementation.

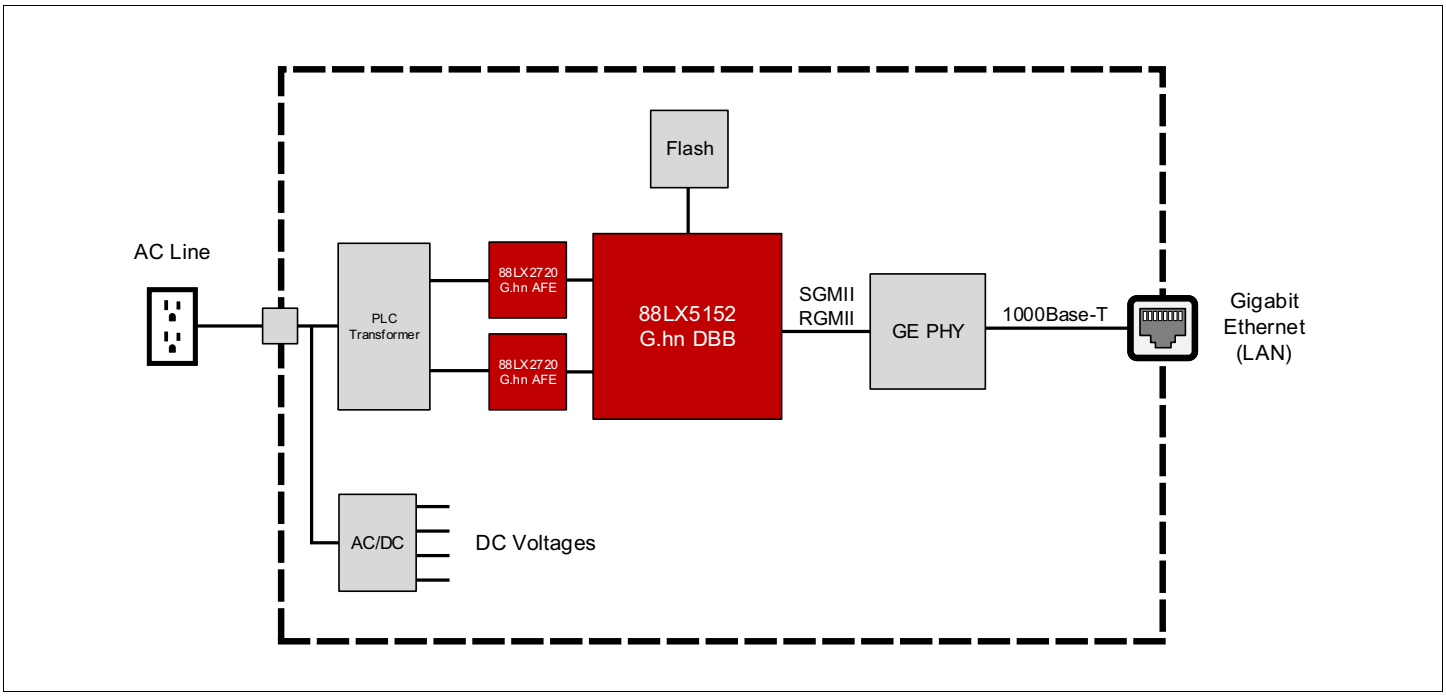

Figure 2: G.hn GbE MIMO PLC Adapter Block Diagram

The following figure shows the block diagram of the powerline-to-Ethernet SISO implementation.

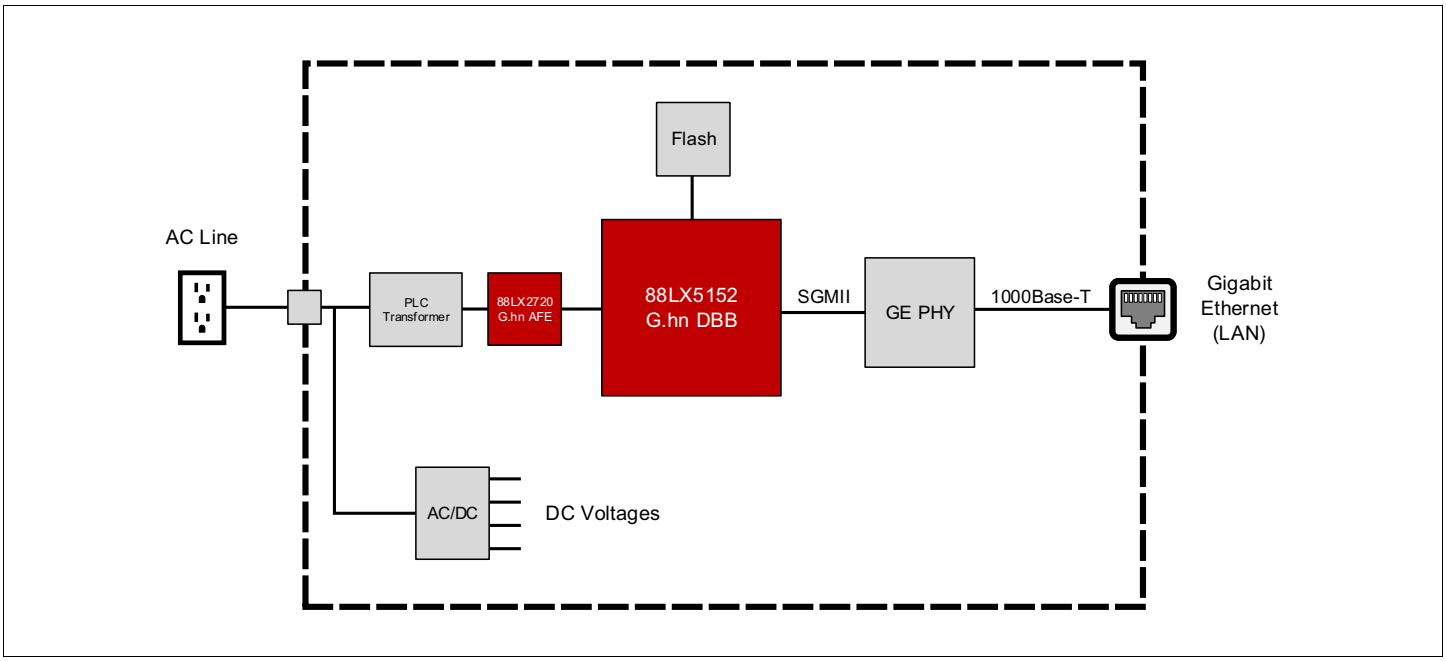

Figure 3: G.hn GbE SISO PLC Adapter Block Diagram

If an auxiliary-filtered AC outlet is required, guidelines on how to implement this feature are provided in the *GE-DW720 Auxiliary Filtered AC Outlet Application Note* (073AN).

Coaxial/Phone Line-to-Ethernet Adapter

The coaxial/phone line-to-Ethernet adapter is a stand-alone application containing the G.hn chipset (88LX5153 and 88LX2730) and Ethernet interface in a single desktop box. The design to cover this application can implement either the coaxial or the phone line interface, and can use an external AC/DC power supply.

If the phone line interface is implemented, the G.hn chipset can support the bonding of two 100MHz channels. In this case, two 88LX2730 devices are needed.

The following figure shows the block diagram of a coaxial-Ethernet adapter

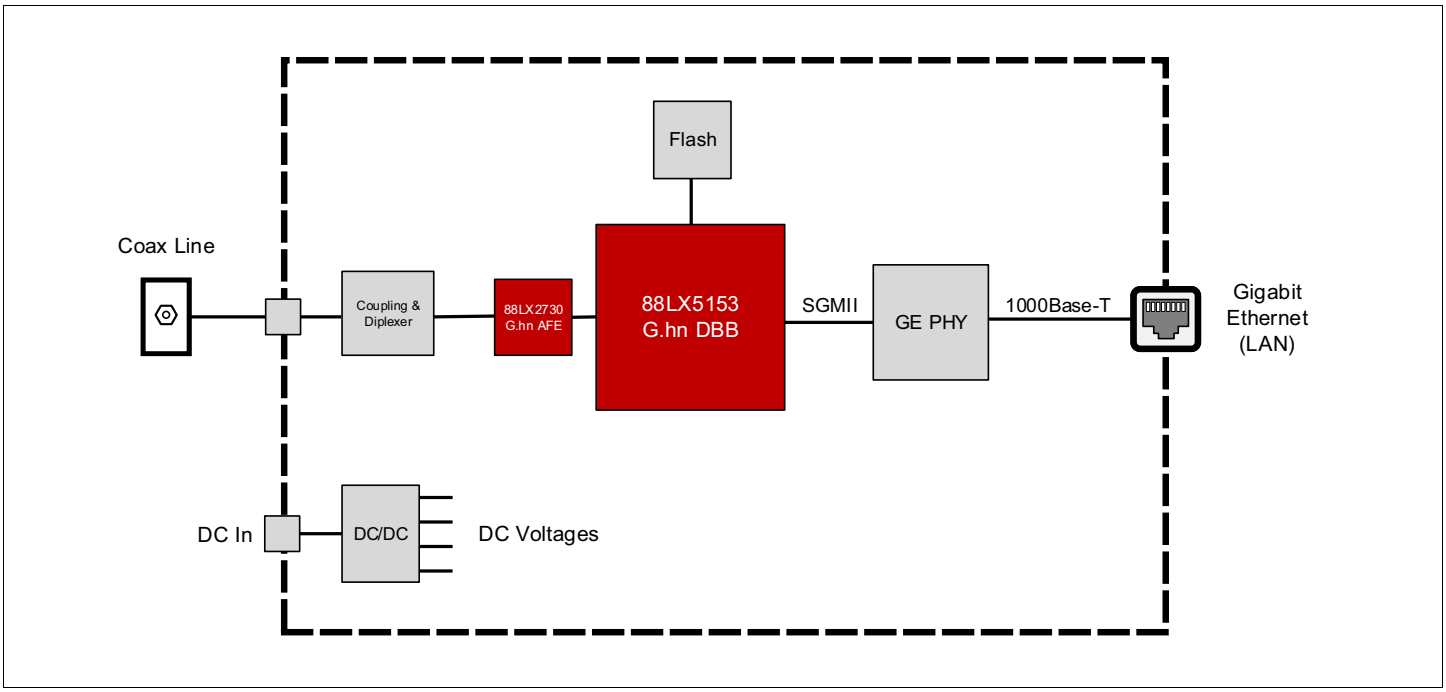

Figure 4: Coaxial-to-Ethernet Adapter Block Diagram

The following figure shows the block diagram of a coaxial-Ethernet adapter with 4 × 1Gbps ports switch using SGMII 2.5Gbps.

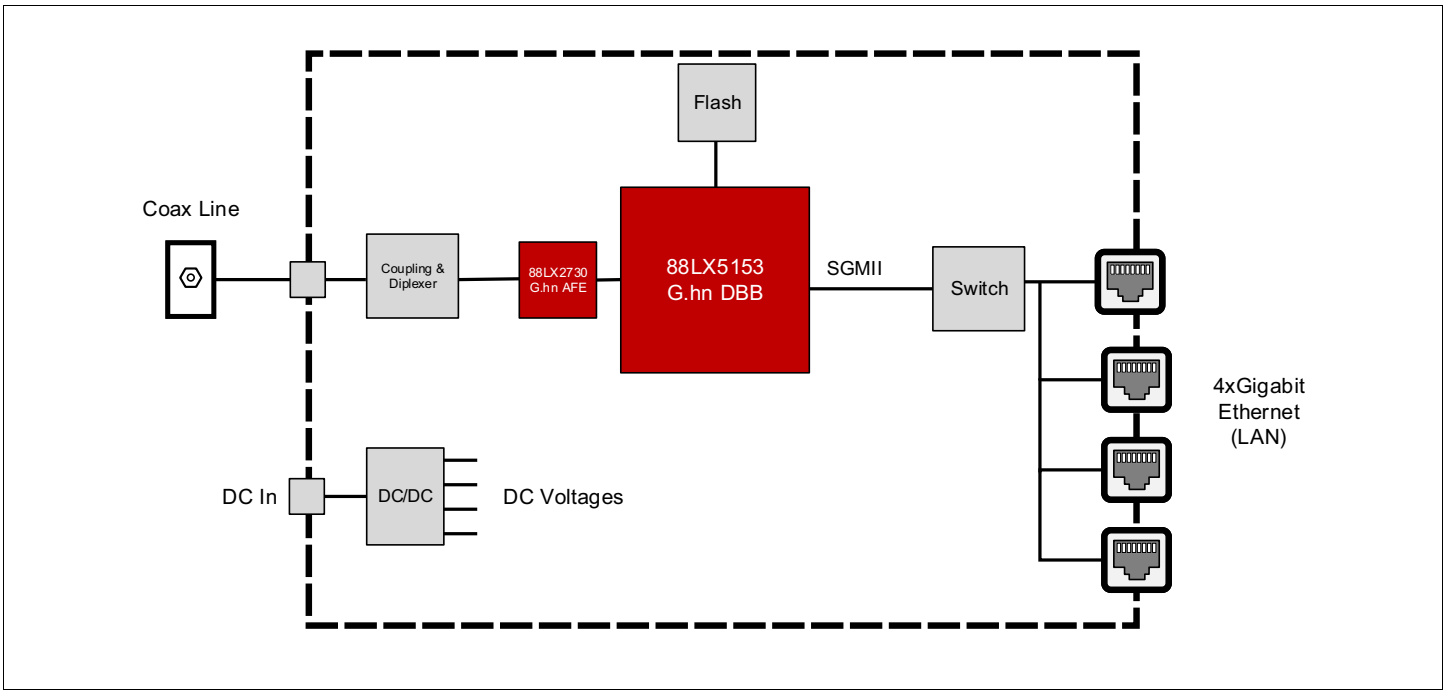

Figure 5: Coaxial-to-Ethernet Adapter Block Diagram with SGMII 2.5Gbps

The following figure shows the block diagram of a phone line-to-Ethernet adapter supporting channel bonding.

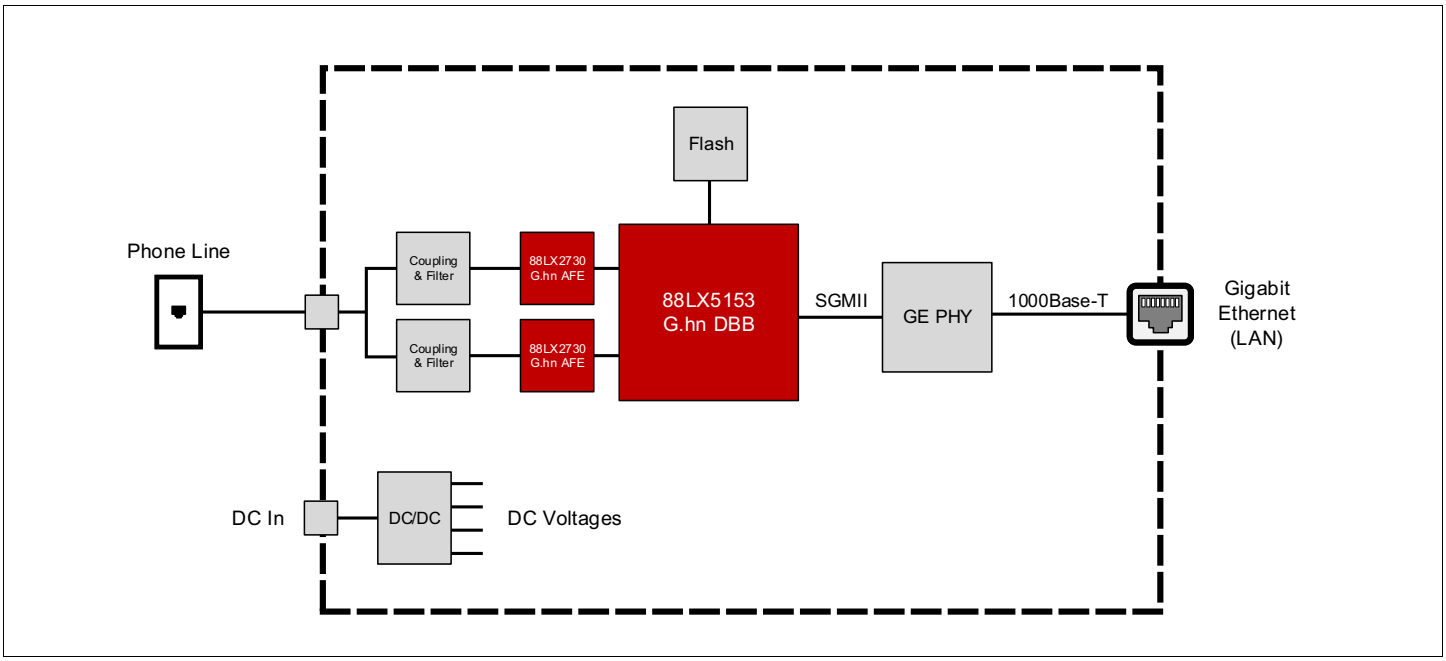

Figure 6: Phone Line-to-Ethernet Adapter Block Diagram

Multi-Medium-to-Ethernet Adapter

The multi-medium-to-Ethernet adapter is a stand-alone design containing the Wave-2 G.hn chipset, power supply, and Ethernet interface in a single wall-plug box.

Depending on which path is active, the adapter can support a SISO/MIMO powerline, SISO/MIMO phone line, or SISO coaxial connectivity to ensure maximum flexibility in installation options due to the versatility of G.hn.

The following figure shows a block diagram of the multi-medium Ethernet adapter.

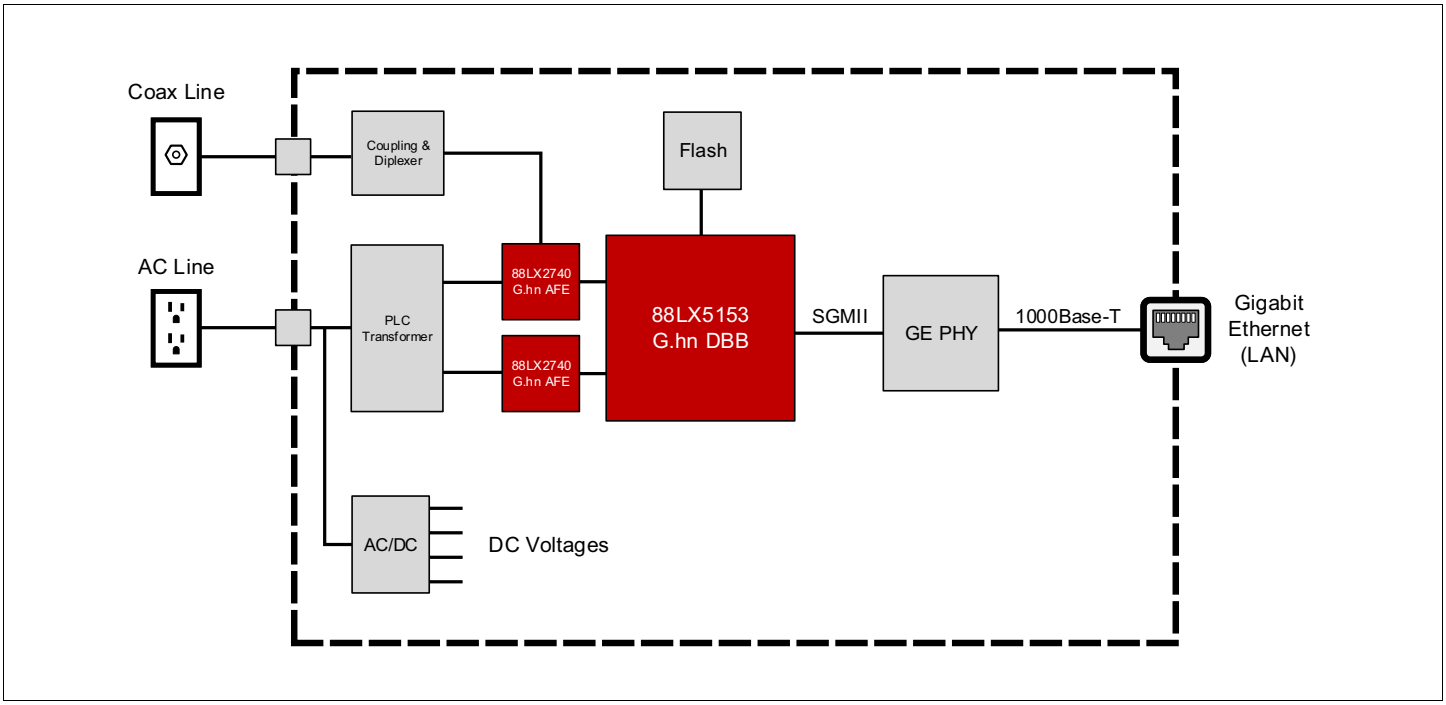

Figure 7: Multi-Medium G.hn Gigabit Ethernet Adapter Block Diagram

Coaxial/Powerline Backhauling of WiFi Mesh Systems

The coaxial/powerline-WiFi extender is a stand-alone application containing the G.hn chipset, a CPU, the power supply, and a WiFi access point in a single platform, which is used to improve the coverage of wireless networks when the distance from a primary access point does not allow for an acceptable performance with the wireless end point. Placing this device, including a secondary access point nearer the end point using powerline as backbone, provides significant improvement in this wireless link.

This application can implement the GbE interface, PLC MIMO, and any kind of *IEEE 802.11*-based WiFi access point. The design can be modified to use SISO only to provide the backbone over coaxial or phone lines.

The following figure shows the block diagram of the coaxial-WiFi platform example.

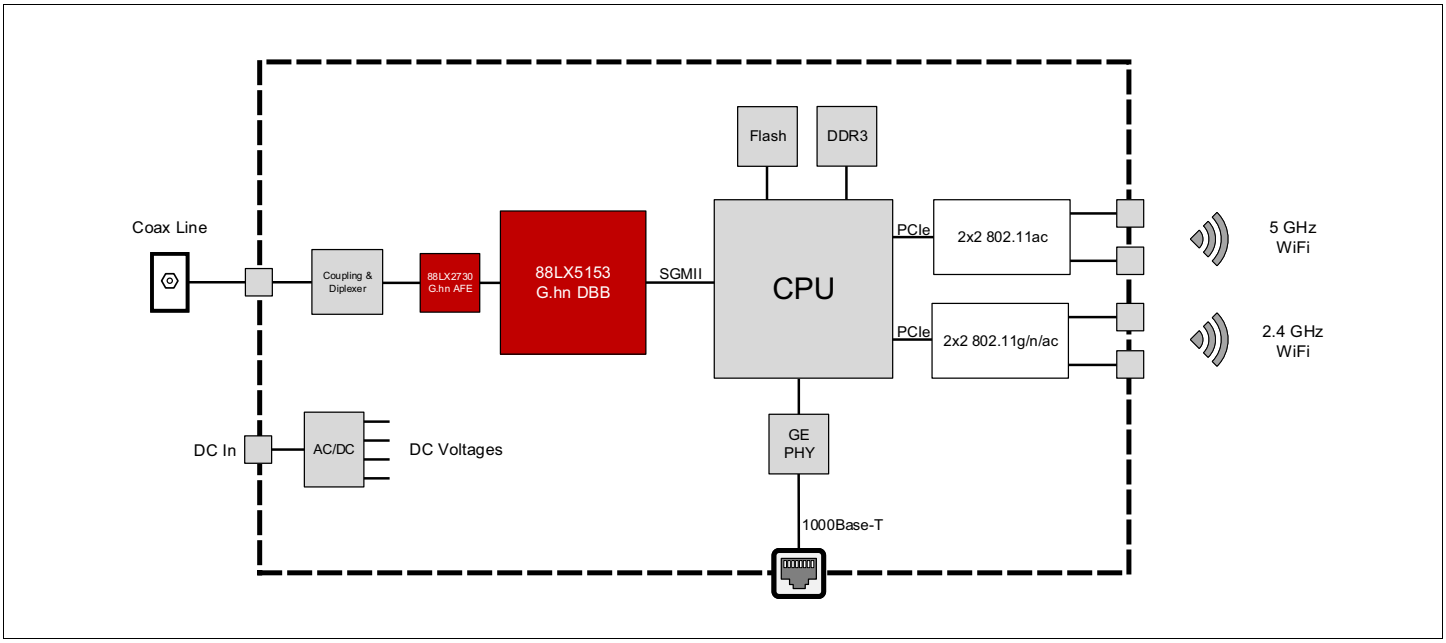

Figure 8: Coaxial-WiFi Extender Block Diagram

The following figure shows the block diagram of the powerline-WiFi platform example.

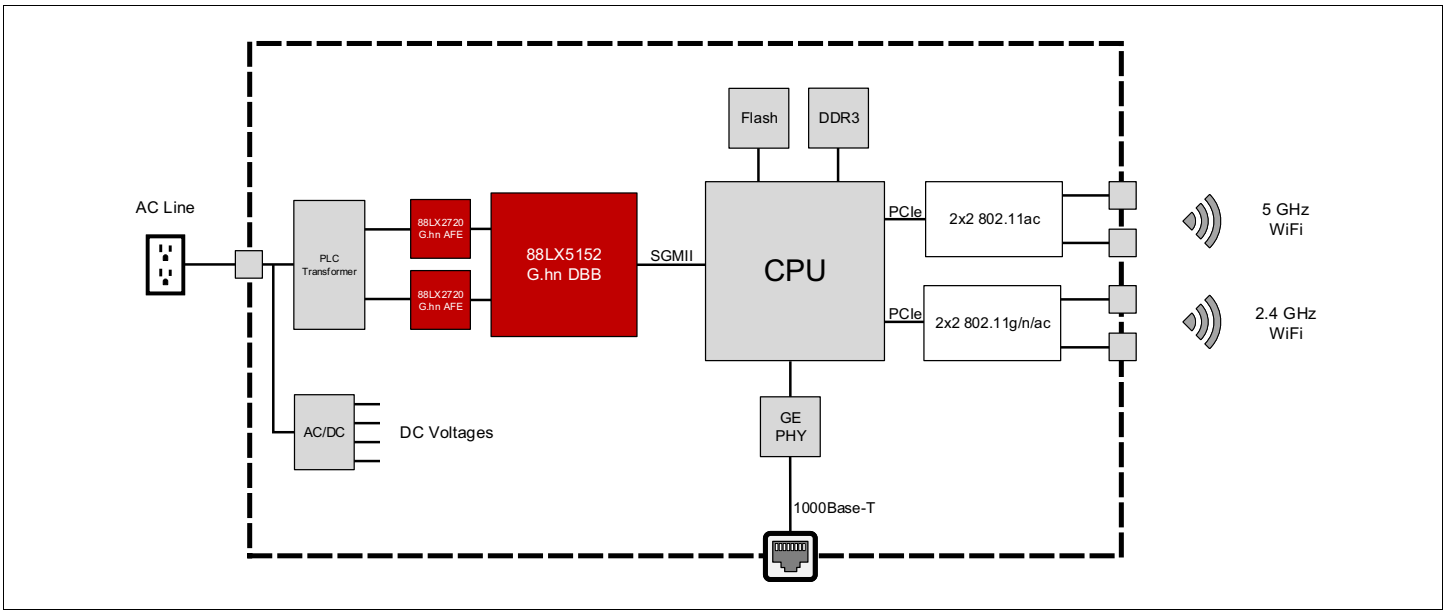

Figure 9: Powerline WiFi Extender Block Diagram

Embedded G.hn Modem

The G.hn chipset can be embedded in other designs to provide a powerful networking capability on wired media other than Ethernet. There are two possible ways of interconnecting the 88LX5152 and 88LX5153 DBB processor to the host system:

- RGMII/MII: The device can operate as MAC or PHY depending on the strapping configuration defined in “Pin Description” on page 21. The delays for Tx and Rx clocks can be configured by strapping. Only full-duplex operation is supported.
- SGMII: The device can operate different modes depending on the strapping configuration defined in “Pin Description” on page 21. Only full-duplex operation is supported.

The following figure shows the block diagram of an embedded G.hn modem.

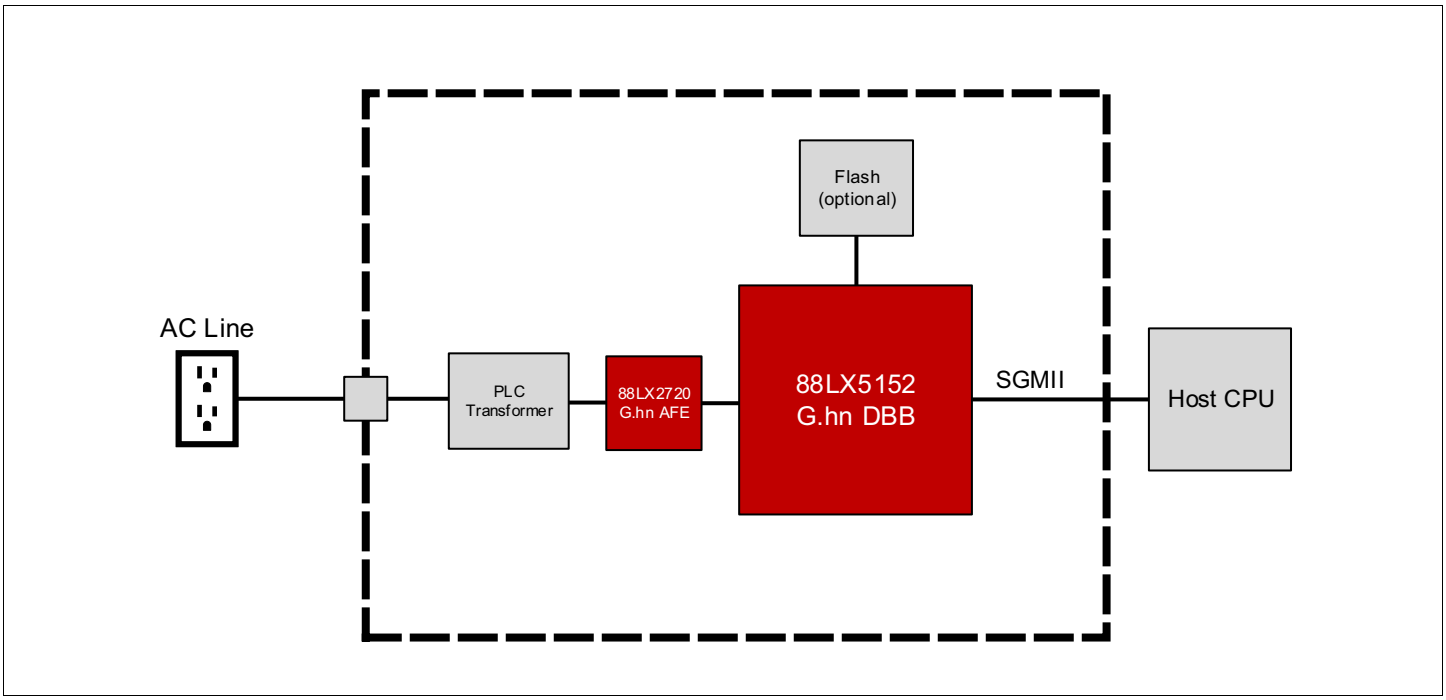

Figure 10: Embedded G.hn Modem Block Diagram

When the design is embedded in a larger system, two functions can be exported to the host CPU:

- Firmware loading: The G.hn DBB device can boot from the host CPU over the MII or RGMIIinstead of booting from a flash memory. In this case the host CPU must implement a daemon to detect the boot request message and download the firmware to the BB chipset.
- Centralized configuration: The configuration of the G.hn DBB device can be stored in the host instead of in the G.hn flash memory. In this case the host CPU must implement a method to transfer the G.hn configuration to the DBB device in addition to the GUI and the storage of the data.

The flash memory supporting the G.hn device can be saved only when both functions are fully implemented.

For hardware and software guidelines on how to embed the G.hn chipset refer to the *Device Embedding Kit (DEK) Description User Guide (*053UG*).*

G.hn Aggregation Multiplexer for MDU Phone Line Access

The G.hn aggregation multiplexer (GAM) application is a multi-port platform that includes the G.hn chipset, high-end switching, and a CPU to support MDU access scenarios over existing phone lines.

The following figure shows a block diagram of a GAM implementation example.

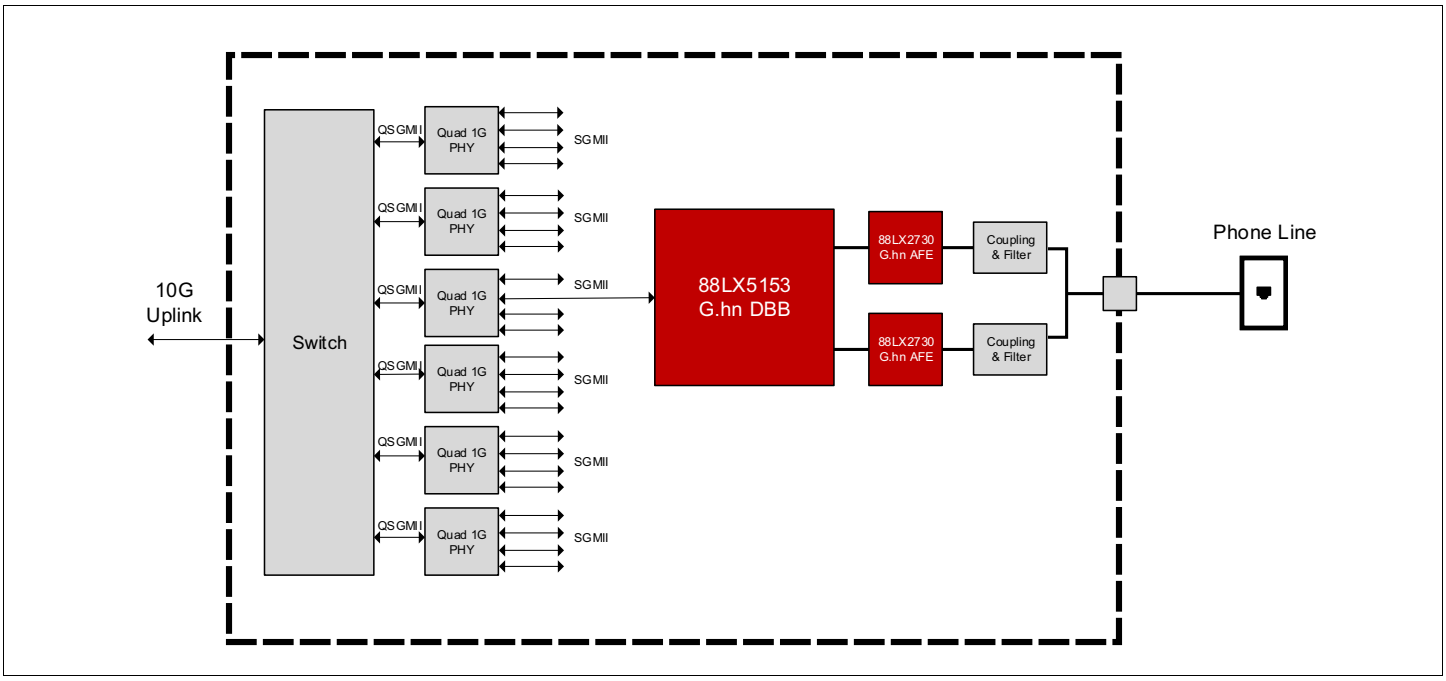

Figure 11: GAM Implementation Example Block Diagram

Embedded Communication Module for Industrial Applications

The G.hn PLC smart grid application embeddable module is a SISO based design that uses the industrial temperature range chipset 88LX5153A and 88LX2741. It is suitable for industrial applications such as automatic metering reading (AMR), street lighting, smart elevators, or lighting control.

The following figure shows a block diagram of an industrial module example with internal power scheme that is based on Maxlinear's power management parts.

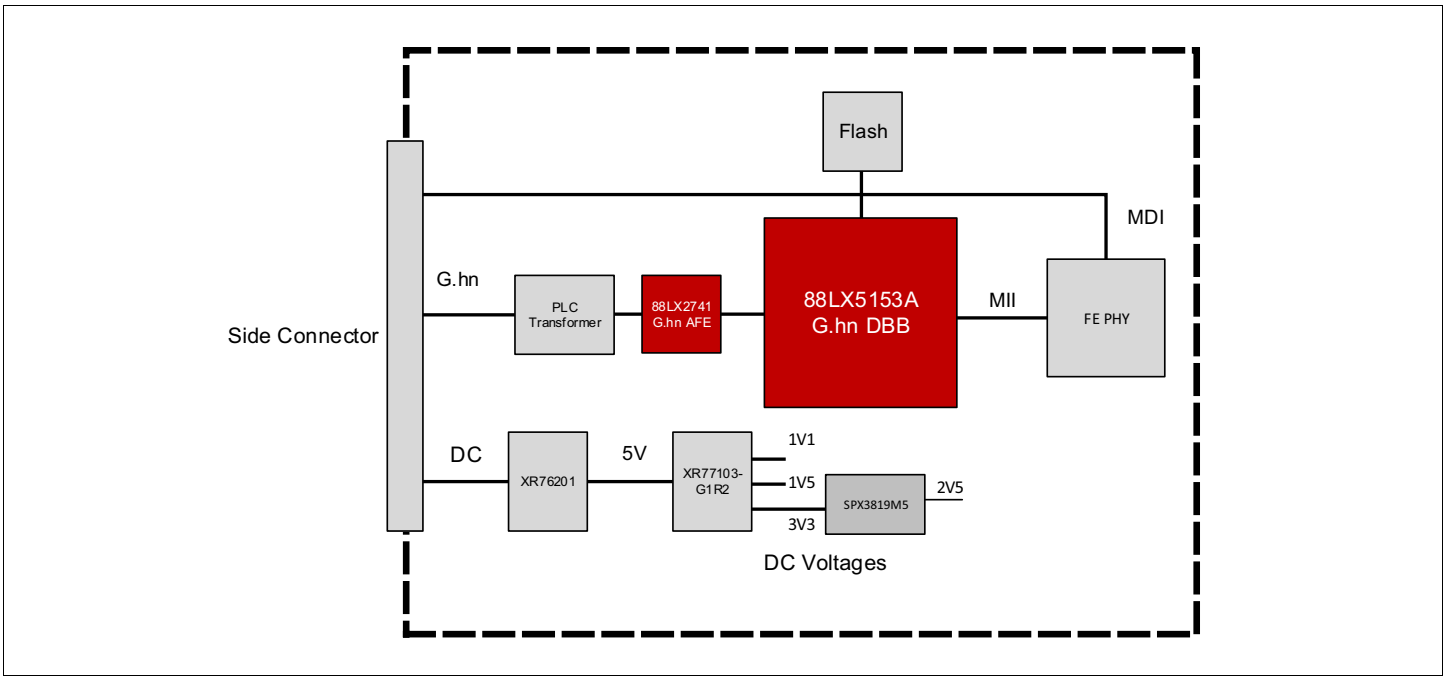

Figure 12: Industrial Module Example Block Diagram

G.hn Fiber Extenders

The G.hn DPU application is a flexible design to allow multiple FTT configurations including the G.hn chipset, high end switching, and a CPU to support MDU access scenarios over existing coaxial (point to point or point to multipoint scenarios) or phone lines (point to point connections in crosstalk scenario).

The following figures show examples of block diagrams of a DPU implementation.

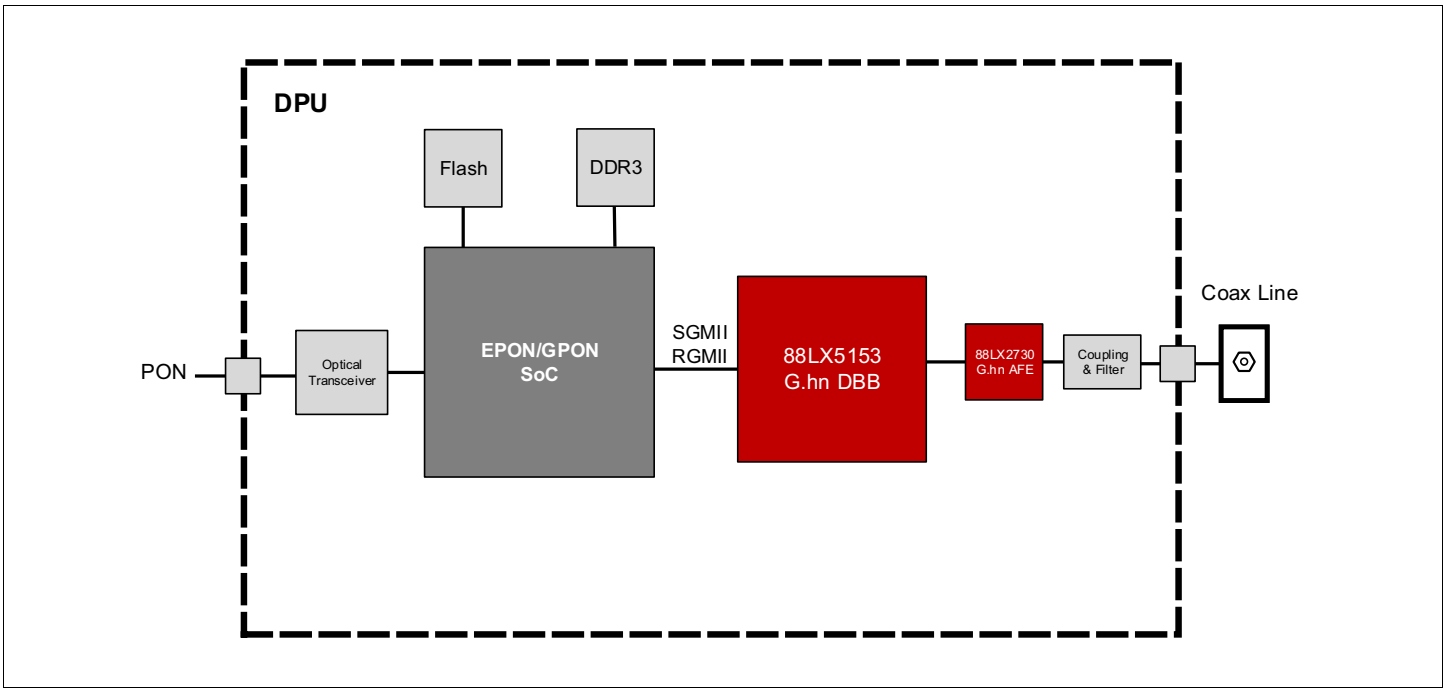

Figure 13: Small DPU Point-to-Multipoint over Coaxial Serving up to 16 Subscribers

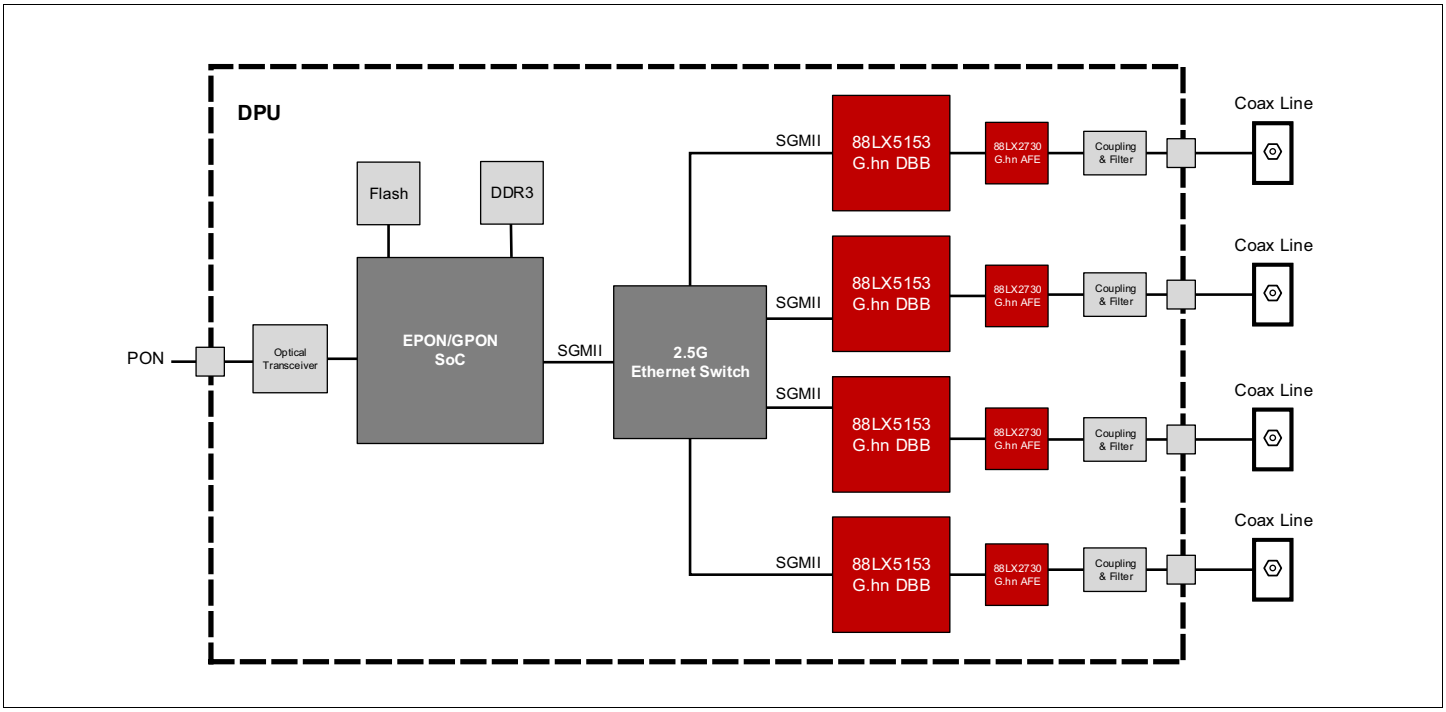

Figure 14: Medium DPU Point-to-Multipoint over Coaxial Serving up to 4 × 16 = 64 Subscribers

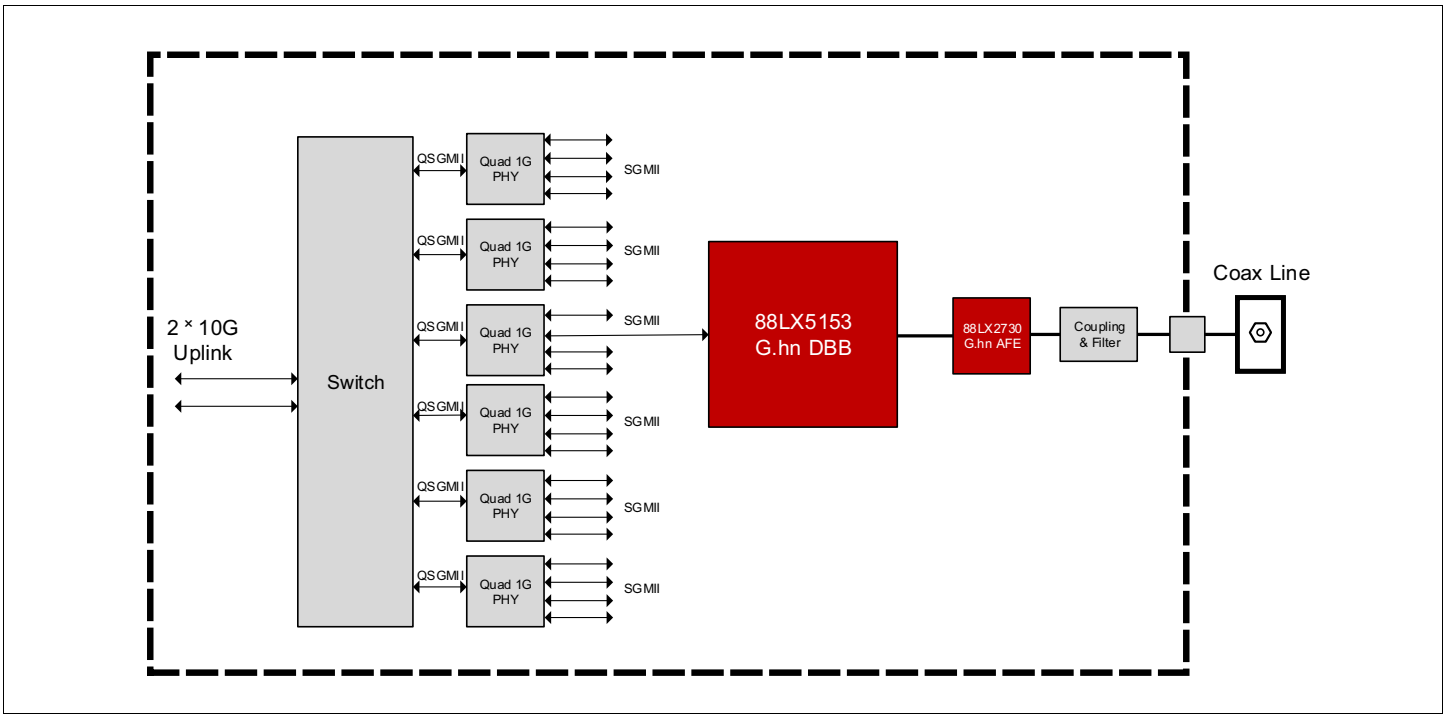

Figure 15: Large DPU Point-to-Multipoint over Coaxial Serving up to 24 × 16 = 384 Subscribers

G.9991 LiFi Access Point and End Point

The G.9991 LiFi access point and end point are a stand-alone application that contain the G.9991 chipset (88LX5153 and 88LX2730), a power supply, and an optical transceiver (for example, IR LED, visible light LED) in a single platform. It enables a wirelessly high speed secure network that uses infrared and/or visible light spectrum. For more information, refer to the *G.9991 ITU-T Recommendation*.

The access point is placed in a lightning device and connected to the backhaul through an Ethernet interface. The access point can communicate with up to 16 end points through LiFi communication.

The following figure shows a block diagram example of the G.9991 LiFi access point.

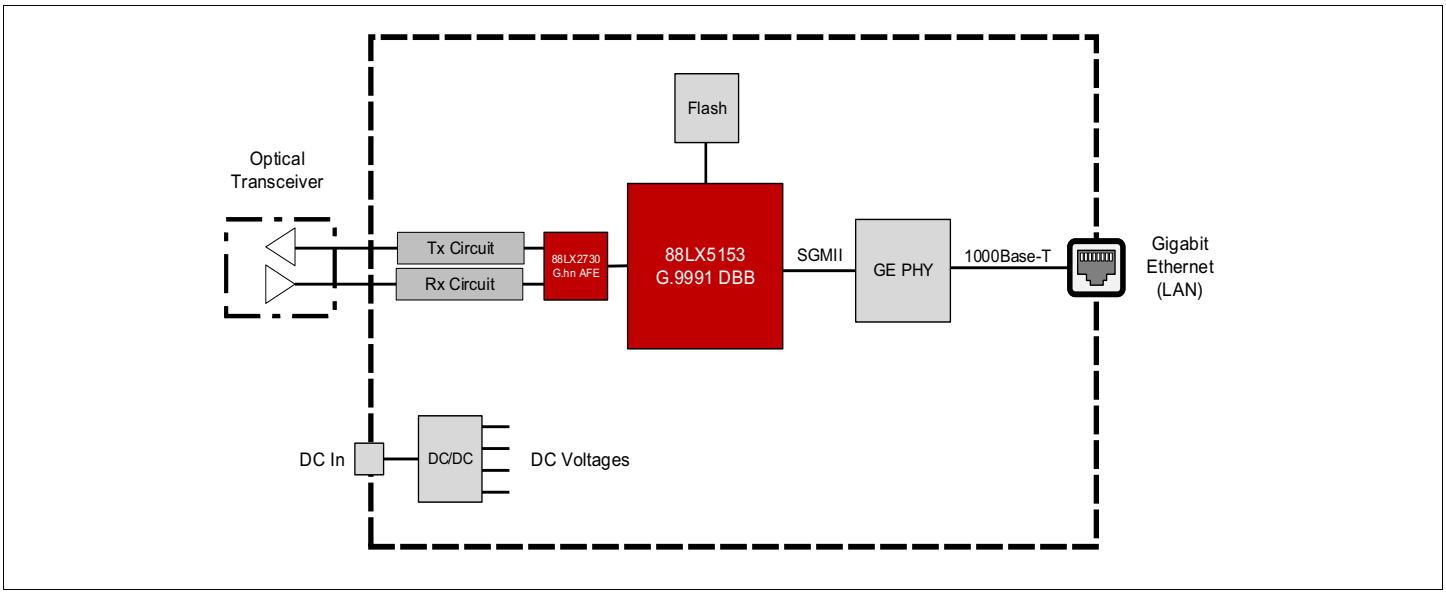

Figure 16: LiFi Access Point Enclosed

The following figure shows a block diagram example of the G.9991 LiFi end point.

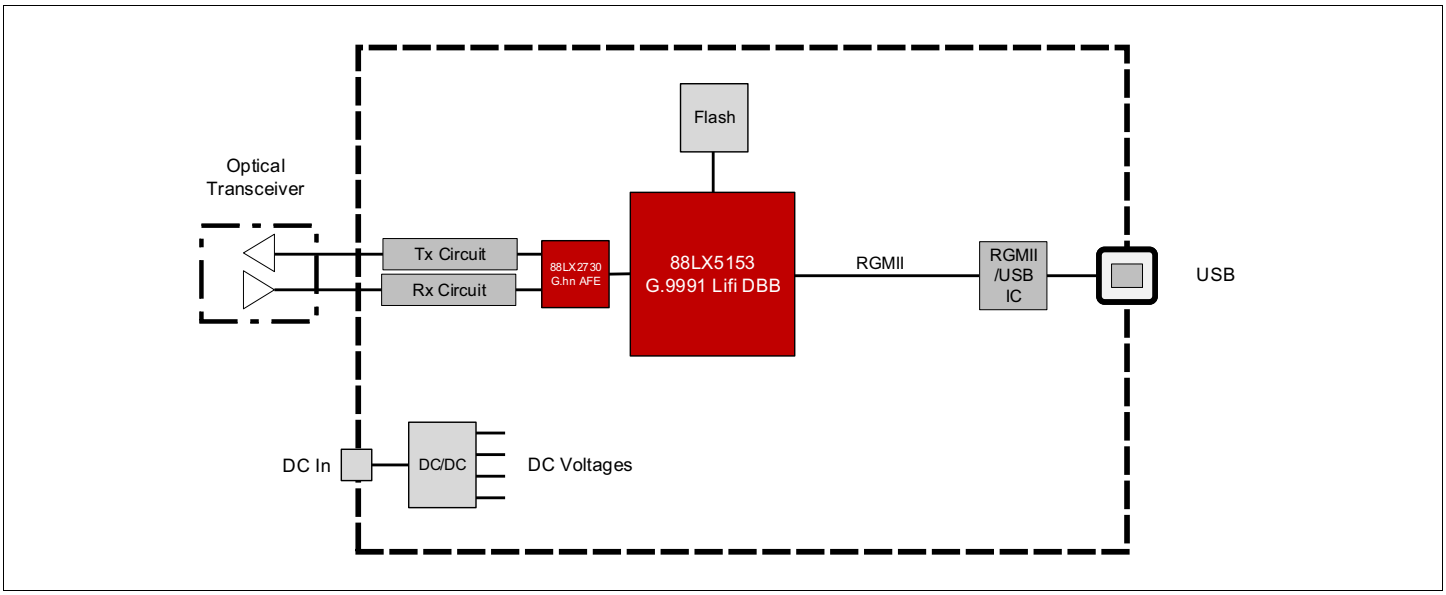

Figure 17: LiFi End Point Enclosed

Pin Information

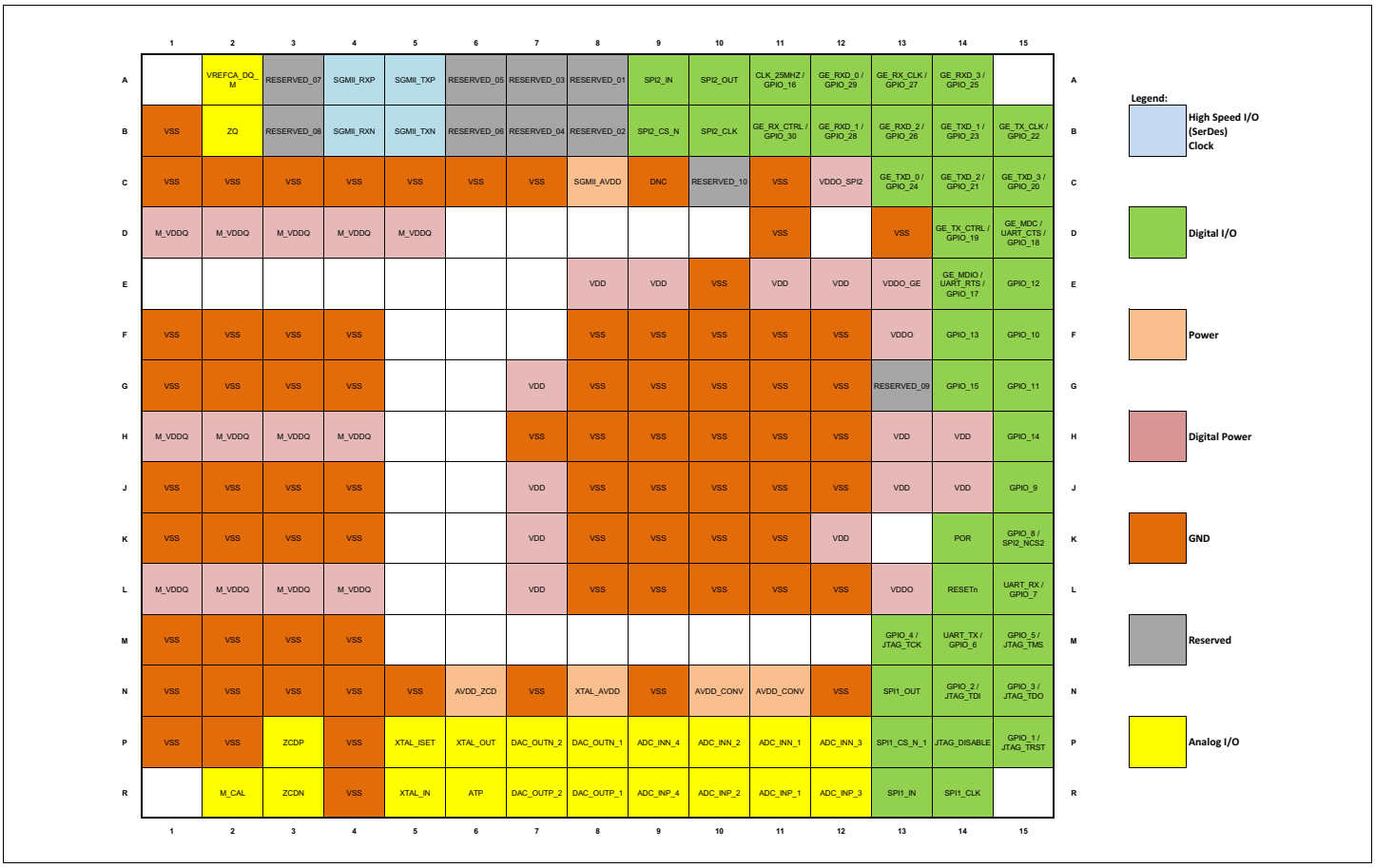

Figure 18: 88LX5152 and 88LX5153 186-Pin TFBGA Package

Pin Description

Table 2: Signal Pin List Sorted Alphabetically

Pin #	Signal Name
P11	ADC_INN_1
P10	ADC_INN_2
P12	ADC_INN_3
P9	ADC_INN_4
R11	ADC_INP_1
R10	ADC_INP_2
R12	ADC_INP_3
R9	ADC_INP_4
R6	ATP
A11	CLK_25MHZ/GPIO_16
P8	DAC_OUTN_1
P7	DAC_OUTN_2
R8	DAC_OUTP_1
R7	DAC_OUTP_2
C9	DNC
D15	GE_MDC/UART_CTS/GPIO_18
E14	GE_MDIO/UART_RTS/GPIO_17
A13	GE_RX_CLK/GPIO_27
B11	GE_RX_CTRL/GPIO_30
A12	GE_RXD_0/GPIO_29
B12	GE_RXD_1/GPIO_28
B13	GE_RXD_2/GPIO_26
A14	GE_RXD_3/GPIO_25
B15	GE_TX_CLK/GPIO_22
D14	GE_TX_CTRL/GPIO_19
C13	GE_TXD_0/GPIO_24
B14	GE_TXD_1/GPIO_23
C14	GE_TXD_2/GPIO_21
C15	GE_TXD_3/GPIO_20
P15	GPIO_1/JTAG_TRST
F15	GPIO_10
G15	GPIO_11
E15	GPIO_12
F14	GPIO_13
H15	GPIO_14
G14	GPIO_15
P5	XTAL_ISET

Pin #	Signal Name
N14	GPIO_2/JTAG_TDI
N15	GPIO_3/JTAG_TDO
M13	GPIO_4/JTAG_TCK
M15	GPIO_5/JTAG_TMS
K15	GPIO_8/SPI2_NCS2
J15	GPIO_9
P14	JTAG_DISABLE
R2	M_CAL
K14	POR
A8	RESERVED_01
B8	RESERVED_02
A7	RESERVED_03
B7	RESERVED_04
A6	RESERVED_05
B6	RESERVED_06
A3	RESERVED_07
B3	RESERVED_08
G13	RESERVED_09
C10	RESERVED_10
L14	RESETn
B4	SGMII_RXN
A4	SGMII_RXP
B5	SGMII_TXN
A5	SGMII_TXP
R14	SPI1_CLK
P13	SPI1_CS_N_1
R13	SPI1_IN
N13	SPI1_OUT
B10	SPI2_CLK
B9	SPI2_CS_N
A9	SPI2_IN
A10	SPI2_OUT
L15	UART_RX/GPIO_7
M14	UART_TX/GPIO_6
A2	VREFCA_DQ_M
R5	XTAL_IN
P3	ZCDP

Table 2: Signal Pin List Sorted Alphabetically

Pin #	Signal Name	Pin #	Signal Name
P6	XTAL_OUT	B2	ZQ
R3	ZCDN		

Table 3: Power Pin List Sorted Alphabetically

Pin #	Power Group
N10, N11	AVDD_CONV
N8	AVDD_PLL
N6	AVDD_ZCD
D1, D2, D3, D4, D5, H1, H2, H3, H4, L1, L2, L3, L4	M_VDDQ
C8	SGMII_AVDD
E11, E12, E8, E9, G7, H13, H14, J13, J14, J7, K12, K7, L7	VDD
F13, L13	VDDO
E13	VDDO_GE
C12	VDDO_SPI2
B1, C1, C11, C2, C3, C4, C5, C6, C7, D11, D13, E10, F1, F10, F11, F12, F2, F3, F4, F8, F9, G1, G10, G11, G12, G2, G3, G4, G8, G9, H10, H11, H12, H7, H8, H9, J1, J10, J11, J12, J2, J3, J4, J8, J9, K1, K10, K11, K2, K3, K4, K8, K9, L10, L11, L12, L8, L9, M1, M2, M3, M4, N1, N12, N2, N3, N4, N5, N7, N9, P1, P2, P4, R4	VSS

Chip Configuration Pins

The following table lists the pins used to configure the device's operating mode, which are sampled on the rising edge of RESETn.

- Internal weak pull-up resistors: Set the default mode of operation to *high*.
- External pull-down resistors: Required to change the default mode to *low* (use recommended 4.7kΩ resistor connected to VSS).

The I/O pins must remain pulled up or pulled down until RESETn de-assertion.

Caution: Do not connect drivers to any of the listed device configuration pins. The drivers can affect the level of the pin at the time the reset is de-asserted, which can cause unexpected behavior of the device. The feature set can vary depending on the firmware version.

Table 4: Chip Configuration Pins

Pin Name	Description	Description
GE_TXD_0/GPIO_24 GE_TXD_1/GPIO_23 GE_TXD_2/GPIO_21 GE_TXD_3/GPIO_20	MII_CONF_0 MII_CONF_1 MII_CONF_2 MII_CONF_3	■ Configures the Ethernet boot mode. ■ One connectionless port for registration. ■ MII_CONF[3:0]: • 0b0000: Reserved. • 0b0001: SGMII media, with auto-negotiation (Cisco specification). • 0b0010: MAC mode with external PHY on MII, with auto-negotiation. • 0b0011: PHY mode on RGMII, 1000Mbps full-duplex, delay of 0 always without auto-negotiation. • 0b0100: PHY mode on MII, 100Mbps full-duplex, without auto-negotiation. • 0b0101: PHY mode on RGMII, 1000Mbps full-duplex, delay of 1 always without auto-negotiation. • 0b0110: Reserved. • 0b0111: MAC mode with external PHY on RGMII, 100Mbps, delay of 1, with auto-negotiation. • 0b1000: Reserved. • 0b1001: SGMII mode 2500BASE-X. • 0b1010: MAC mode with external PHY on RGMII, 100/1000Mbps, delay of 0, with auto-negotiation. • 0b1011: SGMII mode system (PHY) 1000Mbps • 0b1100: PHY mode on RGMII, 100Mbps full-duplex, delay of 0 always without auto-negotiation. • 0b1101: SGMII mode 1000BASE-X. • 0b1110: PHY mode on RGMII, 100Mbps full-duplex, delay of 1, always without auto-negotiation. • 0b1111: SGMII mode for 88E1514.
GPIO_9	SPI_BOOT_ENABLE	Enables/disables the boot from the SPI flash memory. ■ High: Boot from the flash memory. ■ Low: Boot from the Ethernet interface by using the mode that is configured with the strapping pins.
SPI2_OUT SPI2_CLK	RGMII_POWER_LEVEL_1 RGMII_POWER_LEVEL_2	Configures the RGMII pins' voltage level. RGMII_POWER_LEVEL_[2:1]: ■ 0b01 = 2V5 ■ 0b10 = 1V8
SPI1_OUT	HALT_ON_RESETn	Enables/disables the CPU being stopped after reset. ■ High: Disable (default). ■ Low: Enable (used for debugging).
SPI1_CLK	JTAG_TAP_CPU	Enables/disables the CPU JTAG. ■ High: Enable (default) ■ Low: Disable (the boundary scan TAP JTAG)

Pinout and Signal Description

Overview

This section describes the signals and pins of the 88LX5152 and 88LX5153. The pins can be divided into the following categories:

- Power pins.
- Dedicated I/O pins.
- Multifunction I/O pins.

Signal Description

This section describes the signals of the 88LX5152 and 88LX5153. Signals can either have dedicated pins or are available only as alternate function of a multifunction pin. The functionality of the multifunction pins is configured by firmware. The power pins are also described as signals in this section. The following table lists the signal types of the 88LX5152 and 88LX5153.

Table 5: Signal Types

Pin Type	Definition
A, I	Analog Input
A, O	Analog Output
A, IO	Analog Input/Output
DNC	Do not Connect
GND	Ground
I	Digital Input
I/O	Digital I/O
N	Active Low
O	Digital Output
OD	Open Drain
PD	Internal Pull-Down
PU	Internal Pull-Up
PWR	Power Supply
Z	Tri-state Output

GPIO Interface

Table 6: GPIO Interface

Pin #	Pin Name	Power Group	Type	Description
P15	**GPIO_1**/JTAG_TRST	VDDO	I/O, PD	**GPIO**. Can be defined individually as either input or output, and is multiplexed with other functions.
M14	UART_TX/**GPIO_6**	VDDO	I/O	
K15	**GPIO_8**/SPI_NCS2			
F15	GPIO_10			
G15	GPIO_11			
E15	GPIO_12			
F14	GPIO_13			
H15	GPIO_14			
G14	GPIO_15			
N14	**GPIO_2**/JTAG_TDI	VDDO	I/O, PU	
N15	**GPIO_3**/JTAG_TDO			
M13	**GPIO_4**/JTAG_TCK			
M15	**GPIO_5**/JTAG_TMS			
L15	UART_RX/**GPIO_7**			
A11	CLK_25MHZ/**GPIO_16**	VDDO_GE	I/O	
D14	GE_TX_CTRL/**GPIO_19**			
B15	GE_TX_CLK/**GPIO_22**			
E14	GE_MDIO/UART_RTS/ **GPIO_17**	VDDO_GE	I/O, PU	
D15	GE_MDC/UART_CTS/ **GPIO_18**			
A14	GE_RXD3/**GPIO_25**			
B13	GE_RXD2/**GPIO_26**			
A13	GE_RX_CLK/**GPIO_27**			
B12	GE_RXD1/**GPIO_28**			
A12	GE_RXD0/**GPIO_29**			
B11	GE_RX_CTRL/**GPIO_30**			
J15	GPIO_9	VDDO	I/O, PU	**GPIO**. Can be defined individually as either input or output. Theses pins are used to configure the device at start-up. When the RESETn pin is asserted, it becomes input, and configuration information is latched on the rising edge of RESETn. MaxLinear does not recommend connecting a driver to this pin. For more information about the use at reset, see “Pin Description” on page 21.
C15	GE_TXD3/**GPIO_20**	VDDO_GE	I/O, PU	
C14	GE_TXD2/**GPIO_21**			
B14	GE_TXD1/**GPIO_23**			
C13	GE_TXD0/**GPIO_24**			

UART Interface

Table 7: UART Interface

Pin #	Pin Name	Power Group	Type	Description
D15	**UART_CTS**/GE_MDC/ GPIO_18	VDDO_GE	I, PU	**UART CTS Input.** The input control signal to the extended UART. This pin can be used as GE_MDC or GPIO if the UART is not needed or not extended. The default functionality is GE_MDC. This pin is internally pulled high, so it can be left unconnected if not used.
E14	**UART_RTS**/GE_MDIO/ GPIO_17	VDDO_GE	O, PU	**UART RTS Output**. The output control signal from the extended UART. This pin can be used as GE_MDIO or GPIO if the UART is not needed or not extended. The default functionality is GE_MDIO. This pin is internally pulled high, so it can be left unconnected if not used.
L15	**UART_RX**/GPIO_7	VDDO	I, PU	**UART Rx Input**. The input to the general purpose UART. This pin can be used as GPIO if the UART is not needed. The default functionality is UART_RX. This pin is internally pulled high, so it can be left unconnected if not used.
M14	**UART_TX**/GPIO_6	VDDO	O	**UART Tx Output.** The output from the general purpose UART. This pin can be used as GPIO if the UART is not needed. The default functionality is UART_RX.

Note: UART_CTS and UART_RTS are supplied from VDDO_GE power group that is shared with the RGMII bus.

SMI

The SMI is a serial synchronous interface.

Table 8: SMI for RGMII/MII

Pin #	Pin Name	Type	Description
D15	**GE_MDC**/UART_CTS/ GPIO_18	I/O, PU	**Management Data Clock for the SMI.** The SMI works as a: ■ Master: Pin is the output reference clock for GE_MDIO ■ Slave: Pin is input reference clock for GE_MDIO This pin can be used as a UART_CTS or GPIO if the SMI is not needed. The default functionality is GE_MDC. This pin is internally pulled high, so it can be left unconnected if not used.
E14	**GE_MDIO**/UART_RTS/ GPIO_17	I/O, PU	**Management Data I/O for the SMI.** Used to transfer management data in and out of the device synchronously to GE_MDC. This pin can be used a UART_RTS or GPIO if the SMI is not needed. The default functionality is GE_MDIO. This pin is internally pulled high, so it can be left unconnected if not used.

Note: At boot time:

- The SMI bus works as master when the RGMII/MII is in MAC mode.
- The SMI bus works as slave when the RGMII/MII is in PHY mode following the configuration defined with the strapping pins.

After the firmware starts, the SMI can be configured independently of the RGMII/MII mode.

When the SMI bus operates as slave, the device responds on address 0. When the firmware is started, the address can be changed.

The SMI only supports Clause 22 addressing.

The SMI pins are supplied from VDDO_GE power pins and have the same voltage level as GPIO 19-30 corresponding to RGMII interface. When using an Ethernet transceiver connected to the SGMII bus make sure that VDDO_GE has a voltage level that is suitable for such transceiver. If GPIO 19-30 are used for other purposes, make sure that the voltage level is suitable for both purposes.

RGMII/MII

The RGMII/MII has the following characteristics:

- MII mode: 2.5MHz/25MHz single data rate. The clock is driven by the PHY.
- RGMII mode: 125MHz double data rate or 2.5MHz/25MHz single data rate. The clock is driven by the data source.
- Optional 2ns skew on clock signals in RGMII mode. Configurable by strapping pins.
- Half-duplex mode not supported.

Note:

- For all of the RGMII/MII multifunction pins, the default functionality is RGMII/MII.If you need to use the RGMII/MII and SGMII interfaces simultaneously, contact MaxLinear's Customer Technical Support to evaluate the specific user case.

These pins are supplied from power group VDDO_GE.

Table 9: RGMII

Pin #	Pin Name	Type	Description
A12 B12 B13 A14	**GE_RXD_0**/GPIO_29 **GE_RXD_1**/GPIO_28 **GE_RXD_2**/GPIO_26 **GE_RXD_3**/GPIO_25	I, PU	**RGMII Rx Data**. The input data pins are synchronous to GE_RX_CLK. This pin can also be used as GPIO. These pins are internally pulled high, so they can be left unconnected if not used.
A13	**GE_RX_CLK**/GPIO_27	I, PU	**RGMII Rx Clock.** Continuous clock input to the device. The clock frequency can be 125MHz, 25MHz, or 2.5MHz, depending on Ethernet speed. This pin can also be used as a GPIO. This pin is internally pulled high, so it can be left unconnected if not used.
B11	**GE_RX_CTRL**/GPIO_30	I, PU	**RGMII Rx Control.** Input Ethernet data control signal. This pin can also be used as a GPIO. This pin is internally pulled high, so it can be left unconnected if not used.
B14 C13 C14 C15	**GE_TXD_1**/GPIO_23 **GE_TXD_0**/GPIO_24 **GE_TXD_2**/GPIO_21 **GE_TXD_3**/GPIO_20	O, PU	**RGMII Tx Data.** Output data pins that are synchronous to GE_TX_CLK. This pin can also be used as GPIO. These pins are internally pulled high, so they can be left unconnected if not used. These pins are used to configure the device at start-up. When the RESETn pin is asserted, they become input and the configuration information is latched on the rising edge of RESETn. MaxLinear does not recommend connecting a driver on these lines. For more information about the use of these pins at reset, see "Pin Description" on page 21.
B15	**GE_TX_CLK**/GPIO_22	O	**RGMII Tx Clock.** Continuous clock output driven by the device. The clock frequency can be 125MHz, 25MHz, or 2.5MHz, depending on Ethernet speed. This pin can also be used as a GPIO.
D14	**GE_TX_CTRL**/GPIO_19	O	**RGMII Tx Control**. Output Ethernet data control signal. This pin can also be used as a GPIO.

Table 10: MII

Pin #	Pin Name	Type	Description
A12 B12 B13 A14	GE_RXD_0/GPIO_29 GE_RXD_1/GPIO_28 GE_RXD_2/GPIO_26 **GE_RXD_3**/GPIO_25	I, PU	**MII MAC Rx Data.** These four pins represent the data transmitted by the PHY to the device, and are synchronous with GE_RX_CLK. **MII PHY Tx Data.** These four pins represent the data transmitted by the MAC to the device, and are synchronous with GE_RX_CLK. These pins can also be used as GPIO. These pins are internally pulled high, so they can be left unconnected if not used.
A13	**GE_RX_CLK**/GPIO_27	I/O, PU	**MII MAC Rx Clock.** A continuous clock input driven by the external PHY. The clock's frequency can be 25MHz for 100Mbps or 2.5MHz for 10Mbps. **MII PHY Tx Clock.** A continuous clock output driven by the device. The clock's frequency can be 25MHz for 100Mbps or 2.5MHz for 10Mbps. This pin can also be used as a GPIO. This pin is internally pulled high, so it can be left unconnected if not used.
B11	**GE_RX_CTRL**/GPIO_30	I, PU	**MII MAC Rx Data Valid.** An active-high input. When active, this pin indicates valid data on GE_RXD_[3:0]. This pin is synchronous with GE_RX_CLK. **MII PHY Tx Enable**. An active-high input. When active, this pin indicates valid data on GE_RXD_[3:0]. This pin is synchronous with GE_RX_CLK. This pin can also be used as a GPIO. This pin is internally pulled high, so it can be left unconnected if not used.
B14 C13 C14 C15	GE_TXD_1/GPIO_23 GE_TXD_0/GPIO_24 GE_TXD_2/GPIO_21 **GE_TXD_3**/GPIO_20	O, PU	**MAC Tx Data.** These four pins represent the data transmitted by the device to the PHY, and are synchronous with GE_TX_CLK. **MII PHY Rx Data.** These four pins represent the data transmitted by the device to the MAC, and are synchronous with GE_TX_CLK. These pins can also be used as GPIO. These pins are used to configure the device at start-up. When the RESETn pin is asserted, this pin becomes input and the configuration information is latched on the rising edge of RESETn. For more information, see "Pin Description" on page 21. These pins are internally pulled high, so they can be left unconnected if not used
B15	**GE_TX_CLK**/GPIO_22	I/O	**MII MAC Tx Clock**. A continuous clock input driven by the external PHY. The clock's frequency can be 25MHz for 100Mbps or 2.5MHz for 10Mbps. **MII PHY Rx Clock.** A continuous clock output driven by the device. The clock's frequency can be 25MHz for 100Mbps or 2.5MHz for 10Mbps. This pin can also be used as a GPIO.
D14	**GE_TX_CTRL**/GPIO_19	O	**MII MAC Tx Enable.** An active-high output. When active, it indicates valid data on GE_TXD_[3:0]. This pin is synchronous with GE_TX_CLK. **MII PHY Rx Data Valid.** An active-high output. When active, it indicates valid data on GE_TXD_[3:0]. This pin is synchronous with GE_TX_CLK. This pin can also be used as a GPIO.

SPIs

The 88LX5152 and 88LX5153 has two SPIs:

- SPI 1: For AFE (88LX27x0) control.
- SPI 2: For serial flash memory and general purpose.

SPI 1

SPI 1 is a four-wire serial interface similar to SPI. This interface is specifically designed to work with 88LX27x0 AFEs.

The information provided in this section is only informative and not intended to explain the use of this bus for other SPI devices. This bus has the following characteristics:

- The 88LX5152 and 88LX5153 acts as the master and drives the clock line always.
- Clock frequency for write operations is 100MHz.
- Clock frequency for read operations is 25MHz.

Two operating modes supported:

- Single mode: In this mode only the SPI_OUT pin is used to send information to the AFE device. The SPI1_IN pin remains in high impedance during write operations inputs data during read operations. This mode is equivalent to the standard SPI mode 3 (CPOL=1, CPHA=1).

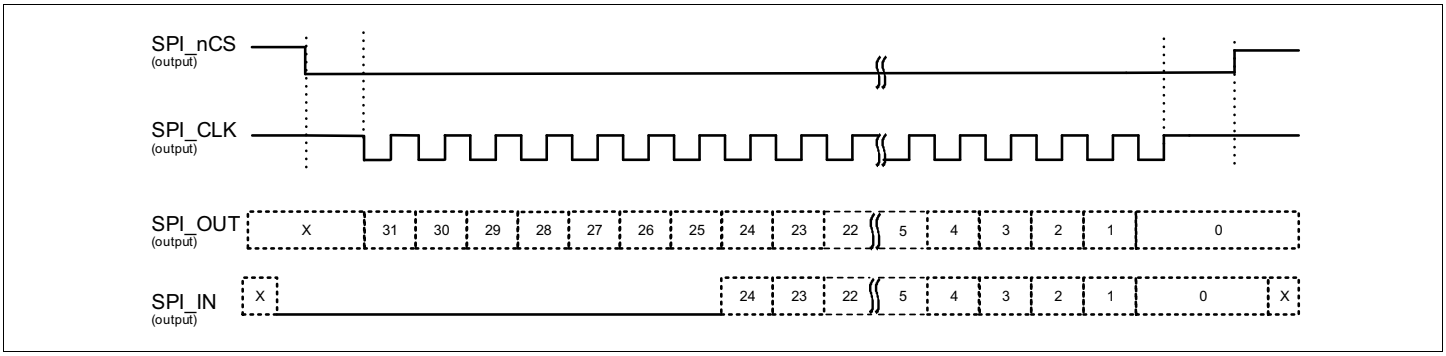

Figure 19: SPI1 Single Mode

- Parallel mode: In this mode the SPI_IN pin becomes an output and works in parallel with SPI_OUT, doubling the data rate and reducing the duration of the frame by half. The change to parallel mode is configured in one of the AFE registers during a previous single mode transaction.

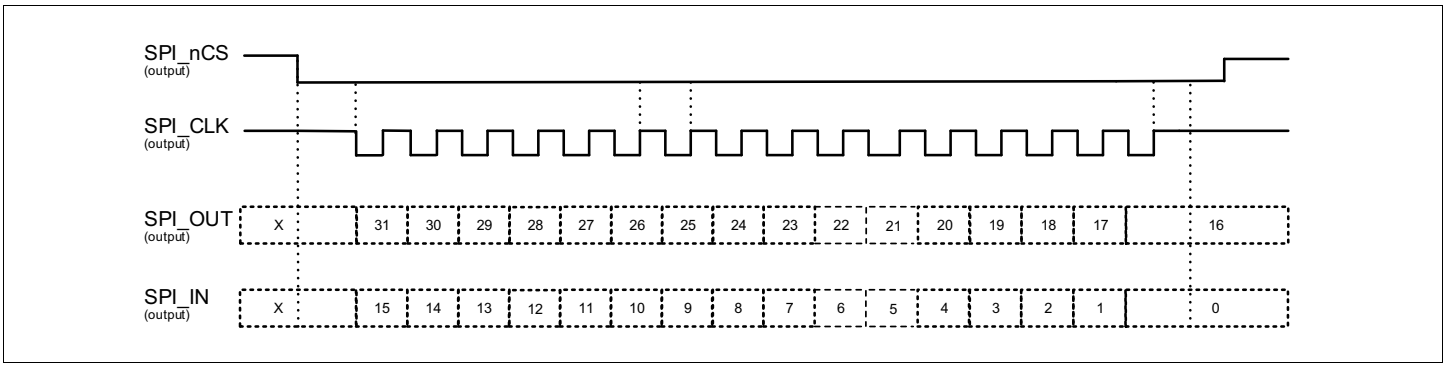

Figure 20: SPI1 Parallel Mode

SPI1_IN remains in high impedance when SPI1_CS_N_1 is not asserted. The biasing of the line is assured by the internal pull-up resistors of the AFE and the DBB devices.

When more than one AFE is used in a product, the SPI lines should be routed in a T shape with the branches reaching each chip having the same length.

SPI1 lines are supplied from VDDO power group. This bus is used to interface to 88LX27x0 AFE exclusively and VDDO voltage must be 3.3V.

Table 11: SPI 1

Pin #	Pin Name	Type	Description
N13	SPI1_OUT	O, PU	**SPI Data Output.** Used to transfer data serially out of the device. This pin is used to configure the device at start-up. When the RESETn pin is asserted, this pin becomes input and the configuration information is latched on the rising edge of RESETn. For more information, see “Pin Description” on page 21. This pin is internally pulled high, so it can be left floating for a configuration high.
R13	SPI1_IN	I/O, PU	**SPI Data Input.** Used to transfer data serially into the device. Used as an output when the SPI works in parallel mode. This pin is internally pulled high.
P13	SPI1_CS_N_1	O, PU, N	**SPI Chip Select**. Provides the active-low chip select for the AFE. This pin is internally pulled high. An external pull-down is not allowed.
R14	SPI1_CLK	O, PU	**SPI Clock.** Provides the non-continuous timing reference for the first serial interface. This pin is used to configure the device at start-up. When the RESETn pin is asserted, this pin becomes input and the configuration information is latched on the rising edge of RESETn. For more information, see “Pin Description” on page 21. This pin is internally pulled high, so it can be left floating for a configuration high.

SPI 2

SPI 2 is a fully compatible SPI bus supporting the four operating modes. This bus has the following characteristics:

- Clock frequency up to 50MHz.
- Optional chip select pin; can also be used with other peripherals.
- 88LX5152 and 88LX5153 acts as the master only.
- Clock is driven by the88LX5152 and 88LX5153.

Table 12: SPI 2

Pin #	Pin Name	Type	Description
A9	SPI2_IN	I, PU	**SPI Data Input.** Used to transfer data serially into the device. This pin is internally pulled high.
A10	SPI2_OUT	O, PU	**SPI Data Output.** Used to transfer data serially out of the device. This pin is used to configure the device at start-up. When the RESETn pin is asserted, this pin becomes input and the configuration information is latched on the rising edge of RESETn. For more information, see “Pin Description” on page 21. This pin is internally pulled high, so it can be left floating for a configuration high.
B9	SPI2_CS_N	O, PU, N	**SPI Chip Select.** Provides the active-low chip select for the external device (typically used for a serial flash memory). This pin is internally pulled high. An external pull-down is not allowed.
B10	SPI2_CLK	O, PU	**SPI Clock.** Provides the non-continuous timing reference for the second serial interface. This pin is used to configure the device at start-up. When the RESETn pin is asserted, this pin becomes input and the configuration information is latched on the rising edge of RESETn. For more information, see “Pin Description” on page 21. This pin is internally pulled high, so it can be left floating for a configuration high.
K15	GPIO_8/**SPI2_NCS2**	I/O, PU	**Secondary SPI Chip Select**. Can also be used as GPIO. The default functionality is GPIO.

SPI 2 bus is supplied from VDDO_SPI2 power group.

SGMII

The SGMII has the following characteristics:

- Serial Ethernet interface, up to 2.5Gbps, full duplex.
- Clock encoded (for example, no dedicated signal).
- One differential pair for each Tx and Rx.
- Supports auto-negotiation.

Table 13: SGMII

Pin #	Pin Name	Type	Description
A4	SGMII_RXP	I	**SGMII Rx.** Differential pair of positive and negative bi-directional signal lines.
B4	SGMII_RXN	I	
A5	SGMII_TXP	O	**SGMII Tx.** Differential pair of positive and negative bi-directional signal lines.
B5	SGMII_TXN	O	

Note: RGMII/MII interface and SGMII interface cannot be used simultaneously. For further information contact MaxLinear's Customer Technical Support.

SGMII interface is supplied from SGMII_AVDD power group. This power supply must be decoupled down to 300kHz.

ADC/DAC Interface

The 88LX5152 and 88LX5153 has two ADC interfaces and one DAC interface with the following characteristics:

- DAC interface: Differential current output.
- ADC interfaces: DC coupled differential voltage inputs.
- 1.5V power supply.

Table 14: ADC/DAC Interface

Pin #	Pin Name	Type	Description
P9 P10 P11 P12	ADC_INN_4 ADC_INN_2 ADC_INN_1 ADC_INN_3	A, I	**ADC negative input.**
R9 R11 R12 R10	ADC_INP_4 ADC_INP_1 ADC_INP_3 ADC_INP_2	A, I	**ADC positive input.**
P7 P8	DAC_OUTN_2 DAC_OUTN_1	A, O	**DAC negative output.**
R7 R8	DAC_OUTP_2 DAC_OUTP_1	A, O	**DAC positive output.**

ADC and DAC converters are supplied from AVDD_CONV power group. This power supply must be decoupled in the band of the G.hn signal.

JTAG Interface

The JTAG interface has the following characteristics:

- Two different JTAG modes:
  - Boundary scan mode.
  - CPU debug port mode.
- Mode selection is performed during the reset release with a strapping pin (also see "Pin Description" on page 21).

Table 15: JTAG Interface

Pin #	Pin Name	Type	Description
M13	GPIO_4/**JTAG_TCK**	I, PU	**JTAG Test Clock.** In debug mode, this pin is the input clock timing reference for the JTAG test logic. This pin can also be used as GPIO. The default functionality is GPIO. This pin is internally pulled high, so it can be left unconnected if not used.
M15	GPIO_5/**JTAG_TMS**	I, PU	**JTAG Test Mode Select.** In debug mode, this pin is the JTAG test mode select input used by the TAP controller to control test operations. This pin can also be used as GPIO. The default functionality is GPIO. This pin is internally pulled high, so it can be left unconnected if not used.
N14	GPIO_2/**JTAG_TDI**	I, PU	**JTAG Test Data Input or GPIO.** In debug mode, this pin is the JTAG test serial data input, which is sampled on the rising edge of JTAG_TCK to receive the serial test instructions and data. This pin can also be used as GPIO. The default functionality is GPIO. This pin is internally pulled high, so it can be left unconnected if not used.
N15	GPIO_3/**JTAG_TDO**	O, PU	**JTAG Test Data Output.** In debug mode, this pin is the JTAG test reset serial data output, which is sampled on the rising edge of JTAG_TCK to transmit the serial test instructions and data as set by the test logic. This pin can also be used as GPIO. The default functionality is GPIO. This pin is internally pulled high, so it can be left unconnected if not used.
P14	JTAG_DISABLE	I, PU	**JTAG Disable.** Used to disable JTAG functionality while the JTAG interface is not connected. This pin can also be used as GPIO. The default functionality is JTAG_DISABLE. This pin must be tied low when the JTAG connector is plugged in, and kept tied high externally when the JTAG connector is unplugged.
P15	GPIO_1/**JTAG_TRST**	O, PD	**JTAG Test Reset.** In debug mode, this pin is the JTAG test reset input. This pin can also be used as GPIO. The default functionality is GPIO. If the JTAG interface is enabled, this pin must be driven low to reset the internal TAP (if the JTAG interface is disabled, the TAP reset is internally forced). This pin is internally pulled down, so it can be left unconnected if not used.

This interface is supplied from VDDO power group.

Zero Cross Detector Interface

The Zero-Cross Detector (ZCD) interface is used to:

- Determine the frequency and the phase of the AC supply voltage with high accuracy, which is required for PLC communication.
- Align the MAC cycle among several masters in G.now applications.

The ZCD interface can be configured as a single-ended digital input or an analog differential input.

Table 16: ZCD Interface

Pin #	Pin Name	Type	Description
P3	ZCDP	I	**ZCD Differential Input (Positive).** If the ZCD differential N input is not used, then this pin can be used as ZCD single-ended input.
R3	ZCDN	I	**ZCD Differential Input (Negative).**

Note: The operating mode of the ZCD (single-ended or differential) is pre-configured in the firmware per reference design. In case the design is modified, the operating mode can be changed using a configuration tool (PCK).

This interface is supplied from AVDD_ZCD power group. This supply must be decoupled down to 300kHz.

Reset and POR

- RESETn: The reset input for all digital circuits of the device.
- POR: This pin is used to generate a system reset signal during the power-up of the device. This signal has the following characteristics:
  - Open-drain output.
  - Monitors.
  - Core voltage supply.
  - Assertion lasts for 20ms typically after core voltage is over threshold.

To use the POR feature, the line must be pulled-up externally and connected to the RESETn pin.

Table 17: POR

Pin #	Pin Name	Type	Description
K14	POR	OD	**POR.**
L14	RESETn	I, PU, N	**System Reset.** The active-low, asynchronous system reset for the device. A reset pulse of at least 10ms is required. Configuration pins must have the correct voltage level at the end of the reset pulse.

The RESETn and POR pins are referred to the VDDO power group.

Reference Clock

The nominal reference clock to use has a frequency of 25MHz.

The 88LX5152 and 88LX5153 boots with the Xtal oscillator enabled (for example, the XTAL_OUT pin is active).

Table 18: Reference Clock

Pin #	Pin Name	Power Group	Type	Description
P6	XTAL_OUT	AVDD_PLL	A	**PLL Crystal Output.** Provides the output for the 25MHz system clock crystal. If an oscillator is used, this pin must be left unconnected.
R5	XTAL_IN	AVDD_PLL	A	**PLL Crystal Input.** Provides the input for the 25MHz system clock crystal. If an oscillator is used, it must be connected to this pin.
A11	**CLK_25MHZ**/GPIO_16	VDDO_GE	O	**25MHz output clock.** Commonly used by the external RGMII PHY. This pin can be used as GPIO if the output clock is not needed. The 25MHz clock is output on this pin at boot time and remains active until disabled by firmware, if required.

Note: When using CLK_25MHZ/GPIO_16 pin to drive the clock input of another device use a capacitor divider to adapt the voltage level.

Power and Ground

Table 19: Power and Ground

Pin #	Pin Name	Type	Typical Voltage	Description
N10, N11	AVDD_CONV	PWR	1.5V	**Analog supply for DAC and ADCs.**
N6	AVDD_ZCD	PWR	1.5V	**Analog supply ZCD.**
N8	XTAL_AVDD	PWR	1.5V	**Analog supply for Xtal and PLL.**
C8	SGMII_AVDD	PWR	1.5V	**Analog supply for SGMII.**
E8, E9, E11, E12, G7, H14, J7, J14, K7, K12, L7, H13, J13	VDD	PWR	1.1V	**Digital core power supply.**
L13, F13	VDDO	PWR	3.3V	**General digital I/O power supply.**
E13	VDDO_GE	PWR	2.5V 3.3V	**Digital I/O power supply for:** ■ RGMII/MII ■ CLK_25MHZ/GPIO_16 ■ GE_MDC/UART_CTS/GPIO_18 ■ GE_MDIO/UART_RTS/GPIO_17 **Digital I/O power supply for the same pins as GPIO.**
C12	VDDO_SPI2	PWR	3.3V	**Digital I/O power supply for SPI 2.**
D1, D2, D3, D4, D5, H1, H2, H3, H4, L1, L2, L3, L4	M_VDDQ	PWR	1.5V	**Power supply for DDR.**
B1, C1, C11, C2, C3, C4, C5, C6, C7, D11, D13, E10, F1, F10, F11, F12, F2, F3, F4, F8, F9, G1, G10, G11, G12, G2, G3, G4, G8, G9, H10, H11, H12, H7, H8, H9, J1, J10, J11, J12, J2, J3, J4, J8, J9, K1, K10, K11, K2, K3, K4, K8, K9, L10, L11, L12, L8, L9, M1, M2, M3, M4, N1, N12, N2, N3, N4, N5, N7, N9, P1, P2, P4, R4	VSS	GND	0V	**Ground.**

Others

Table 20: Others Pins

Pin #	Pin Name	Type	Description
P5	XTAL_ISET	A, IO	**Current Reference.** Connect to an external 6.04kΩ resistor with 1% accuracy. This pin generates internal reference currents.
A2	VREFCA_DQ_M	A, I	**DRAM Reference Voltage.** Set to M_VDDQ/2.
B2	ZQ	A, IO	Place a 240Ω 1% resistor between ZQ and VSS.
R2	M_CAL	A, IO	**Calibration Pad.** Place a 120Ω 1% resistor between M_CAL and VSS.
R6	ATP	DNC	Reserved pin, which must be left floating.
C9	DNC	DNC	Reserved pin, which must be left floating.
A8	RESERVED_1	DNC	Reserved pin, which must be left floating.
B8	RESERVED_2	DNC	Reserved pin, which must be left floating.
A7	RESERVED_3	DNC	Reserved pin, which must be left floating.
B7	RESERVED_4	DNC	Reserved pin, which must be left floating.
A6	RESERVED_5	DNC	Reserved pin, which must be left floating.
B6	RESERVED_6	DNC	Reserved pin, which must be left floating.
A3	RESERVED_7	DNC	Reserved pin, which must be left floating.
B3	RESERVED_8	DNC	Reserved pin, which must be left floating.
G13	RESERVED_9	DNC	Reserved pin, which must be left floating.
C10	RESERVED_10	DNC	Reserved pin, which must be left floating.

Electrical Specifications

Absolute Maximum Ratings

Important! The stresses above what is listed under the following table may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under the following table or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above the recommended extended periods of time may affect device reliability. Solder reflow profile is specified in the IPC/JEDEC J-STD-020C standard.

Table 21: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Digital I/O Power Supply	–0.4	3.63	V
Digital Core Power Supply	–0.4	1.32	V
Analog SGMII Power Supply	–0.4	1.8	V
Analog PLL and Xtal Power Supply	–0.4	1.8	V
Analog Converters Power Supply	–0.4	1.8	V
Analog ZCD Power Supply	–0.4	1.98	V
Storage Temperature	–40	150	°C

Required Operating Conditions

Table 22: Required Operating Conditions

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
VDDO	Digital I/O Power Supply	VDDO at 3.3V VDDO at 2.5V	3.135 2.375	3.3 2.5	3.465 2.635	V V
VDD	Digital Core Power Supply	-	1.067	1.1	1.133	V
XTAL_AVDD	Analog PLL and Crystal Power Supply	-	1.455	1.5	1.545	V
SGMII_AVDD	Analog SGMII Power Supply	-	1.455	1.5	1.545	V
AVDD_CONV	Analog Converters Power Supply	-	1.455	1.5	1.545	V
M_VDDQ	Analog DDR Power Supply	-	1.455	1.5	1.545	V
AVDD_ZCD	Analog ZCD Power supply	-	1.455	1.5	1.545	V
T_A	Ambient Operating Temperature Commercial Grade Industrial Grade	 - -	 0 –40	 - -	 70 85	 °C °C
T_J	Maximum Junction Temperature	-	-	-	125	°C

DC Electrical Characteristics

Table 23: Power Consumption

Ping	Condition	Minimum	Typical	Maximum	Unit
VDD (1.1V)	-	-	1000	1800	mW
XTAL_AVDD, SGMII_AVDD, AVDD_CONV, AVDD_ZCD, M_VDDQ (1.5V)	-	-	375	500	mW
VDDO (3.3V)	Does not include VDDO_GE	-	20	40	mW
VDDO_GE (2.5V)	-	-	60	80	mW

Note:

- Actual power consumption depends on several factors, such as
  - Traffic bursts.
  - Actual driving settings for the I/Os.
  - Capacitance on the I/Os.
  - Transmission modes.
- VDDO power consumption does not include low impedance loads, such as LEDs.

Digital Pins Operating Conditions

Table 24: Digital Pins Operating Conditions

Symbol	Parameter	Pins	Condition	Minimum	Maximum	Unit
V_{IH}	High Level Input Voltage	XTAL_IN	-	0.8	-	V
		All Others (Single-ended)	-	VDDO × 0.7	VDDO + 0.4	V
V_{IL}	Low Level Input Voltage	XTAL_IN	-	-	0.2	V
		All Others (Single-ended)	-	–0.4	VDDO × 0.3	V
I_{OH}	High Level Output Current	RGMII Inputs[1]	VDDO_GE=2.5V	4	-	mA
		All Others	VDDO = 3.3V	7	-	mA
I_{OL}	Low Level Output Current	RGMII Inputs	0.2V	4	-	mA
		All Others	0.2V	10	-	mA
I_{LK}	Input Leakage Current	All	VDDO is ON, 0 < V(PAD) < VDDO	-	2	µA
PU	Pull-up Resistance	All (with Pull-up)	-	30	150	kΩ
PD	Pull-down Resistance	All (with Pull-down)	-	30	150	kΩ
C_{IN}	Input Capacitance	XTAL_IN	-	-	8	pF
		All Others	-	-	5	pF

1. RGMII Inputs:
   - GE_RXD_3/GPIO_25
   - GE_RXD_2/GPIO_26
   - GE_RX_CLK/GPIO_27
   - GE_RXD_1/GPIO_28
   - GE_RXD_0/GPIO_29
   - GE_RX_CTRL/GPIO_30

Thermal Resistance Characteristics

Table 25: Thermal Resistance Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
θ_{JC} [1, 2]	Junction-to-case Thermal Resistance	-	10.4	-	°C/W
θ_{JA} [2]	Junction-to-ambient Thermal Resistance	-	37.1	-	°C/W

1. Thermal resistance between the junction and package case surface assumes that all heat from the junction is taken out from the case surface.

2. Values obtained from simulations based on the *JEDEC 2s2p PCB*.

System Clock Specifications

The system clock is obtained using an oscillator with an external quartz crystal. The crystal network must be adjusted to produce the nominal frequency at 25°C and comply with the drive level specified by the manufacturer.

Table 26: System Clock Specifications

Parameter	Minimum	Typical	Maximum	Unit
Frequency	-	25	-	MHz
Tolerance	-	-	± 25	ppm

ESD Performance

Pins meet the ESD levels listed in the following table.

Table 27: ESD Levels

Parameter	Description	Level Passed
JESD22-A114-F	HBM	2 KV
JESD22-C101E	CDM	800V

AC Electrical Specifications

Reset

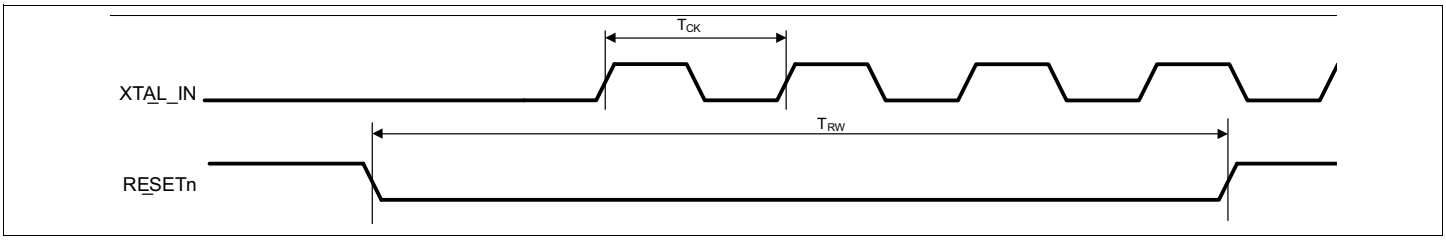

Figure 21: Reset Timing Specification

Table 28: Reset Requirements

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{CK}	Clock Period.	-	40	-	ns
T_{RW}	Reset pulse width.	4	-	-	Clock cycles
T_{RW}	Reset pulse width.	-	20[1]	-	ms

1. To ensure a correct voltage level of configuration pins at the end of reset, a pulse of typically 10ms is required.

SPI Timings

SPI Features

- Master only operation.
- The AFE must always be connected to SPI1 through SPI1_CS_N.
- Similarly, SPI2 must always be connected to a SPI flash memory using SPI2_CS_N.

AC Electrical Characteristics

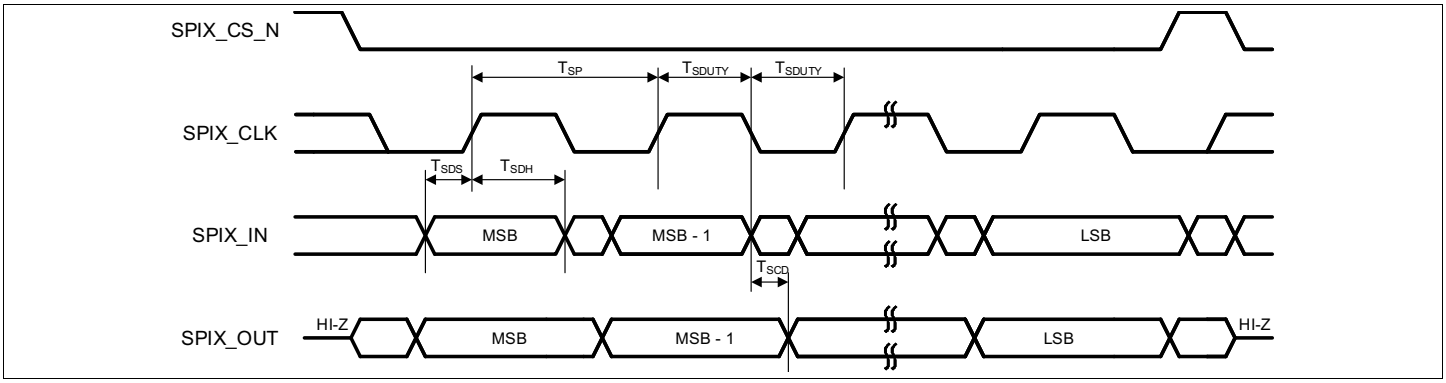

Figure 22: SPI Timing Characteristics

Note: The X represents either SPI1 or SPI2. The diagram shown in Figure 22 is drawn for CPHA=0 CPOL=0 and CPHA=1 CPOL=1.

Table 29: SPI1 Timing Characteristics

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{SP}	SPI1 clock period.	10[1] 30[2]	-	-	ns
T_{SDUTY}	SPI1 clock duty cycle.	40	-	-	%
T_{SDS}	SPI1 data setup time.	7	-	-	ns
T_{SDH}	SPI1 data hold time.	0	-	-	ns
T_{SCD}	SPI1 clock to data time.	0	-	3	ns

1. For write operations; Read operations should be ignored.

2. For read operations.

Note: All output delays are defined with a 5pF load.

Table 30: SPI2 Timing Characteristics

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{SP}	SPI2 clock period.	20	-	-	ns
T_{SDUTY}	SPI2 clock duty cycle.	40	-	-	%
T_{SDS}	SPI2 data setup time.	5	-	-	ns
T_{SDH}	SPI2 data hold time.	0	-	-	ns
T_{SCD}	SPI2 clock to data time.	0	-	5	ns

Note: All output delays are defined with a 6pF load.

UART Interface Timings

The basic UART interface consists of two pins and with the capability of an extended UART by using two more control pins (CTS and RTS).

When the device is:

- Transmitting to an external device: UART characters are transmitted serially using the UART_TX wire.
- Receiving data from an external device: UART characters are received serially using the UART_RX wire.

Both UART_TX and UART_RX are asynchronous.

- The UART_RTS requests the device to be prepared to receive data.
- The UART_CTS indicates that device is ready to accept data.

The following figure shows the UART frame transmission and reception format. The UART transmits and receives each data character in a standard format consisting of a single start bit, 8-bits of data, and a single stop bit.

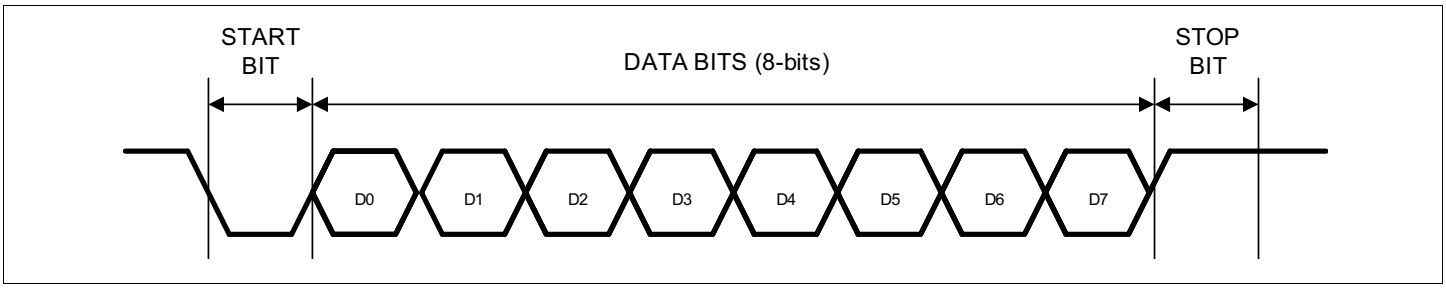

Figure 23: UART Interface

SMI Timings

SMI Master Mode Timings

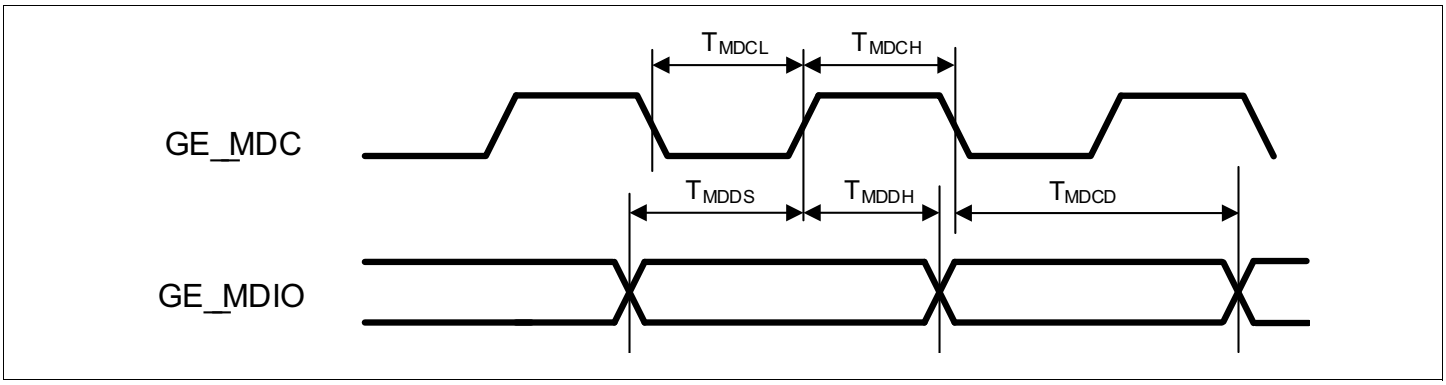

Figure 24: SMI Master Mode Timing Characteristics

Table 31: SMI as Master Timing Characteristics

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{MDCD}	GE_MDIO clock to data timing.	0	-	10	ns
T_{MDDS}	GE_MDIO data setup timing.	10	-	-	ns
T_{MDDH}	GE_MDIO data hold timing.	0	-	-	ns
T_{MDCH}	GE_MDC clock high time.	40	-	-	ns
T_{MDCL}	GE_MDC clock low time.	40	-	-	ns

Note: All output delays are defined with a 5pF load.

SMI Slave Mode Timing

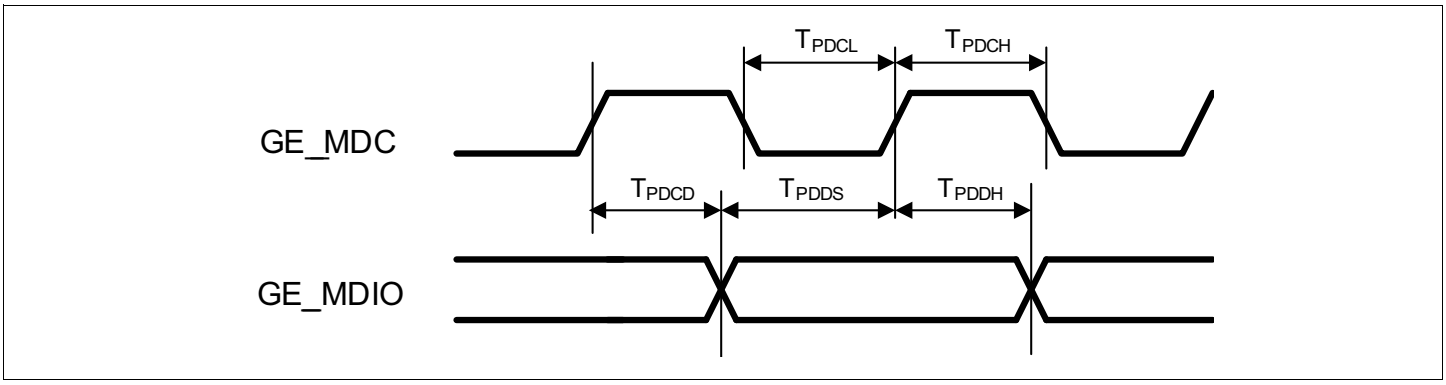

Figure 25: SMI Slave Mode Timing Characteristics

Table 32: SMI as Slave Mode Timing Characteristics

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{PDCD}	GE_MDIO clock to data timing.	0	-	10	ns
T_{PDDS}	GE_MDIO data setup timing.	10	-	-	ns
T_{PDDH}	GE_MDIO data hold timing.	10	-	-	ns
T_{PDCH}	GE_MDC clock high time.	40	-	-	ns
T_{PDCL}	GE_MDC clock low time.	40	-	-	ns

Note: All output delays are defined with a 5pF load.

MII Timings

MII MAC Mode Timings

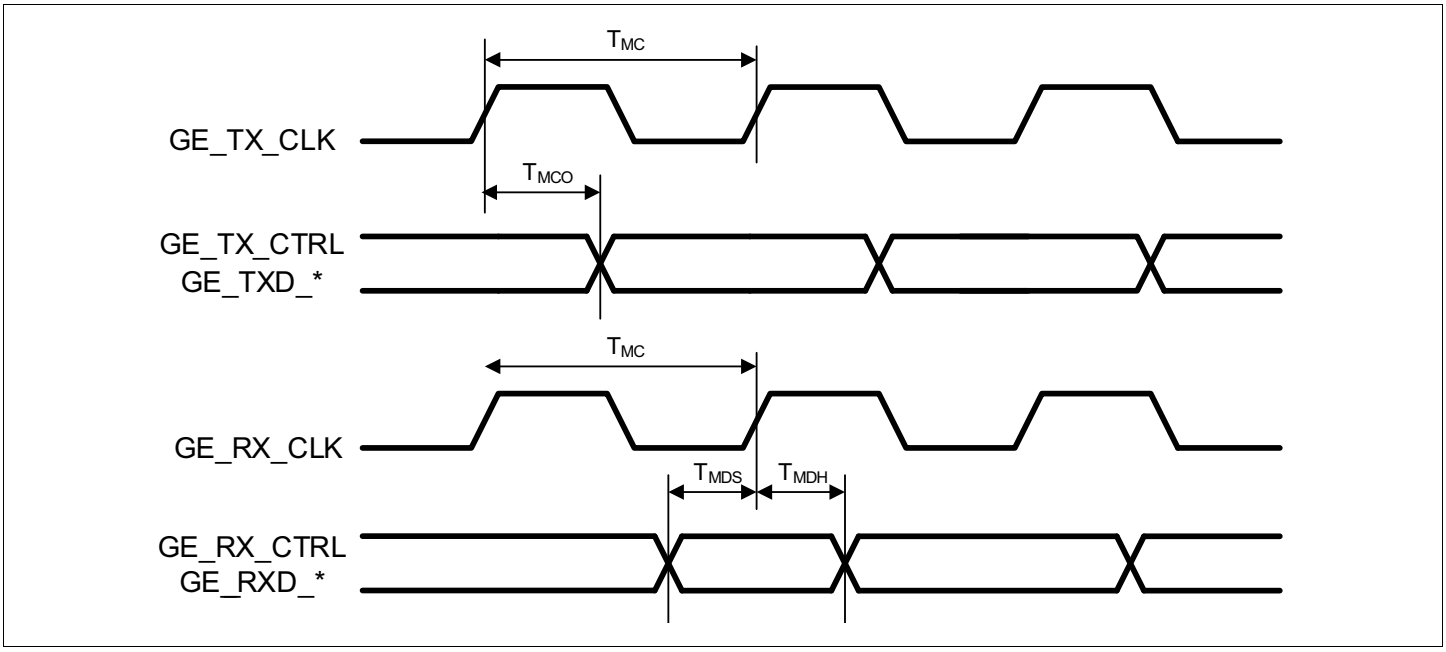

Figure 26: MII MAC Timing Characteristic

Table 33: MII as MAC Timing Characteristics

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{MC}	MII clock.	-	40	-	ns
Duty 10/100	MII duty-cycle.	35	-	65	%
T_{MCO}	MII clock to output timing.	0	-	25	ns
T_{MDS}	MII data setup timing.	10	-	-	ns
T_{MDH}	MII data hold timing.	10	-	-	ns

Note: All output delays are defined with a 5pF load.

MII PHY Mode Timings

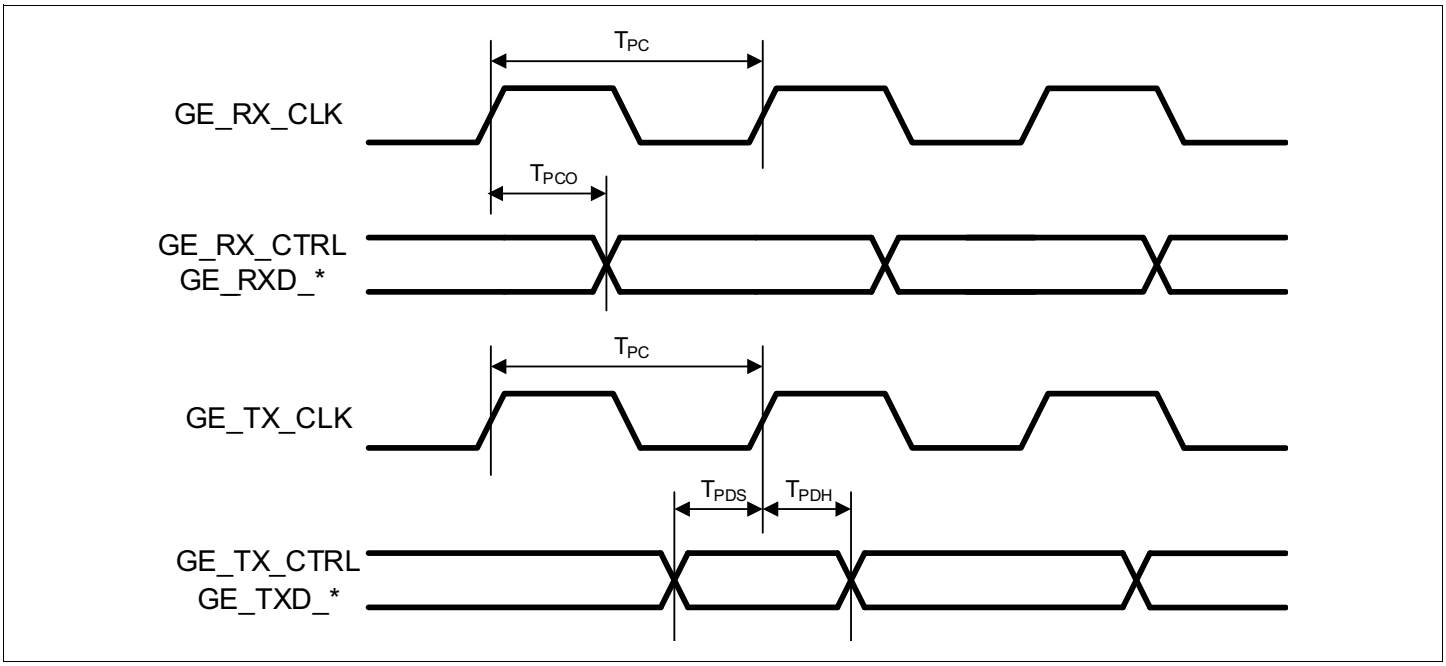

Figure 27: MII PHY Timing Characteristic

Table 34: MII as PHY Timing Characteristics

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{PC}	MII clock.	-	40	-	ns
Duty 10/100	MII duty cycle.	35	-	65	%
T_{PCO}	MII clock to output timing.	15	-	26	ns
T_{PDS}	MII data setup timing.	10	-	-	ns
T_{PDH}	MII data hold timing.	–0.5	-	-	ns

Note: All output delays are defined with a 10pF load.

RGMII Timings

The RGMII uses a 125MHz clock with a 4-bit wide data path. Besides the 4-bit wide data path, the GE_TX_CTL and GE_RX_CTL lines are used to carry control information such as TX_EN, TX_ER, RX_DV, and RX_ER.

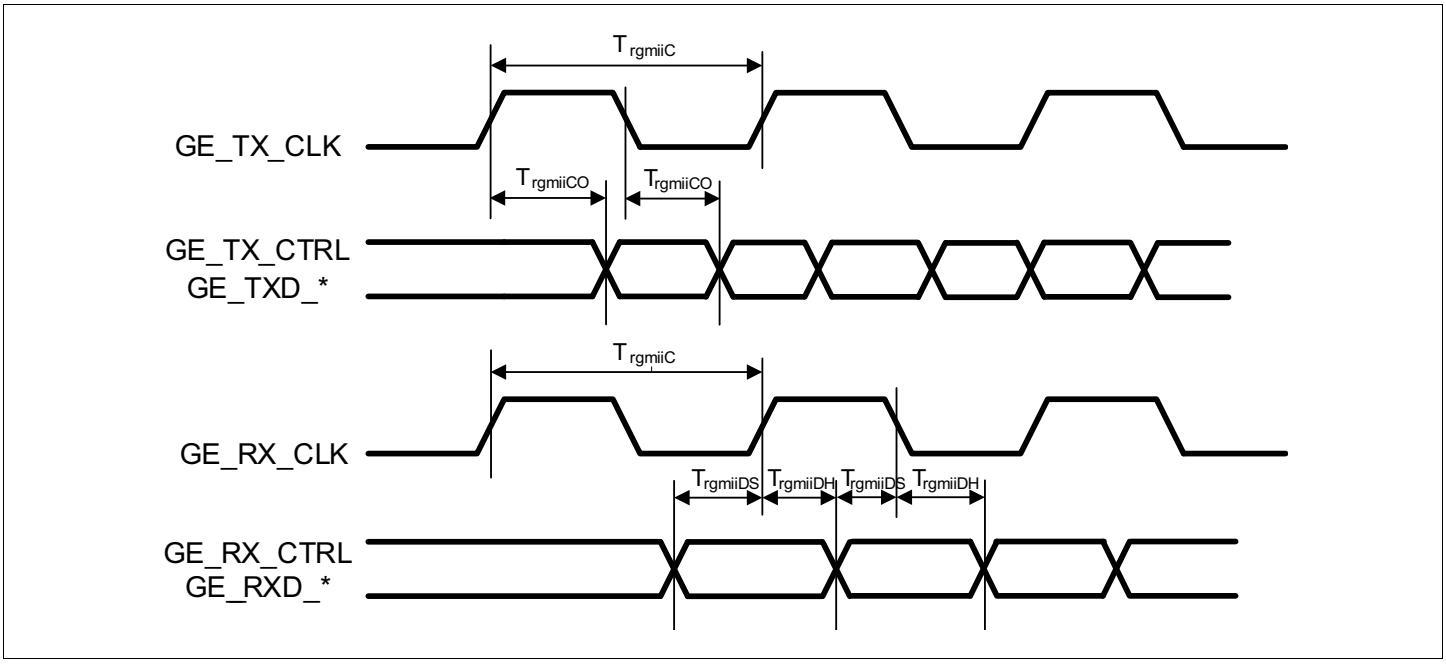

Figure 28: RGMII 1000Mbps Timing Characteristics

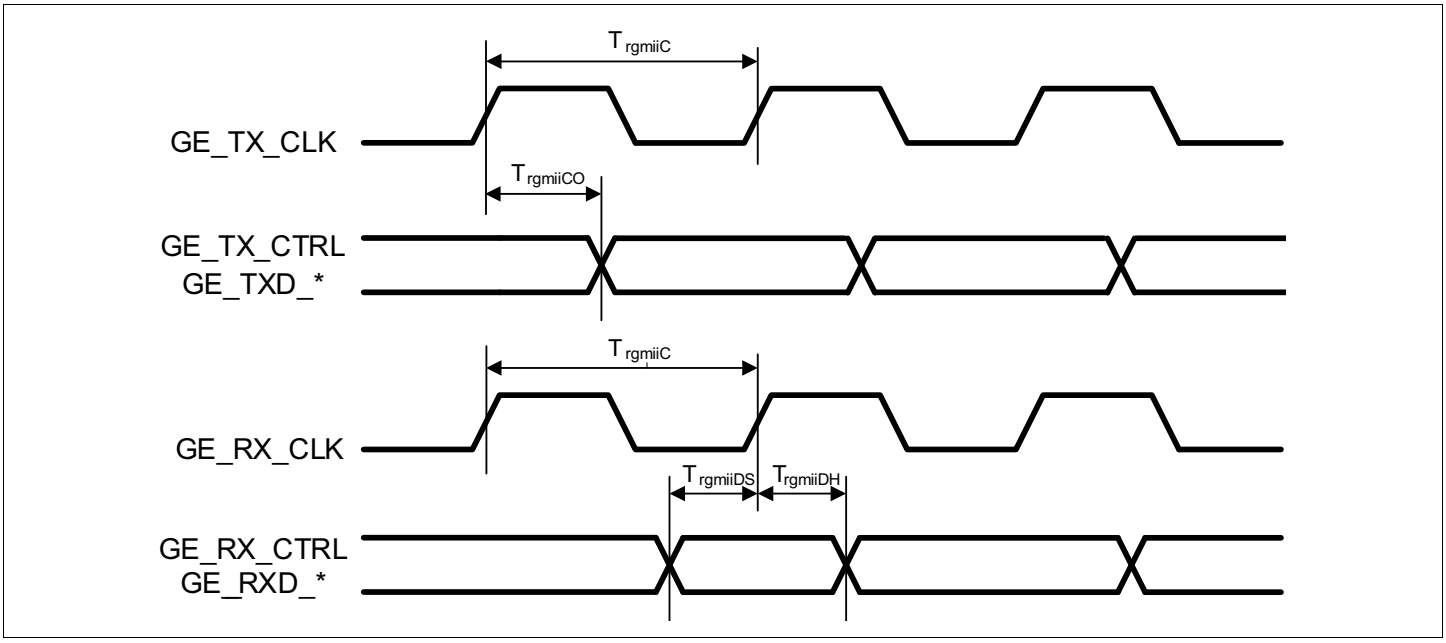

Figure 29: RGMII 10/100Mbps Timing Characteristics

Table 35: RGMII (No Delay Mode, both in Tx and Rx) Timing Characteristics

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{rgmiiC}	RGMII clock cycle duration.	-	7.2	-	-
Duty G	RGMII 1000 duty cycle.	-	45	50	55
Duty T	RGMII 10/100 duty cycle.	-	40	50	60
$T_{rgmiiCO}$	GE_TX_CLK clock to data/CTL timing.	-	–0.5	-	0.5
$T_{rgmiiDS}$	GE_RX data/CTL setup timing.	-	1	-	-
$T_{rgmiiDH}$	GE_RX data/CTL hold timing.	-	0.8	-	-

Note: All output delays are defined with a 5pF load.

Table 36: RGMII (Delay Mode, both in Tx and Rx) Timing Characteristics

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{rgmiiC}	RGMII clock cycle duration.	7.2	8	8.8	ns
Duty G	RGMII 1000 duty cycle.	45	50	55	%
$T_{rgmiiCO}$	GE_TX_CLK clock to data/CTL timing.	–2.6	-	–1.2	ns
$T_{rgmiiDS}$	GE_RX data/CTL setup timing.	–1	-	-	ns
$T_{rgmiiDH}$	GE_RX data/CTL hold timing.	2.6	-	-	ns

Note: All output delays are defined with a 5pF load.

SGMII Specifications

The 88LX5152 and 88LX5153 incorporates a 1Gbps/2.5Gbps SerDes interface. By default, the SerDes is used in SGMII mode.

Table 37: SerDes Specification

Parameter	Condition	Minimum	Typical	Maximum	Unit
SerDes Baud Rate	1G 2.5G	-	1.25 3.125	-	GBd
TXP Differential Output Voltage	1G 2.5G	0.3 0.8	-	0.8 1.2	V_{pp}
TXP Total Jitter[1]	1G/2.5G	-	-	0.35	UI
TXP Differential Impedance	-	-	100	-	Ω
TXP Differential Mode Return Loss	100MHz–2500MHz	8	-	-	dB
TXP Common Mode Return Loss	100MHz–2500MHz	11	-	-	dB
RXP Differential Input Voltage	-	0.2	-	-	V_{pp}
RXP Total Jitter Tolerance[1]	1G	-	-	0.65	UI
RXP 2.5GBase-KX Jitter Tolerance[1,2]	Applied sinusoidal jitter Applied random jitter Applied duty cycle distortion Broadband noise	- - - -	- - - -	0.12 0.2 0.035 10.2	UI_{pp} UI_{pp} UI_{pp} mV
RXP Differential Impedance	-	-	100	-	Ω
RXP Differential Mode Return Loss	100MHz–2500MHz	9.8	-	-	dB
RXP Common Mode Return Loss	100MHz–2500MHz	14.6	-	-	dB

1. Measured at BER: 1E-12.

2. PRBS31 test pattern used.

Note: The external AC-coupling capacitor is required.

JTAG Interface AC Timing

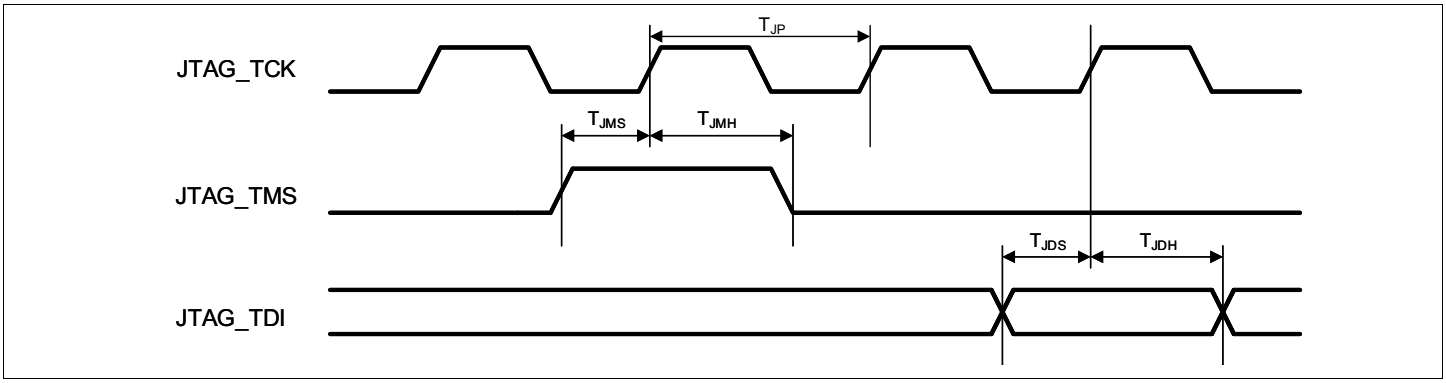

Figure 30: JTAG Input Timing Characteristics

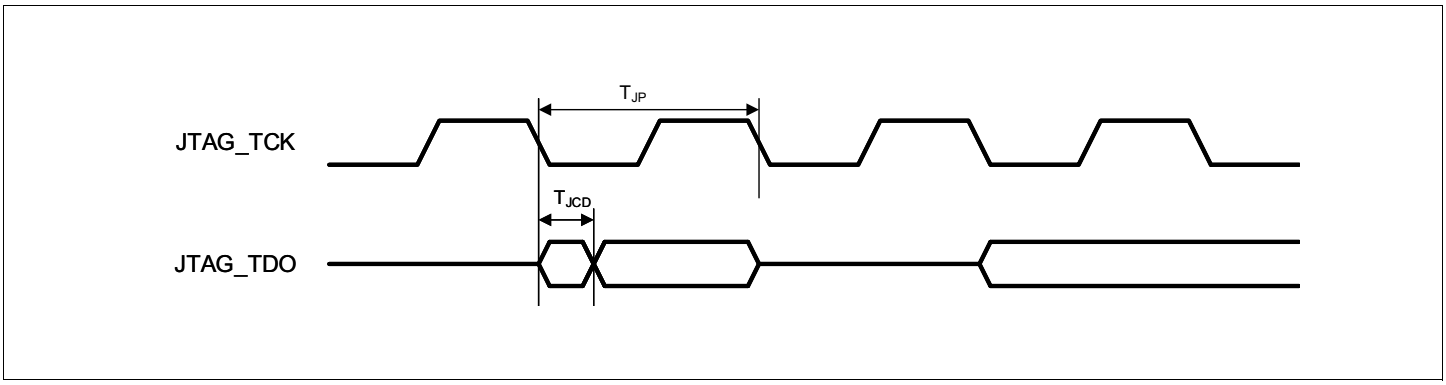

Figure 31: JTAG Output Timing Characteristics

Table 38: JTAG Timing Characteristics

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{JP}	JTAG TCK period.	40	-	-	ns
T_{JMS}	JTAG TMS setup timing.	25	-	-	ns
T_{JMH}	JTAG TMS hold timing.	2	-	-	ns
T_{JDS}	JTAG data setup timing.	25	-	-	ns
T_{JDH}	JTAG data hold timing.	2	-	-	ns
T_{JCD}	JTAG clock to data timing.	0	-	15	ns

Note: All output delays are defined with a 4pF load.

Mechanical Drawings

186-Pin TFBGA Package

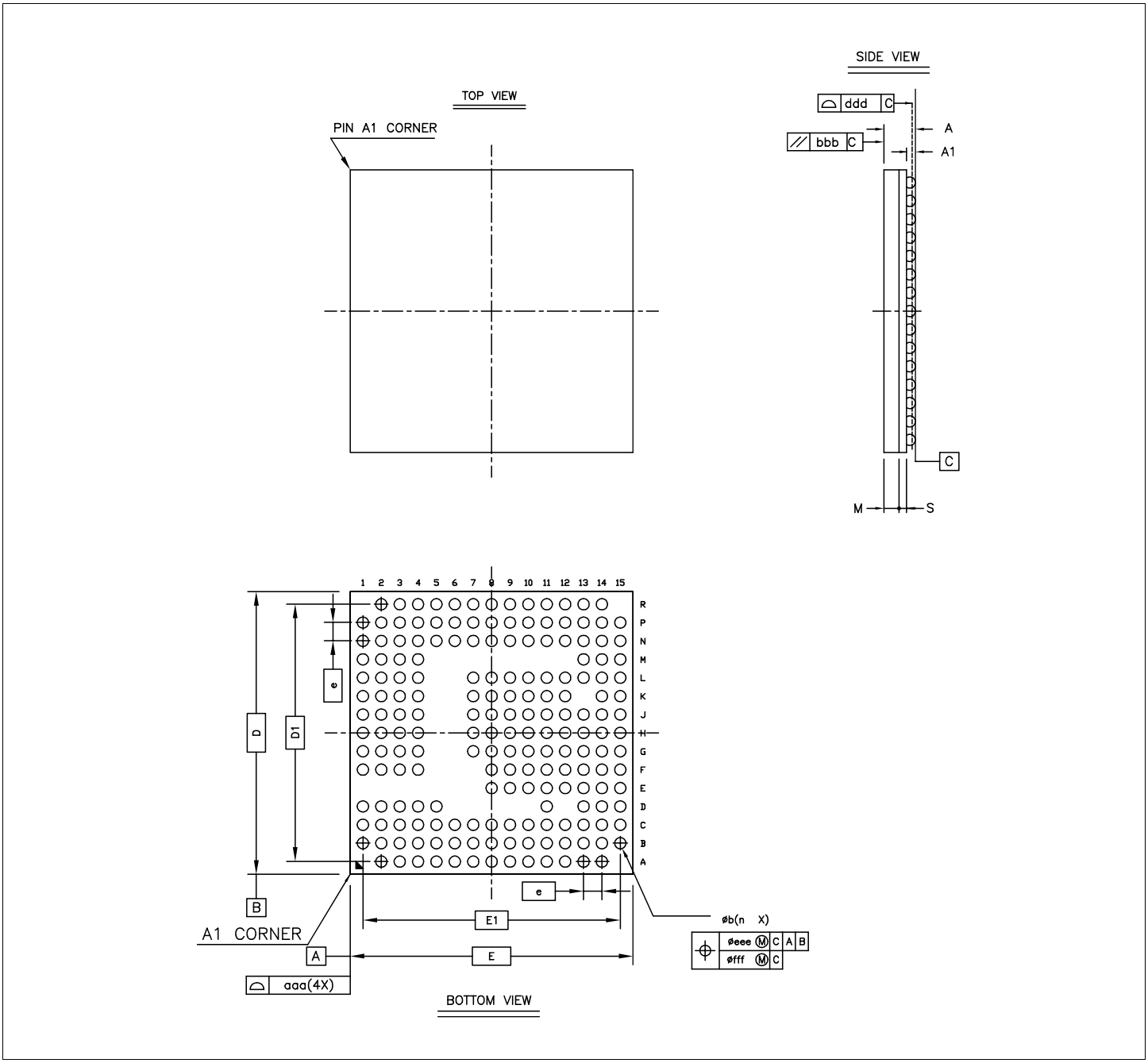

Figure 32: 186-Pin TFBGA Package 10mm × 10mm Mechanical Drawing

Table 39: Package Dimensions

Item		Symbol	Minimum	Nominal	Maximum	Unit
Body Size	X	E	-	10.000	-	mm
	Y	D	-	10.000	-	mm
Ball Pitch		e	-	0.650	-	mm
Total Thickness		A	1.040	1.110	1.180	mm
Mold Thickness		M	-	0.530 Ref.	-	mm
Substrate Thickness		S	-	0.260 Ref.	-	mm
Ball Diameter		-	-	0.400	-	mm
Stand-off		A1	0.270	-	0.370	mm
Ball Width		b	0.380	-	0.380	mm
Package Edge Tolerance		aaa	-	0.150	-	mm
Mold Parallelism		bbb	-	0.200	-	mm
Co-planarity		ddd	-	0.120	-	mm
Ball Offset (Package)		eee	-	0.150	-	mm
Ball Offset (Ball)		fff	-	0.080	-	mm
Ball Count		n	-	186	-	-
Edge Ball Center to Center	X	E1	-	9.100	-	mm
	Y	D1	-	9.100	-	mm

Ordering Information

Part Order Numbering

The following figures show the part order numbering scheme for the 88LX5152 and 88LX5153. For more information, contact MaxLinear's Customer Technical Support.

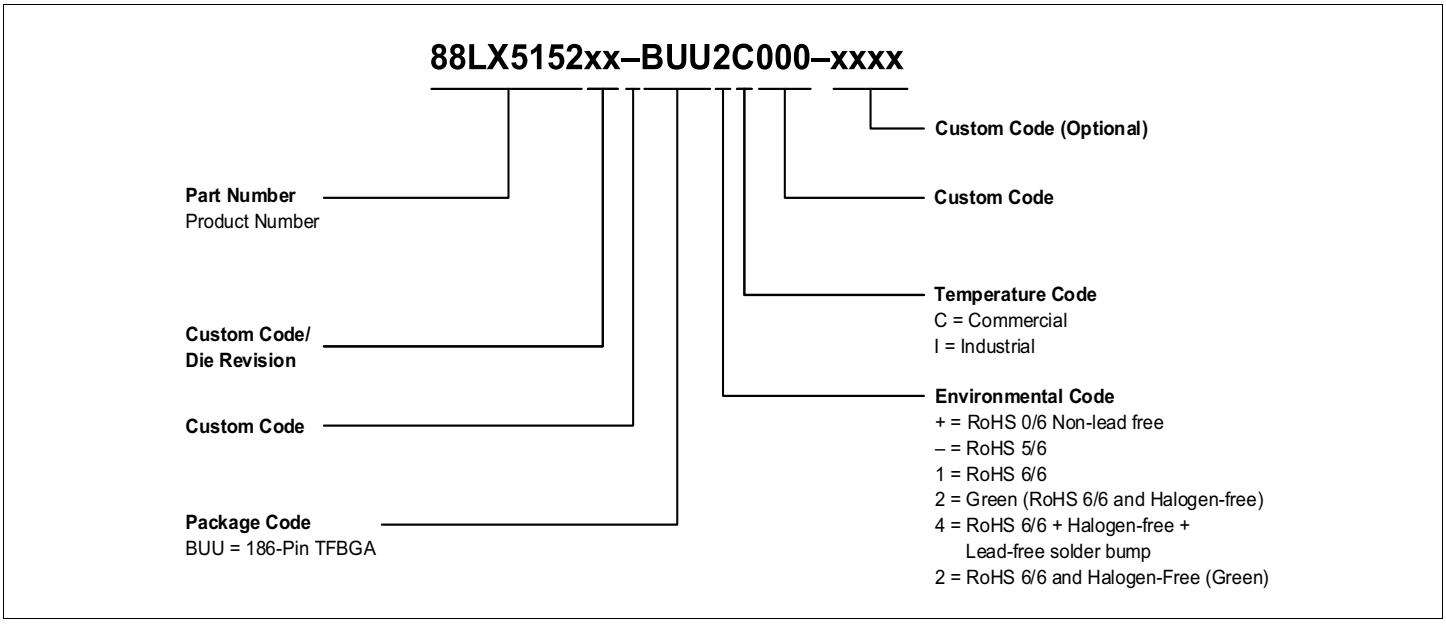

Figure 33: 88LX5152 Sample Part Number

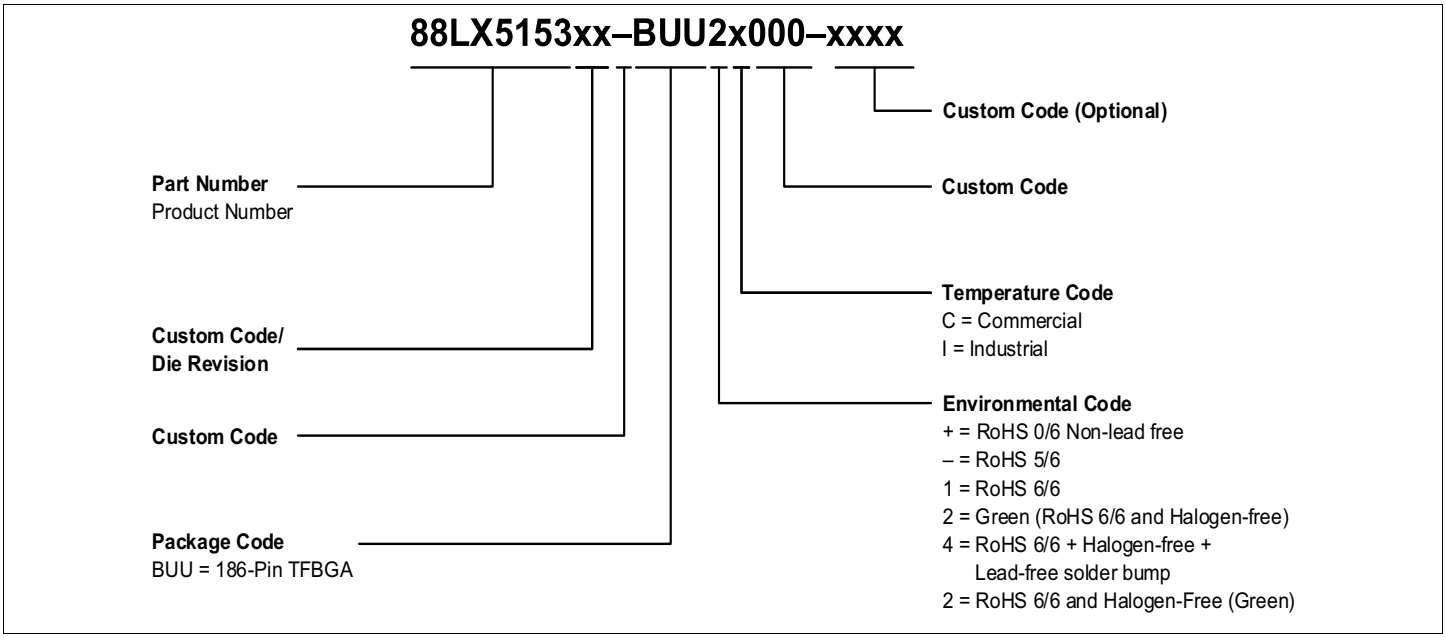

Figure 34: 88LX5153 Sample Part Number

Part Order Options

Table 40: 88LX5152 and 88LX5153 Part Order Options

Package Type	Part Order Number	Description
186-pin TFBGA	88LX5152A0-BUU2C000	G.hn Wave-2 BB—powerline MIMO.
186-pin TFBGA	88LX5153A0-BUU2C000	G.hn Wave-2 BB—coaxial/phone line/powerline MIMO.
186-pin TFBGA	88LX5153A0-BUU2I000	G.hn Wave-2 BB—coaxial/phone line/powerline MIMO (Industrial temperature).

Package Marking

The following figure shows a sample package marking and pin 1 location for the 88LX5152 and 88LX5153 devices.

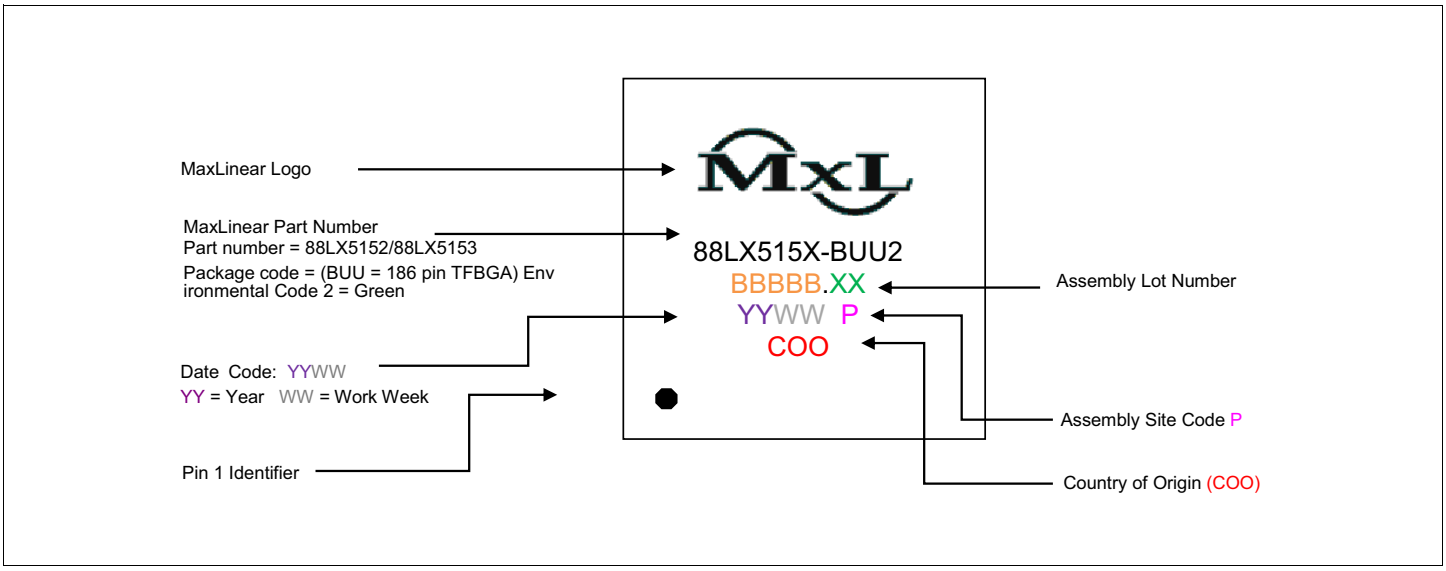

Figure 35: 88LX5152 and 88LX5153 Package Marking and Pin 1 Location

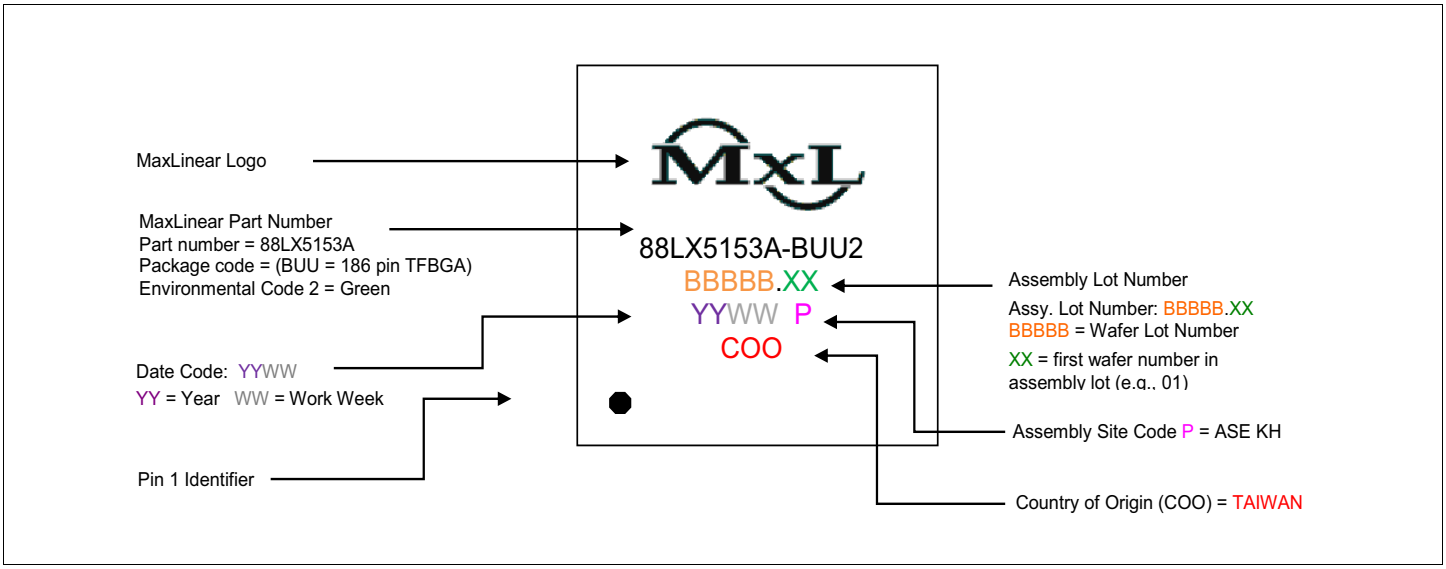

Figure 36: 88LX5153A Package Marking and Pin 1 Location

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