

General Description

The **XR46701** is a current controller which integrates a PWM dimming function which can be controlled by a 1V to 4V control signal. Current is regulated through an external N-channel power MOSFET which allows one to scale current and spread heat dissipation.

The XR46701 is generally configured to be the last step in an LED AC direct step drive solution which provides excellent Power Factor and THD without the need for bulk capacitance or inductors. The DC dimming control signal applied to the DIM pin is converted to a Pulse Width Modulation signal to adjust the LED brightness.

The XR46701 also includes thermal foldback and power line regulation to avoid excessive power loss and over heating which can significantly reduce the life of LEDs. The Over Voltage Protection (OVP) and Over Temperature Protection (OTP) provide a failsafe in the worst operating conditions. The OVP can also be used to enable unique dual range AC direct drive solutions.

FEATURES

- 4V to 40V supply voltage range
- Power line regulation
- 1V to 4V DC to PWM dimming control range
- 400 to 2000 Hz adjustable internal PWM oscillator
- V_{IN} supply clamp eliminates external zener
- Dual Mode over temperature protection
 - Thermal current foldback
 - Thermal shutdown
- Over voltage protection enables dual range lighting solutions
- >600V Native Surge protection extends MOV life
- 5V 1mA output

APPLICATIONS

- AC direct drive LED lighting
- High bay lighting
- Dual range light engines
- Downlights
- Smart lighting

Typical Application

Ordering Information - [Back Page](#)

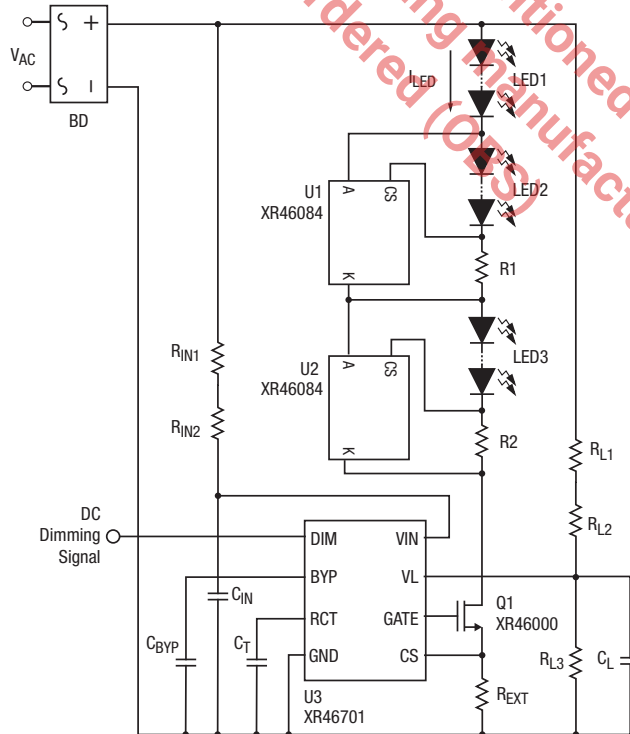


Figure 1: Typical Application

Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition may affect device reliability and lifetime.

Sustaining voltage

V_{IN} pin.....-0.3V to 45V

Other pins.....-0.3V to 7V

Storage temperature range -55°C to 150°C

Lead temperature (soldering, 10 seconds)..... 260°C

NOTES:

1. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
2. All parameters having Min/Max specifications are guaranteed. Typical values are for reference purpose only.
3. Unless otherwise noted, all tests are pulsed tests at the specified temperature, therefore: $T_J = T_C = T_A$.

Operating Conditions

Input voltage, V_{IN}4V to 42V

DC dimming signal, V_{DIM}0V to 5V

VL line regulation control signal, V_{VL}0V to 5V

Internal PWM dimming frequency, f_{RCT} 1200Hz, typical

Operating junction temperature, T_J -40°C to 125°C

Maximum operating junction temperature, T_J 150°C

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Electrical Characteristics

Specifications are for Operating Junction Temperature of $T_J = 25^\circ\text{C}$ only; limits applying over the full Operating Junction Temperature range are denoted by a “•”. Typical values represent the most likely parametric norm at $T_J = 25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise noted, values are at $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
I_{IN}	V_{IN} supply current	$V_{IN} = 5.5\text{V}$ to 36V , DIM = 0V and 5V	0.3	0.6	1.0	mA	
$V_{IN,CLAMP}$	V_{IN} over voltage clamp	When $V_{IN} > V_{IN,CLAMP}$, I_{IN} will increase to $>1\text{mA}$ to clamp V_{IN} at $V_{IN,CLAMP}$.	36	40	42	V	
V_{BYP}	BYP voltage	$6\text{V} \leq V_{IN} \leq 40\text{V}$, $I_{BYP} = 0$ to 2mA	4.6	5.1	5.6	V	
I_{BYP}	BYP pin output current		1			mA	
V_{CS}	CS pin voltage	$V_{IN} = 15\text{V}$, $V_{VL} = 2.7\text{V}$		0.264	0.270	0.276	V
			•	0.260		0.285	
ΔV_{LR}	CS voltage line regulation vs. $V_{IN}^{(1)}$	$V_{IN} = 15\text{V}$, $V_{VL} = 2.7\text{V}$ to 3.3V		-18	-20	-22	%
				-0.08	-0.09	-0.10	mV/mV
$V_{L,OVP}$	VL over voltage protection	V_{VL} increasing		3.40		V	
$V_{L,OVPR}$	VL over voltage protection recovery to normal ⁽²⁾	V_{VL} falling	2.95	3.06	3.15	V	
$V_{CS,OVP}$	VL over voltage protection mode V_{CS}	$V_{VL} > V_{L,OVP}$		0		%	
$V_{L,UVP}$	VL under voltage protection			2.2		V	
$V_{CS,UVP}$	VL Under voltage protection mode V_{CS}	$V_{VL} = 2.0\text{V}$		112		%	
				302		mV	
I_{SOURCE}	GATE source current	$V_{GATE} - V_{CS} = 3\text{V}$		5		mA	
I_{SINK}	GATE sink current	$V_{GATE} - V_{CS} = 3\text{V}$		5		mA	
i_{DOWN}	Internal pull-high current	DIM pins		1		uA	
V_{IH}	DIM pin DC dimming voltage level	"H" level	PWM duty = 100%	4	V_{BYP}	V	
V_{IL}		"L" level	PWM duty = 2% (minimum duty)	0.5	1		
V_{OFF}		Off	PWM duty = 0% (shutdown).	0	0.5		
V_{HYS}		Hysteresis			44		mV
D_{MIN}	PWM dimming minimum duty	$V_{DIM} = 0.5$ to 1V , $f_{RCT} = 1\text{kHz}$		2		%	
f_{RCT}	Internal PWM dimming frequency	RCT pin, $C_{RCT} = 2.2\text{nF}$		1.0		kHz	
i_{CHARGE}	RCT charge current	Source by RCT pin		300		uA	
$i_{DISCHARGE}$	RCT discharge current	Sink by RCT pin		8		uA	

Electrical Characteristics

Specifications are for Operating Junction Temperature of $T_J = 25^\circ\text{C}$ only; limits applying over the full Operating Junction Temperature range are denoted by a “•”. Typical values represent the most likely parametric norm at $T_J = 25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise noted, values are at $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{TP1}	Primary thermal protection trip temperature ^{(3),(4)}	When T_J is higher than T_{TP1} , V_{CS} decreases linearly at the slope of $-1\%/^\circ\text{C}$.	120	135		$^\circ\text{C}$
T_{TP2}	Secondary thermal protection trip temperature ^{(3),(5)}	When T_J is higher than T_{TP2} , V_{CS} decreases to $V_{CS,TP2}$ directly. ($T_{TP2} - T_{TP1} = 25^\circ\text{C}$)		150		$^\circ\text{C}$
$V_{CS,TP2}/V_{CS}$	Secondary thermal protection mode V_{CS} voltage	$T_J > T_{TP2}$		20		%
$T_{SD,HYS}$	Secondary thermal protection hysteresis ⁽³⁾			40		$^\circ\text{C}$

NOTES:

1. The CS voltage line regulation is defined as:

$$\Delta V_{LR} = \frac{\Delta V_{CS}}{\Delta V_{VL}} = \frac{V_{CS}(V_{VL} = 3.3V) - V_{CS}(V_{VL} = 2.7V)}{3.3V - 2.7V}$$

2. VL Under Voltage Protection Mode V_{CS} :

$$\% = \frac{V_{CS}(V_{VL} = 2.0V)}{V_{CS}(V_{VL} = 2.7V)}$$

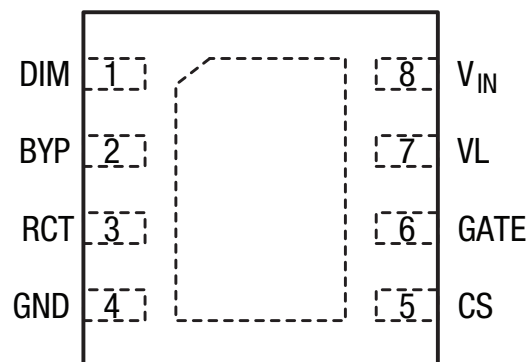
3. Guarantee by design, not by production test.

4. When $T_J > T_{TP1}$, the V_{CS} voltage decreases linearly at the slope of $-1\%/^\circ\text{C}$.

5. When $T_J > T_{TP2}$, the V_{CS} voltage drops to 20%.

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Pin Configuration



DFN-8 3mm x 3mm, Top View



MSOP-8, Top View

Pin Functions

Pin Number	Pin Name	Description
1	DIM	PWM Dimming Control Input pin. A DC control signal from 1V to 4V sets the PWM duty cycle where the frequency is set by RCT pin. An input to the DIM pin higher than 4V results in 100% duty cycle. When the DIM pin is between 0.5V and 1V, the duty is fixed at the minimum of 2%. When the DIM pin is lower than 0.5V, the duty cycle is 0% (off)
2	BYP	Bypass pin of the internal regulator. Connect a de-coupling capacitor to ground.
3	RCT	PWM dimming frequency set pin. Connecting a 2.2nF capacitor between the RCT pin and GND will result in approximately 1.2kHz operation.
4	GND	Ground pin.
5	CS	Current Sense pin. Connect a sense resistor, R_{EXT} , between this pin and the GND pin. The current is set by: $I_{OUT} = \frac{V_{CS}}{R_{EXT}}$
6	GATE	External MOSFET gate drive pin.
7	VL	VAC power line regulation compensation control pin. The VL voltage level is used to control the VCS voltage to provide power line regulation compensation and trigger the over voltage protection circuit.
8	VIN	Power supply pin. This pin is clamped with an internal 40V clamp.

Functional Block Diagram

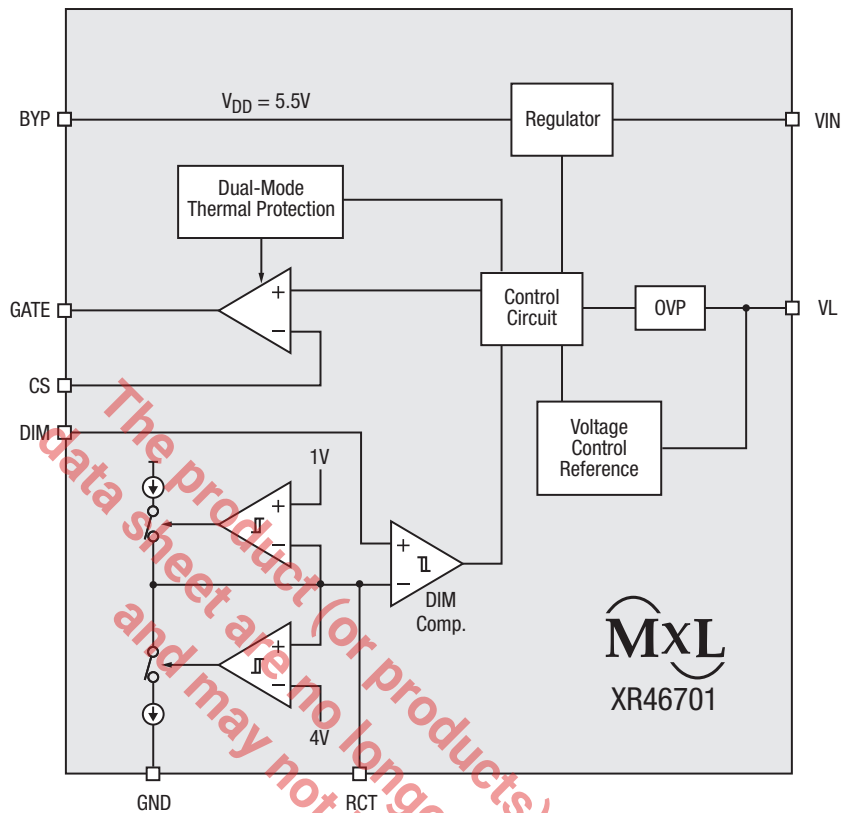


Figure 2: Functional Block Diagram

Applications Information

Dual-Mode Thermal Protection

When the junction temperature T_J reaches T_{TP1} , the V_{CS} voltage starts to decrease linearly at the slope of $-1\%/^{\circ}\text{C}$. The LED driving current decreases accordingly. The system can still work normally under the thermal protection mode with lower driving current. The power dissipation on the XR46701 chip becomes lower so the T_J will stop increasing when thermal balance is reached. If T_J keeps increasing to reach T_{TP2} , the V_{CS} voltage drops to 20% directly.

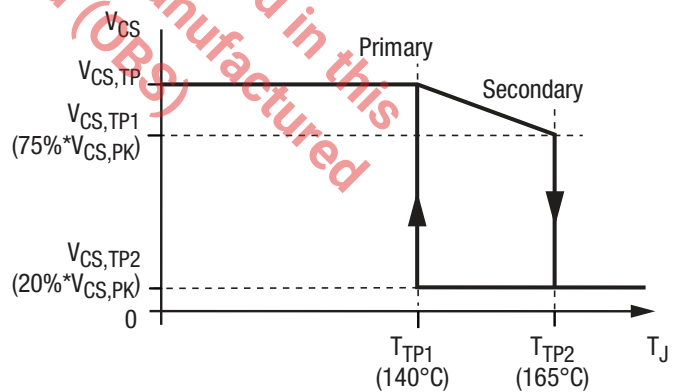


Figure 3: Dual-Mode Thermal Protection

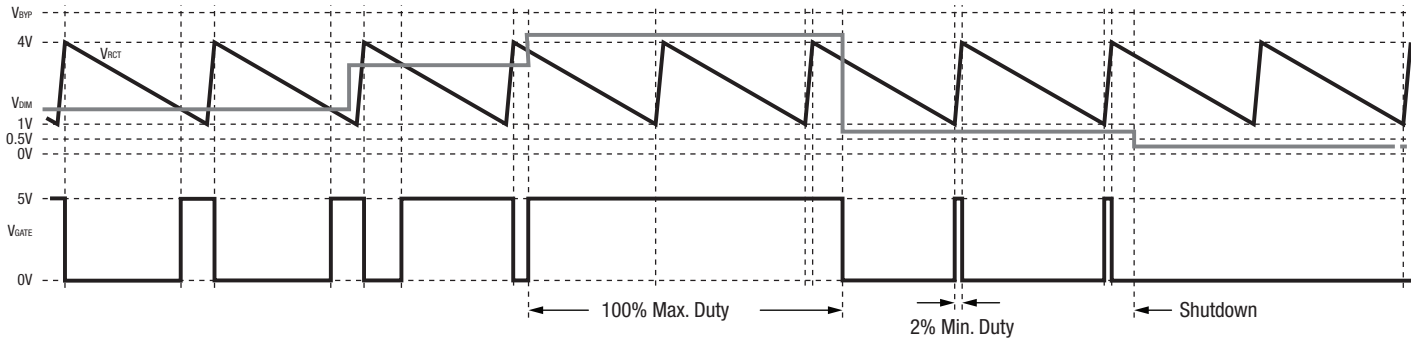


Figure 6: PWM Dimming Timing

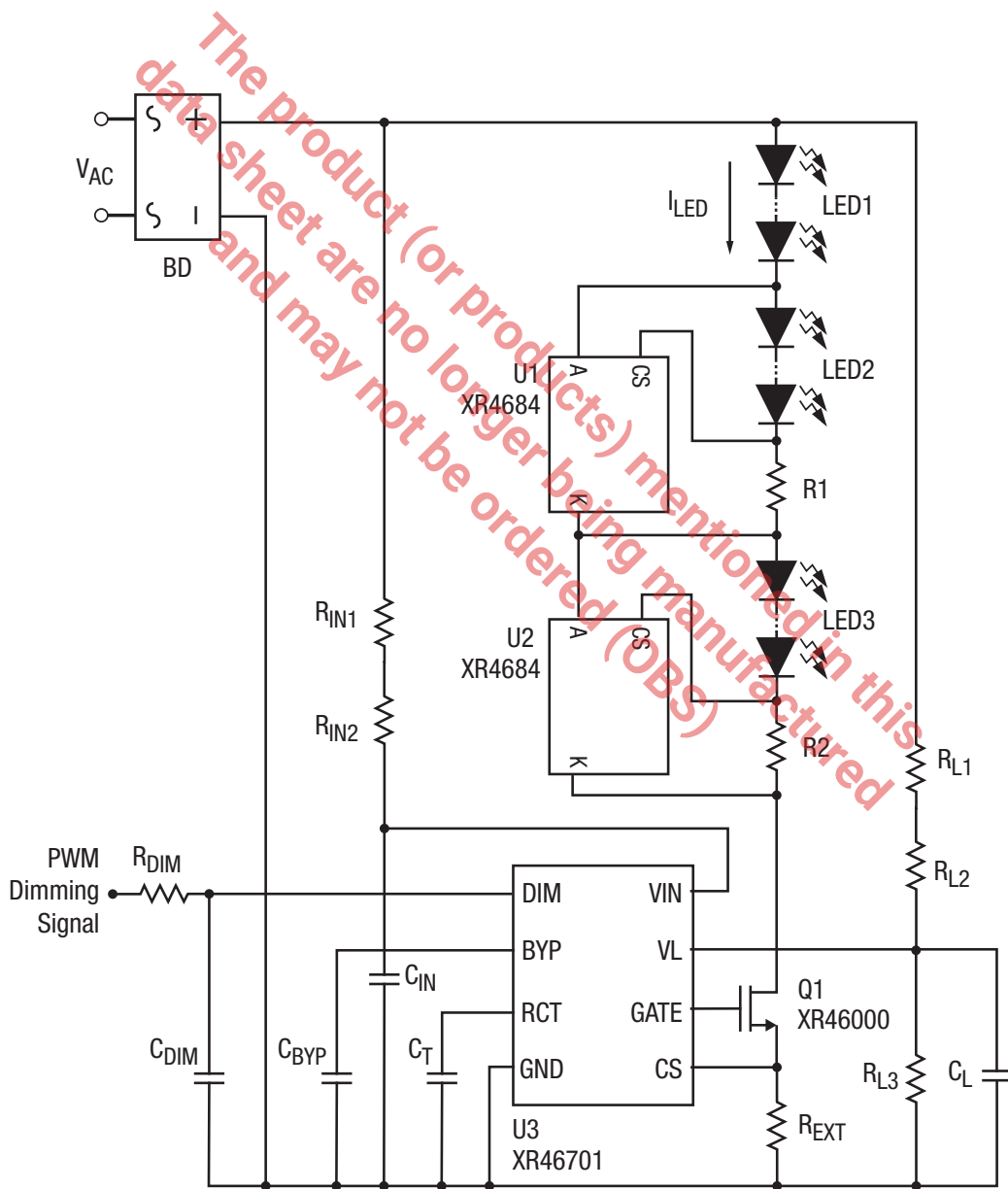
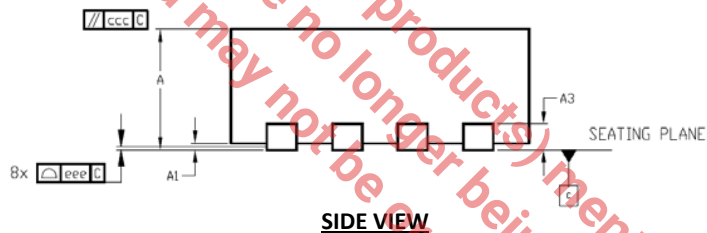
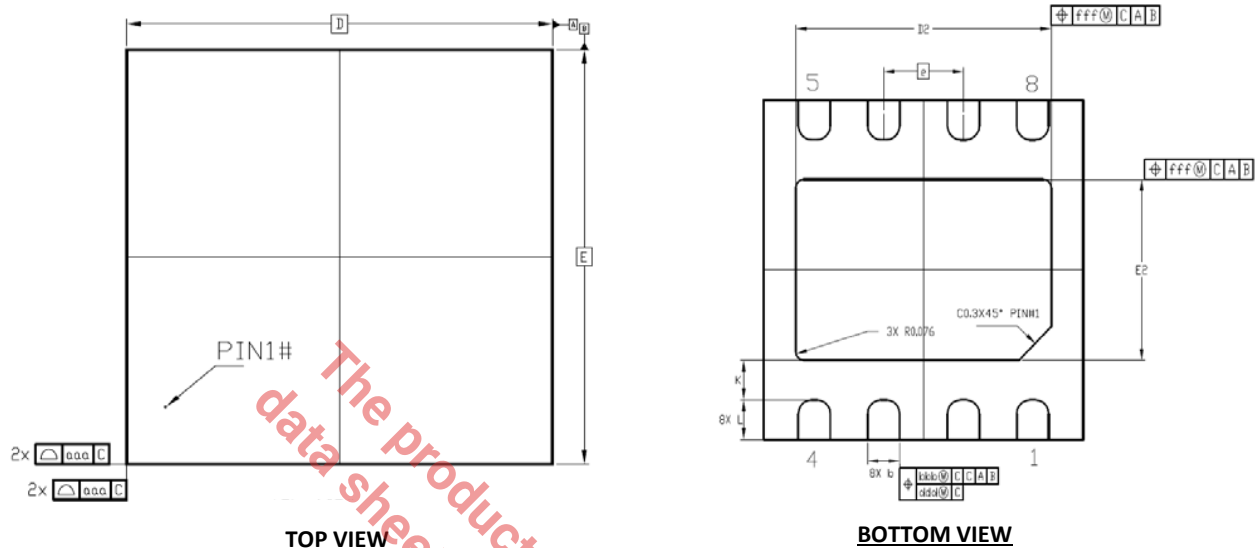


Figure 7: PWM Dimming

Mechanical Dimensions

TDFN-8



DM SYMBOL	Min	Nom	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A3	0.2Ref		
b	0.18	0.25	0.3
D	3.00 BSC		
E	3.00 BSC		
D2	2.2	2.4	2.6
E2	1.4	1.6	1.8
e	0.65 BSC		
L	0.25	0.40	0.55
K	0.20		
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

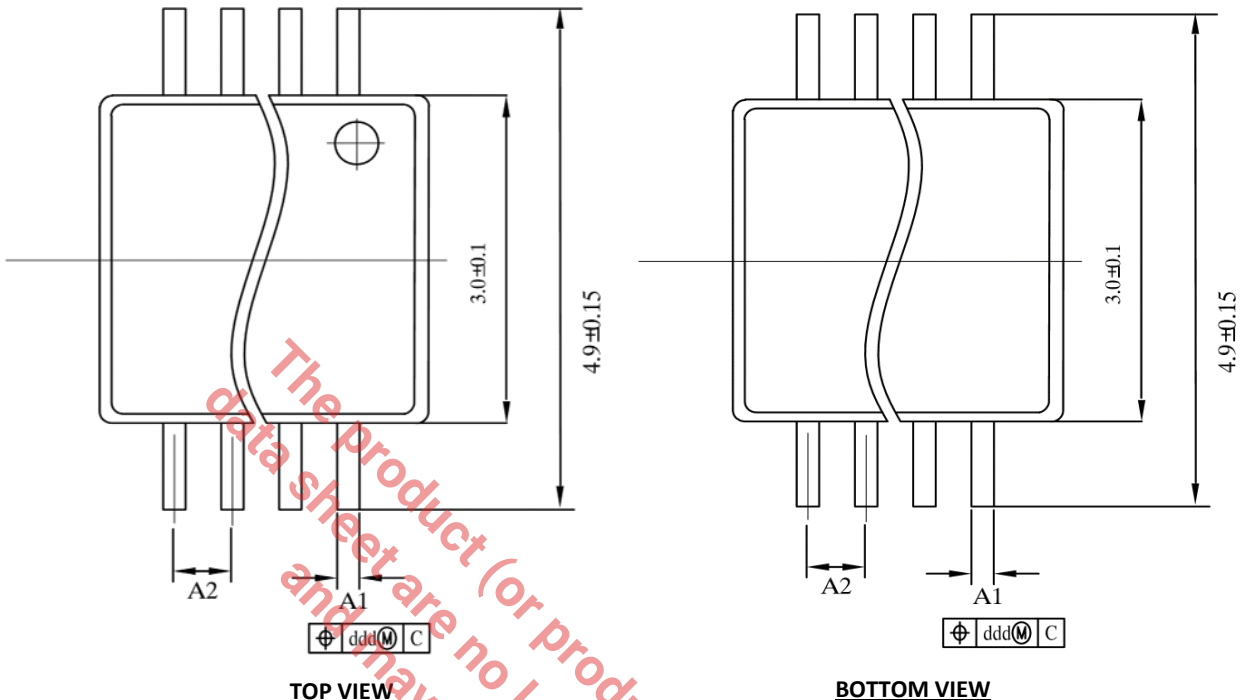
TERMINAL DETAILS

1. All dimensions are in Millimeters
2. Dimensions and tolerance per Jeduc MO-220

Drawing No. : POD - 0000088

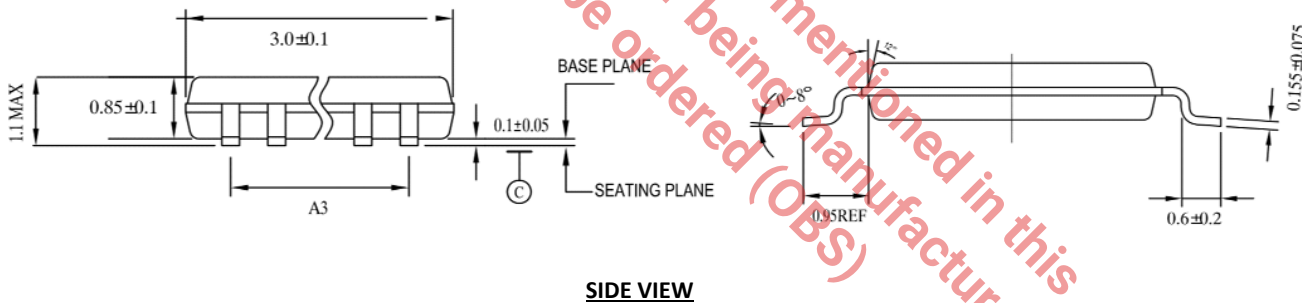
Mechanical Dimensions (Continued)

MSOP-8



TOP VIEW

BOTTOM VIEW



SIDE VIEW

LEAD	A1		A2	A3	ddd
	MIN	MAX			
8LD	0.22	0.38	0.65 BSC	1.95 BSC	0.13

TERMINAL DETAILS

1. All dimensions are in Millimeters
2. Dimensions and tolerance per Jeduc MO-187F

Drawing No. : POD - 0000127

Ordering Information⁽¹⁾

Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
XR46701IHBTR	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	Yes ⁽²⁾	DFN-8	Tape and reel
XR46701IRBTR	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		MSOP-8	Tape and reel

NOTE:

1. Refer to www.exar.com/XR46701 for most up-to-date Ordering Information.
2. Visit www.exar.com for additional information on Environmental Rating.

Revision History

Revision	Date	Description
1A	September 2017	Initial release.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)



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