COMLINEAR® CLC2600, CLC3600, CLC4600

Dual, Triple, and Quad 300MHz Amplifiers

FEATURES

- 0.1dB gain flatness to 95MHz
- 0.03%/0.04° differential gain/phase error
- 230MHz -3dB bandwidth at G = 2
- 300MHz -3dB bandwidth at G = 1
- 1,300V/μs slew rate
- 50mA output current
- 3.3mA supply current
- Fully specified at ±5V supplies
- CLC2600: Pb-free SOIC-8
- CLC3600, CLC4600: Pb-free SOIC-14

APPLICATIONS

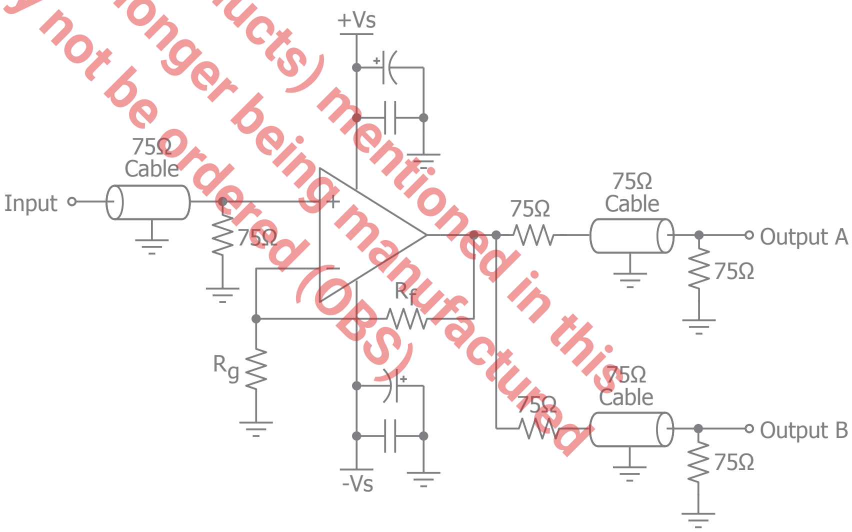
- Video line drivers
- S-Video driver
- Video switchers and routers
- ADC buffer
- Active filters
- Cable drivers
- Twisted pair driver/receiver

General Description

The *Comlinear* CLC2600 (dual), CLC3600 (triple), and CLC4600 (quad) are high-performance, current feedback amplifiers. These amplifiers provide 300MHz unity gain bandwidth, ±0.1dB gain flatness to 95MHz, and provide 1,300V/μs slew rate exceeding the requirements of high-definition television (HDTV) and other multimedia applications. These *Comlinear* high-performance amplifiers also provide ample output current to drive multiple video loads.

The *Comlinear* CLC2600, CLC3600, and CLC4600 are designed to operate from ±5V supplies. They consume only 3.3mA of supply current per channel. The combination of high-speed, low-power, and excellent video performance make these amplifiers well suited for use in many general purpose, high-speed applications including standard definition and high definition video.

Typical Application - Driving Dual Video Loads

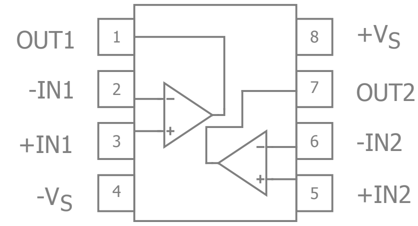


Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC2600ISO8X	SOIC-8	Yes	Yes	-40°C to +85°C	Reel
CLC3600ISO14X	SOIC-14	Yes	Yes	-40°C to +85°C	Reel
CLC4600ISO14X	SOIC-14	Yes	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1.

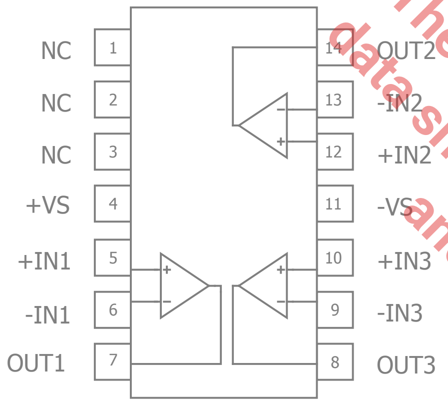
CLC2600 Pin Configuration



CLC2600 Pin Assignments

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

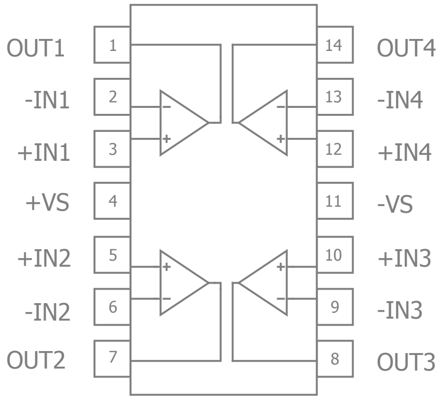
CLC3600 Pin Configuration



CLC3600 Pin Configuration

Pin No.	Pin Name	Description
1	NC	No Connect
2	NC	No Connect
3	NC	No Connect
4	$+V_S$	Positive supply
5	+IN1	Positive input, channel 1
6	-IN1	Negative input, channel 1
7	OUT1	Output, channel 1
8	OUT3	Output, channel 3
9	-IN3	Negative input, channel 3
10	+IN3	Positive input, channel 3
11	$-V_S$	Negative supply
12	+IN2	Positive input, channel 2
13	-IN2	Negative input, channel 2
14	OUT2	Output, channel 2

CLC4600 Pin Configuration



CLC4600 Pin Configuration

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$+V_S$	Positive supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	OUT3	Output, channel 3
9	-IN3	Negative input, channel 3
10	+IN3	Positive input, channel 3
11	$-V_S$	Negative supply
12	+IN4	Positive input, channel 4
13	-IN4	Negative input, channel 4
14	OUT4	Output, channel 4

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the “Absolute Maximum Ratings”. The device should not be operated at these “absolute” limits. Adhere to the “Recommended Operating Conditions” for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	±7 or 14	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
8-Lead SOIC		100		°C/W
14-Lead SOIC		88		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOIC-8	SOIC-14
Human Body Model (HBM)	2.5kV	2.5kV
Charged Device Model (CDM)	2kV	2kV

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	±4		±6	V

Electrical Characteristics

T_A = 25°C, V_S = ±5V, R_f = 510Ω, R_L = 100Ω, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}, R_f = 1.24kΩ		300		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		230		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 4V_{pp}		155		MHz
$BW_{0.1dBSS}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 0.2V_{pp}		95		MHz
$BW_{0.1dBLS}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 4V_{pp}		55		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 2V step; (10% to 90%)		1.8		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		20		ns
OS	Overshoot	V_{OUT} = 0.2V step		2.5		%
SR	Slew Rate	4V step		1300		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	2V_{pp}, 1MHz		-80		dBc
HD3	3rd Harmonic Distortion	2V_{pp}, 1MHz		-86		dBc
THD	Total Harmonic Distortion	2V_{pp}, 1MHz		-79.5		dB
D_G	Differential Gain	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.03		%
D_P	Differential Phase	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.04		°
e_n	Input Voltage Noise	> 1MHz		6.4		nV/√Hz
i_{n+}	Input Current Noise (+)	> 1MHz		1.0		pA/√Hz
i_{n-}	Input Current Noise (-)	> 1MHz		9.3		pA/√Hz
X_{TALK}	Crosstalk	Channel-to-channel 5MHz		-56		dB
DC Performance						
V_{IO}	Input Offset Voltage(1)		-8	1.4	+8	mV
dV_{IO}	Average Drift			15		µV/°C
I_{bn}	Input Bias Current Non-inverting(1)		-3	1.3	3	µA
dI_{bn}	Average Drift			2.6		nA/°C
I_{bi}	Input Bias Current Inverting(1)		-18	4.4	18	µA
dI_{bi}	Average Drift			16		nA/°C
PSRR	Power Supply Rejection Ratio(1)	DC	60	65		dB
A_{OL}	Open-Loop Transresistance	V_{OUT} = V_S / 2		580		kΩ
I_S	Supply Current(1)	CLC2600 Total		6.6	10	mA
		CLC3600 Total		13.2	20	mA
		CLC4600 Total		13.2	20	mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		19		MΩ
C_{IN}	Input Capacitance			1		pF
CMIR	Common Mode Input Range			±2.3		V
CMRR	Common Mode Rejection Ratio(1)	DC	52	57		dB
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		110		mΩ
V_{OUT}	Output Voltage Swing	R_L = 100Ω (1)	-2.6	±3	2.6	V
		R_L = 1kΩ		±3.3		V
I_{OUT}	Output Current			50		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		67		mA

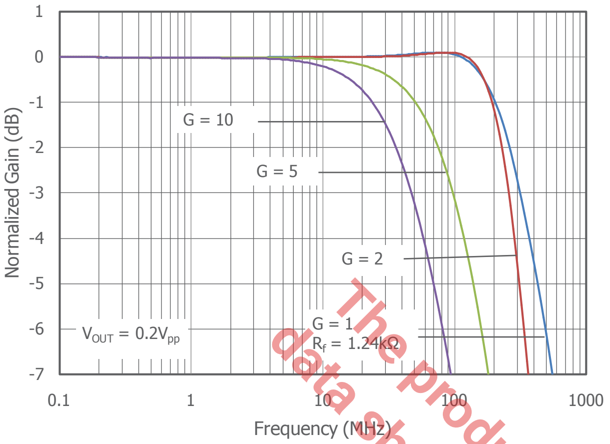
Notes:

1. 100% tested at 25°C

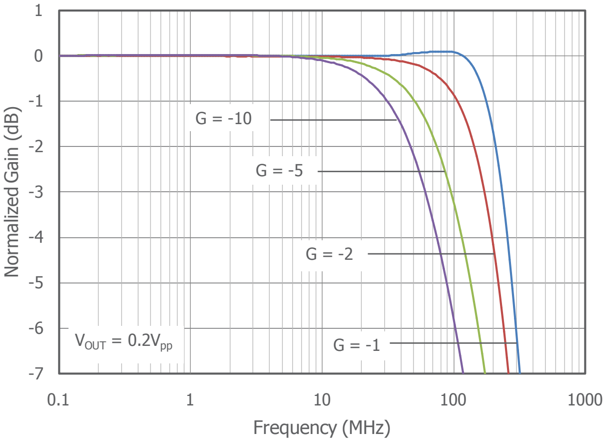
Typical Performance Characteristics

$T_A = 25°C$, $V_s = ±5V$, $R_f = 510\Omega$, $R_L = 100\Omega$, $G = 2$; unless otherwise noted.

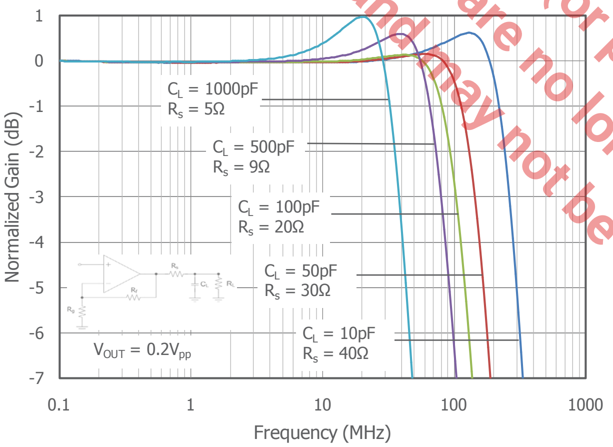
Non-Inverting Frequency Response



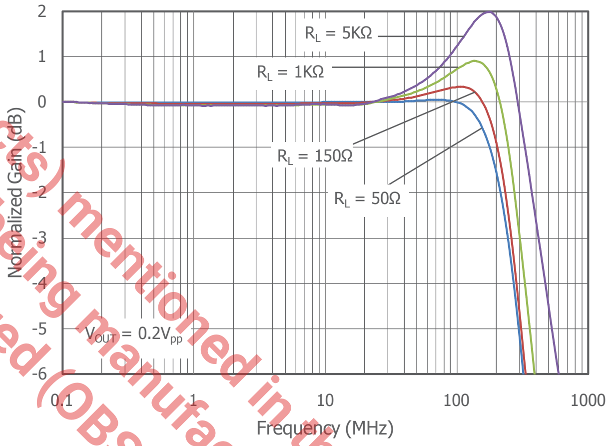
Inverting Frequency Response



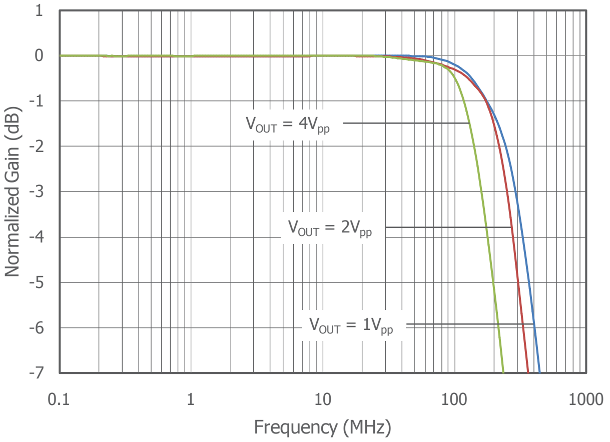
Frequency Response vs. C_L



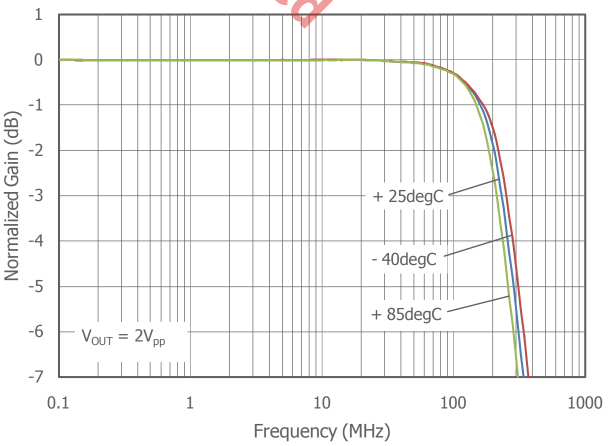
Frequency Response vs. R_L



Frequency Response vs. V_{OUT}



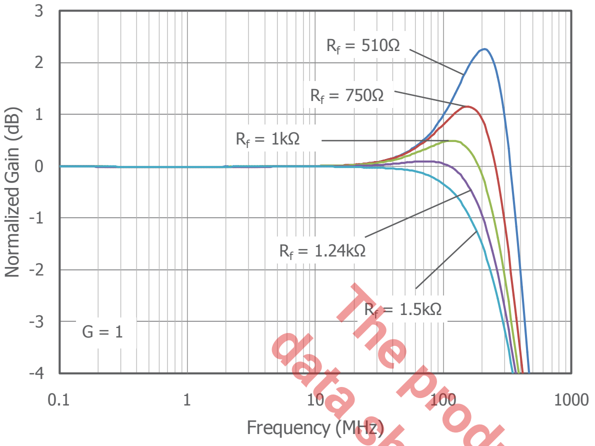
Frequency Response vs. Temperature



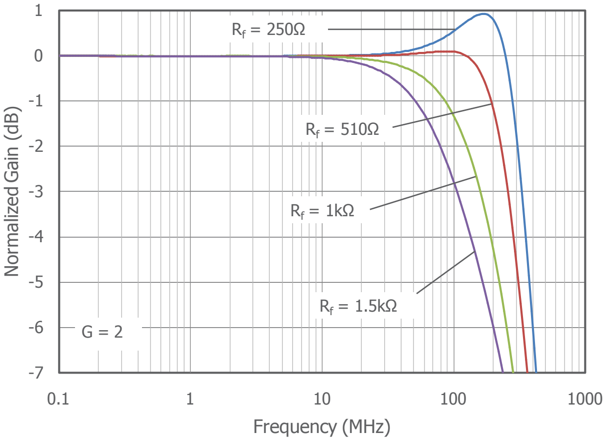
Typical Performance Characteristics - Continued

T_A = 25°C, V_s = ±5V, R_f = 510Ω, R_L = 100Ω, G = 2; unless otherwise noted.

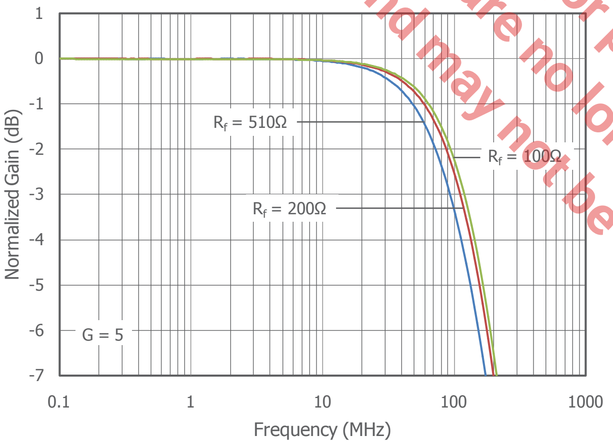
Frequency Response vs. R_f at G=1



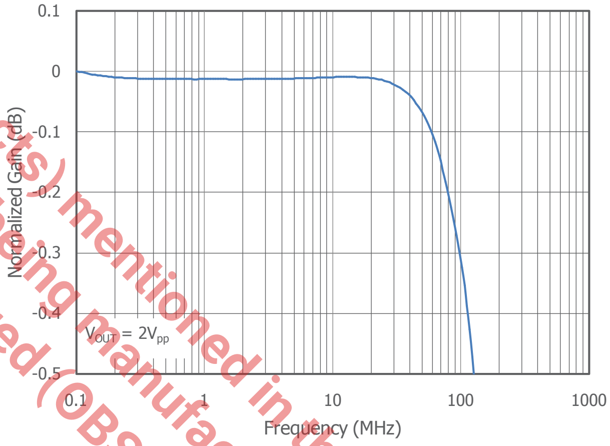
Frequency Response vs. R_f at G=2



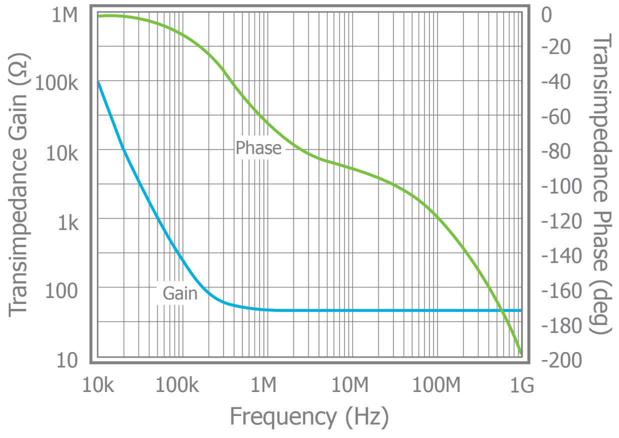
Frequency Response vs. R_f at G=5



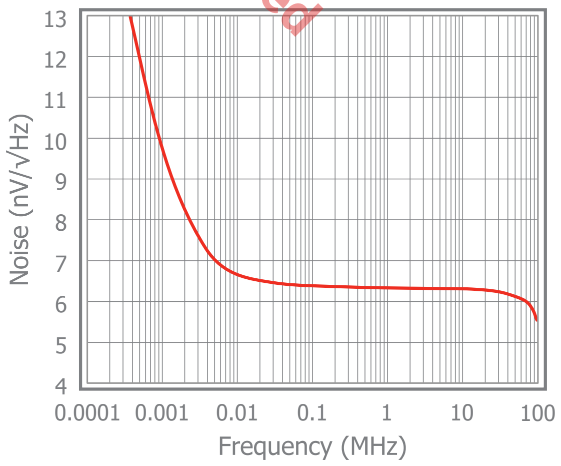
Gain Flatness



Open Loop Transimpendance Gain/Phase vs. Frequency



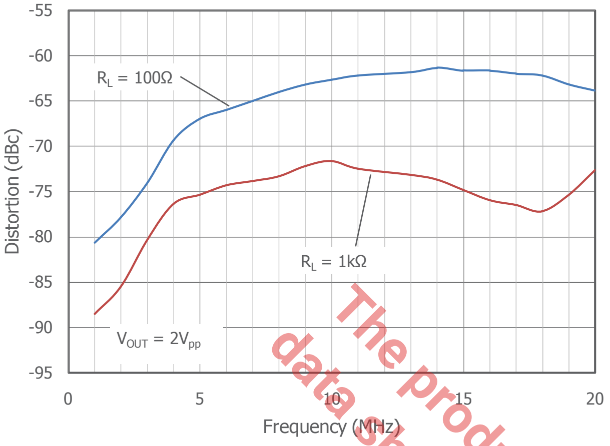
Input Voltage Noise



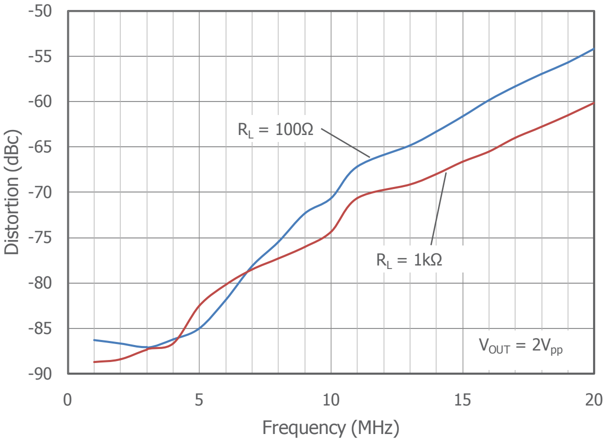
Typical Performance Characteristics - Continued

T_A = 25°C, V_s = ±5V, R_f = 510Ω, R_L = 100Ω, G = 2; unless otherwise noted.

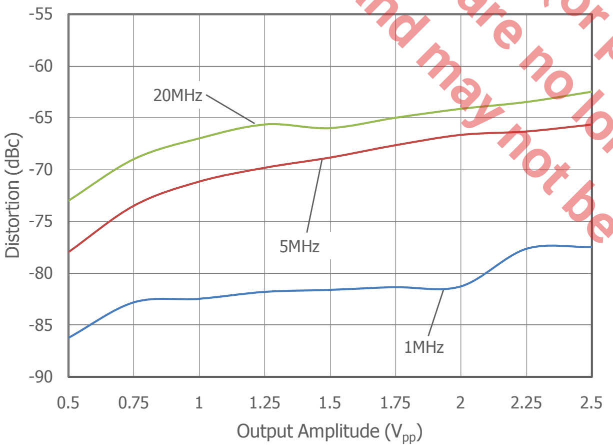
2nd Harmonic Distortion vs. R_L



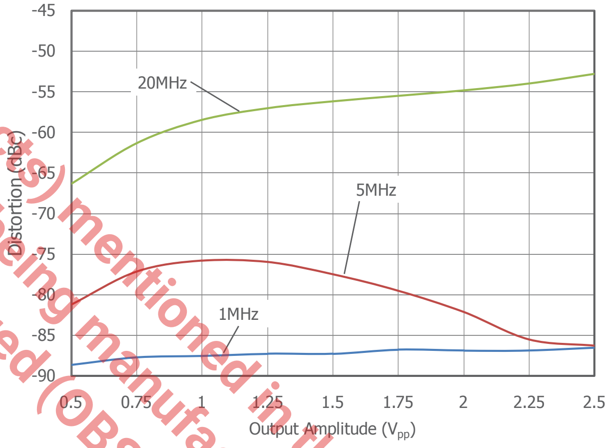
3rd Harmonic Distortion vs. R_L



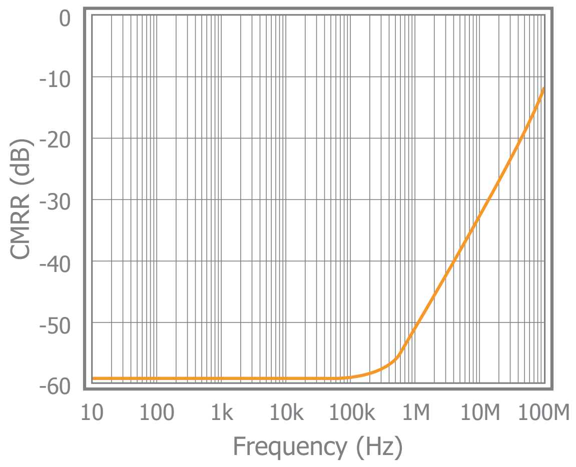
2nd Harmonic Distortion vs. V_{OUT}



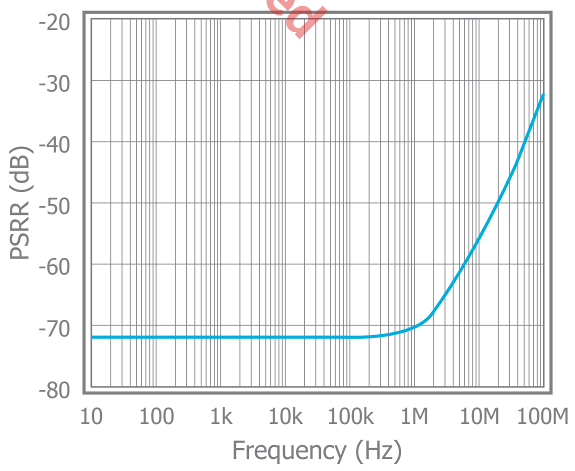
3rd Harmonic Distortion vs. V_{OUT}



CMRR vs. Frequency



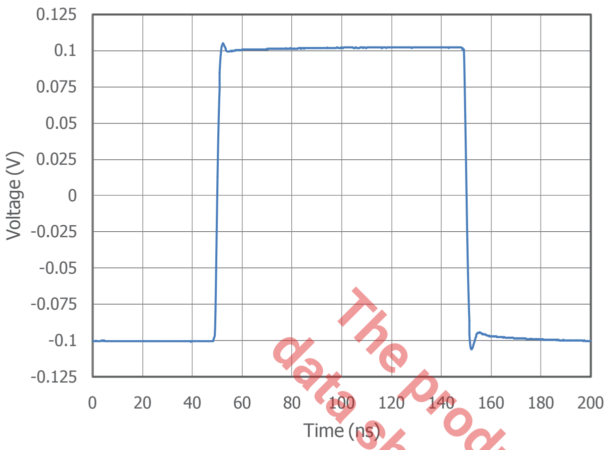
PSRR vs. Frequency



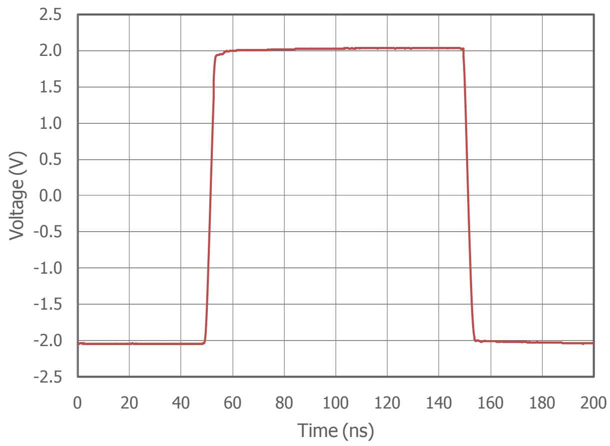
Typical Performance Characteristics - Continued

$T_A = 25°C$, $V_s = ±5V$, $R_f = 510Ω$, $R_L = 100Ω$, $G = 2$; unless otherwise noted.

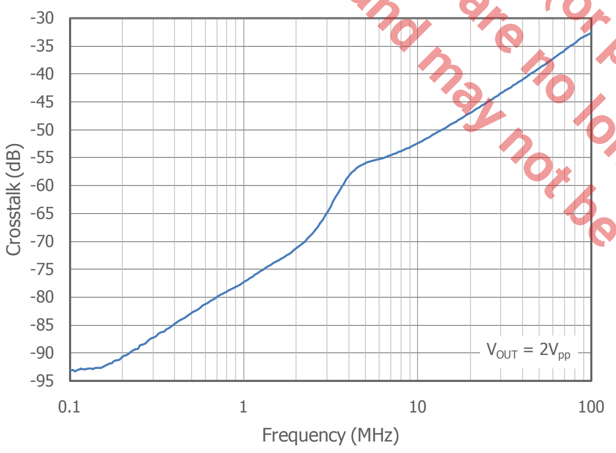
Small Signal Pulse Response



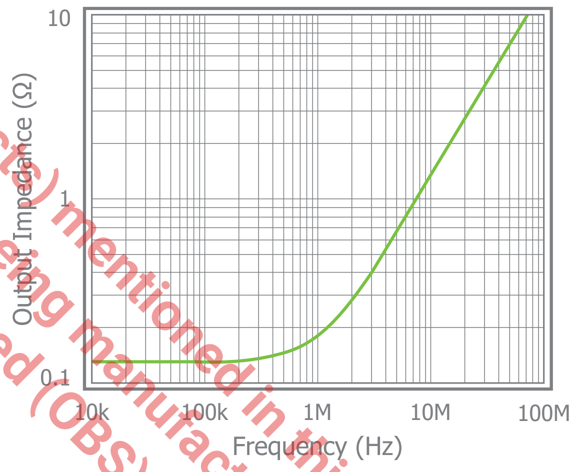
Large Signal Pulse Response



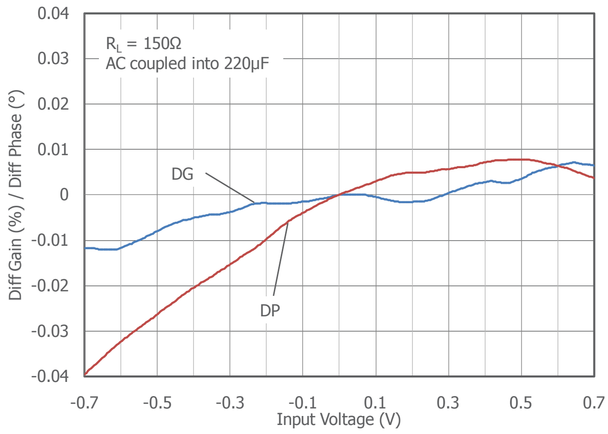
Crosstalk vs. Frequency



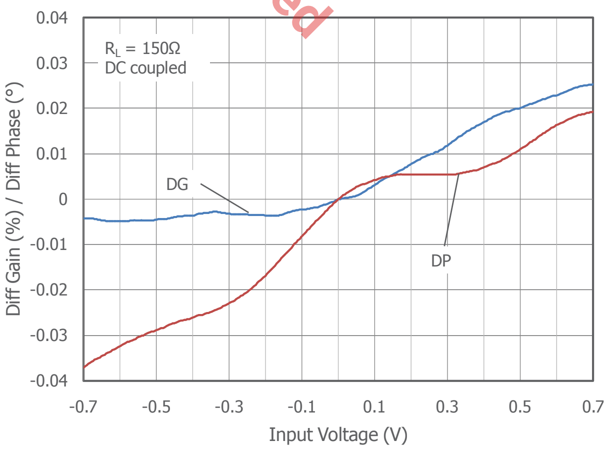
Closed Loop Output Impedance vs. Frequency



Differential Gain & Phase AC Coupled



Differential Gain & Phase DC Coupled



General Information - Current Feedback Technology

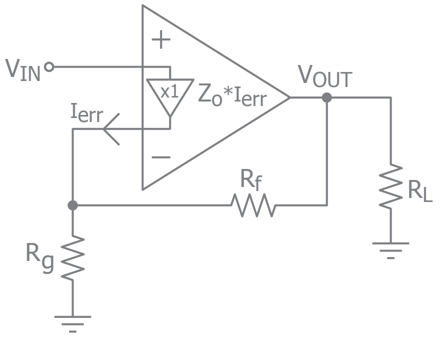
Advantages of CFB Technology

The CLCx600 Family of amplifiers utilize current feedback (CFB) technology to achieve superior performance. The primary advantage of CFB technology is higher slew rate performance when compared to voltage feedback (VFB) architecture. High slew rate contributes directly to better large signal pulse response, full power bandwidth, and distortion.

CFB also alleviates the traditional trade-off between closed loop gain and usable bandwidth that is seen with a VFB amplifier. With CFB, the bandwidth is primarily determined by the value of the feedback resistor, R_f. By using optimum feedback resistor values, the bandwidth of a CFB amplifier remains nearly constant with different gain configurations.

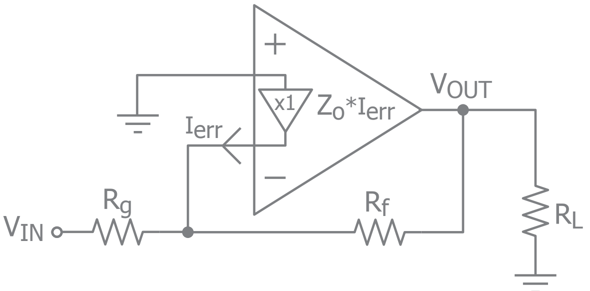
When designing with CFB amplifiers always abide by these basic rules:

- Use the recommended feedback resistor value
- Do not use reactive (capacitors, diodes, inductors, etc.) elements in the direct feedback path
- Avoid stray or parasitic capacitance across feedback resistors
- Follow general high-speed amplifier layout guidelines
- Ensure proper precautions have been made for driving capacitive loads



$$\frac{V_{OUT}}{V_{IN}} = \left(1+\frac{R_f}{R_g}\right) + \left(\frac{1}{1+\frac{R_f}{Z_{o(j\omega)}}}\right) \qquad \text{Eq. 1}$$

Figure 1. Non-Inverting Gain Configuration with First Order Transfer Function



$$\frac{V_{OUT}}{V_{IN}} = \left(-\frac{R_f}{R_g}\right) + \left(\frac{1}{1+\frac{R_f}{Z_{o(j\omega)}}}\right) \qquad \text{Eq. 2}$$

Figure 2. Inverting Gain Configuration with First Order Transfer Function

CFB Technology - Theory of Operation

Figure 1 shows a simple representation of a current feedback amplifier that is configured in the traditional non-inverting gain configuration.

Instead of having two high-impedance inputs similar to a VFB amplifier, the inputs of a CFB amplifier are connected across a unity gain buffer. This buffer has a high impedance input and a low impedance output. It can source or sink current (I_{err}) as needed to force the non-inverting input to track the value of Vin. The CFB architecture employs a high gain trans-impedance stage that senses Ierr and drives the output to a value of ($Z_o(j\omega)$ * I_{err}) volts. With the application of negative feedback, the amplifier will drive the output to a voltage in a manner which tries to drive Ierr to zero. In practice, primarily due to limitations on the value of $Z_o(j\omega)$, Ierr remains a small but finite value.

A closer look at the closed loop transfer function (Eq.1) shows the effect of the trans-impedance, $Z_o(j\omega)$ on the gain of the circuit. At low frequencies where $Z_o(j\omega)$ is very large with respect to R_f, the second term of the equation approaches unity, allowing R_f and R_g to set the gain. At higher frequencies, the value of $Z_o(j\omega)$ will roll off, and the effect of the secondary term will begin to dominate. The -3dB small signal parameter specifies the frequency where the value $Z_o(j\omega)$ equals the value of R_f causing the gain to drop by 0.707 of the value at DC.

For more information regarding current feedback amplifiers, visit www.exar.com for detailed application notes, such as AN-3: *The Ins and Outs of Current Feedback Amplifiers*.

Application Information

Basic Operation

Figures 3, 4, and 5 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations.

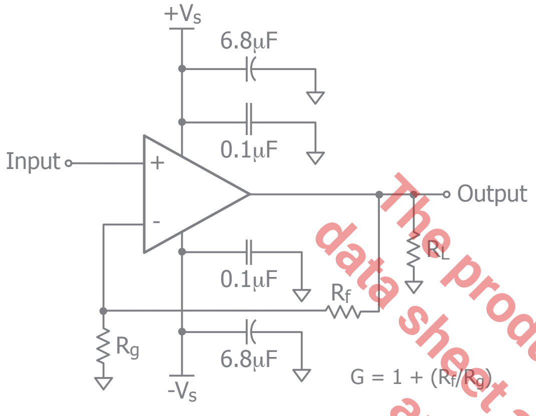


Figure 3. Typical Non-Inverting Gain Circuit

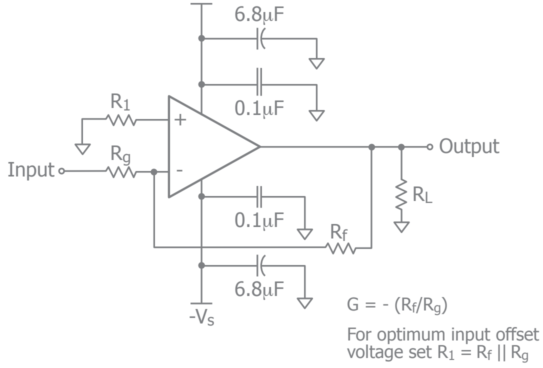


Figure 4. Typical Inverting Gain Circuit

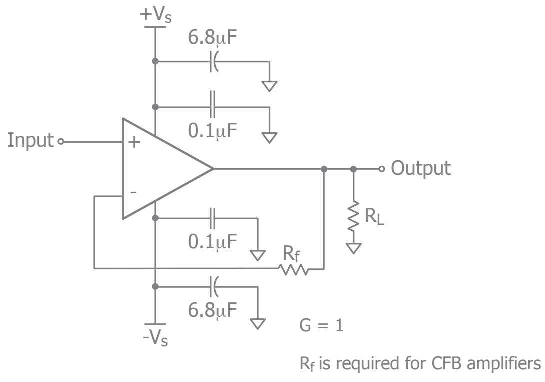


Figure 5. Typical Unity Gain (G=1) Circuit

CFB amplifiers can be used in unity gain configurations. Do not use the traditional voltage follower circuit, where the output is tied directly to the inverting input. With a CFB amplifier, a feedback resistor of appropriate value must be used to prevent unstable behavior. Refer to figure 5 and Table 1. Although this seems cumbersome, it does allow a degree of freedom to adjust the passband characteristics.

Feedback Resistor Selection

One of the key design considerations when using a CFB amplifier is the selection of the feedback resistor, R_f. R_f is used in conjunction with R_g to set the gain in the traditional non-inverting and inverting circuit configurations. Refer to figures 3 and 4. As discussed in the Current Feedback Technology section, the value of the feedback resistor has a pronounced effect on the frequency response of the circuit.

Table 1, provides recommended R_f and associated R_g values for various gain settings. These values produce the optimum frequency response, maximum bandwidth with minimum peaking. Adjust these values to optimize performance for a specific application. The typical performance characteristics section includes plots that illustrate how the bandwidth is directly affected by the value of R_f at various gain settings.

Gain (V/V)	R_f (Ω)	R_g (Ω)	±0.1dB BW (MHz)	-3dB BW (MHz)
1	1240	-	129	300
2	510	510	140	230
5	200	50	18	111

Table 1: Recommended R_f vs. Gain

In general, lowering the value of R_f from the recommended value will extend the bandwidth at the expense of additional high frequency gain peaking. This will cause increased overshoot and ringing in the pulse response characteristics. Reducing R_f too much will eventually cause oscillatory behavior.

Increasing the value of Rf will lower the bandwidth. Lowering the bandwidth creates a flatter frequency response and improves 0.1dB bandwidth performance. This is important in applications such as video. Further increase in Rf will cause premature gain rolloff and adversely affect gain flatness.

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 6.

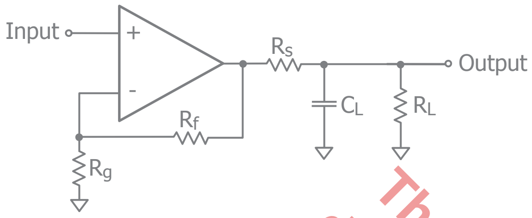


Figure 6. Addition of R_S for Driving Capacitive Loads

Table 2 provides the recommended R_S for various capacitive loads. The recommended R_S values result in <=0.5dB peaking in the frequency response. The Frequency Response vs. C_L plot, on page 5, illustrates the response of the CLCx600 Family.

C_L (pF)	R_S (Ω)	-3dB BW (MHz)
10	40	265
50	30	140
100	20	105

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Parasitic Capacitance on the Inverting Input

Physical connections between components create unintentional or parasitic resistive, capacitive, and inductive elements.

Parasitic capacitance at the inverting input can be especially troublesome with high frequency amplifiers. A parasitic capacitance on this node will be in parallel with the gain setting resistor R_g. At high frequencies, its impedance can begin to raise the system gain by making R_g appear smaller.

In general, avoid adding any additional parasitic capacitance at this node. In addition, stray capacitance across the R_f resistor can induce peaking and high frequency ringing. Refer to the **Layout Considerations** section for additional information regarding high speed layout techniques.

Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLCx600 Family will typically recover in less than 10ns from an overdrive condition. Figure 7 shows the CLC2600 in an overdriven condition.

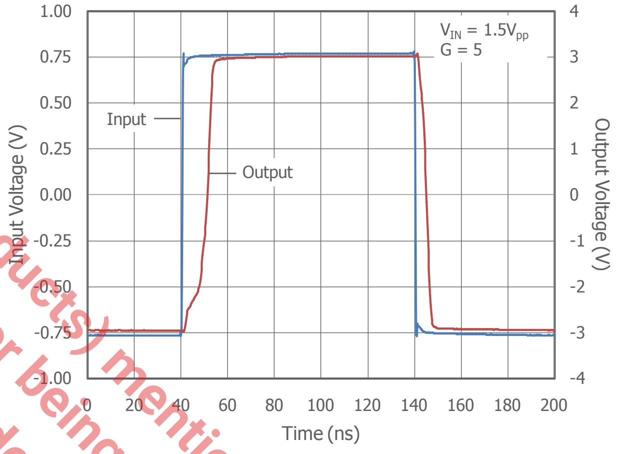


Figure 7. Overdrive Recovery

Power Dissipation

For most applications, the power dissipation due to driving external loads should be low enough to ensure a safe operating condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value Theta_{JA} (Θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\Theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$P_D = P_{supply} - P_{load}$

Supply power is calculated by the standard power equation.

$P_{supply} = V_{supply} \times I_{RMS\ supply}$

$V_{supply} = V_{S+} - V_{S-}$

Power delivered to a purely resistive load is:

$P_{load} = ((V_{LOAD})_{RMS}{}^2)/Rload_{eff}$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in figure 3 would be calculated as:

$R_L \mid\mid (R_f + R_g)$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$P_D = P_{Quiescent} + P_{Dynamic} - P_{Load}$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply}. Load power can be calculated as above with the desired signal amplitudes using:

$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$

$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / Rload_{eff}$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

Figure 8 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8 and 14 lead SOIC packages.

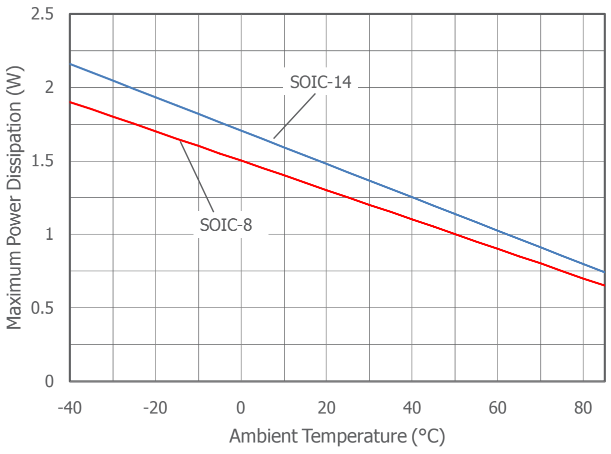


Figure 8. Maximum Power Derating

Better thermal ratings can be achieved by maximizing PC board metallization at the package pins. However, be careful of stray capacitance on the input pins.

In addition, increased airflow across the package can also help to reduce the effective Θ_{JA} of the package.

In the event the outputs are momentarily shorted to a low impedance path, internal circuitry and output metallization are set to limit and handle up to 65mA of output current. However, extended duration under these conditions may not guarantee that the maximum junction temperature (+150°C) is not exceeded.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Exar has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.1μF ceramic capacitors for power supply decoupling
- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB006	CLC2600
CEB018	CLC3600, CLC4600

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 9-14. These evaluation boards are built for dual- supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the -V_S pin of the amplifier is not directly connected to the ground plane.

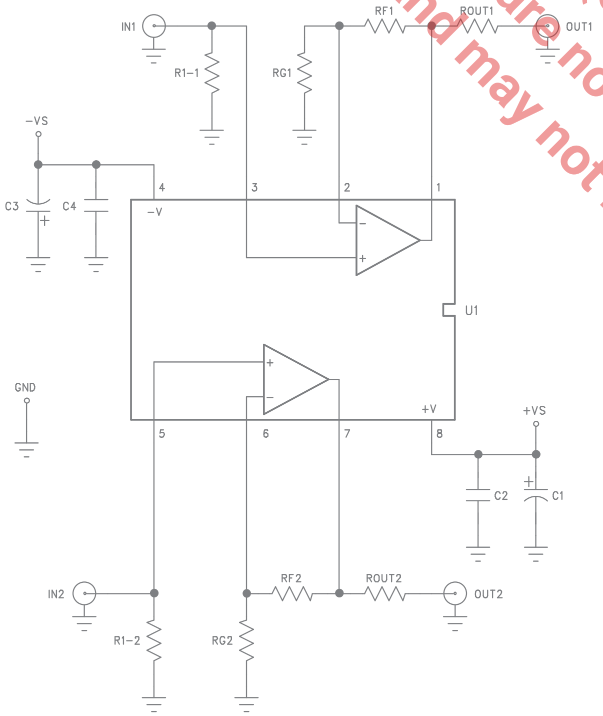


Figure 9. CEB006 Schematic

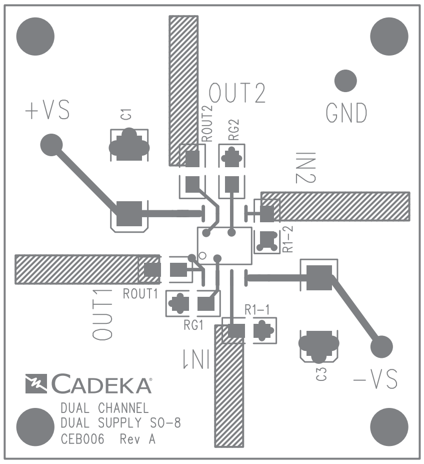


Figure 10. CEB006 Top View

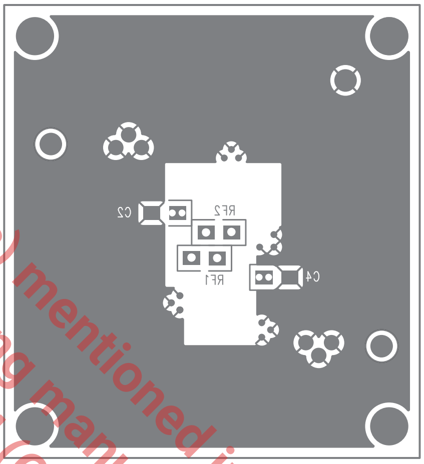


Figure 11. CEB006 Bottom View

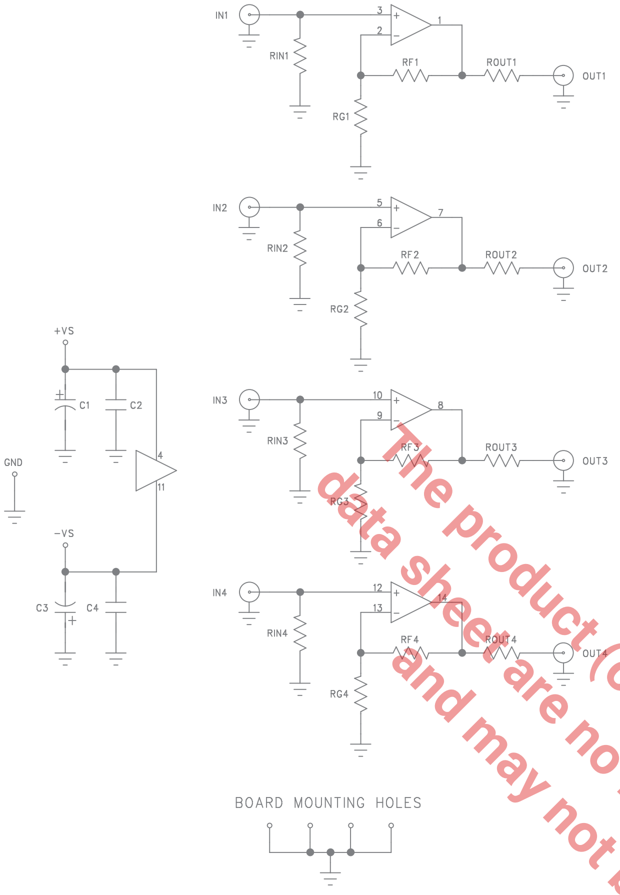


Figure 12. CEB018 Schematic

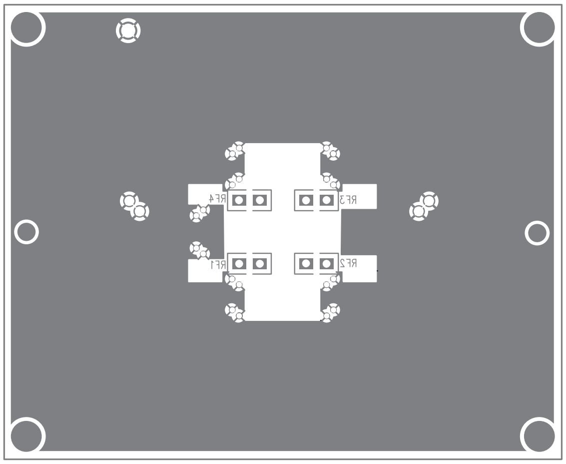


Figure 14. CEB018 Bottom View

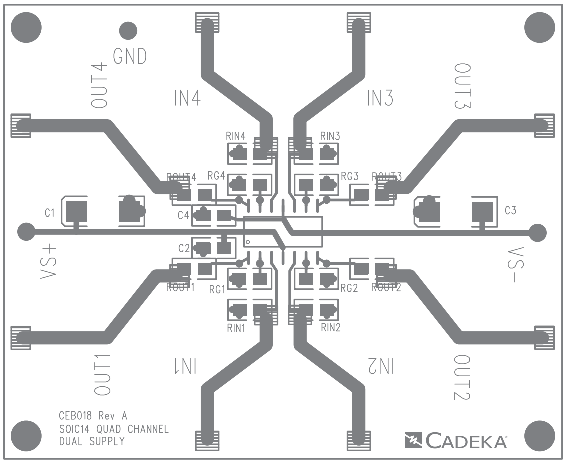
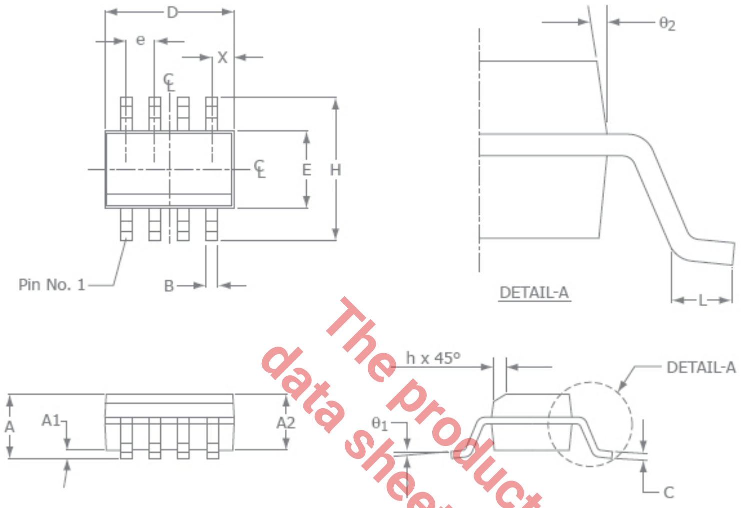


Figure 13. CEB018 Top View

Mechanical Dimensions

SOIC-8 Package



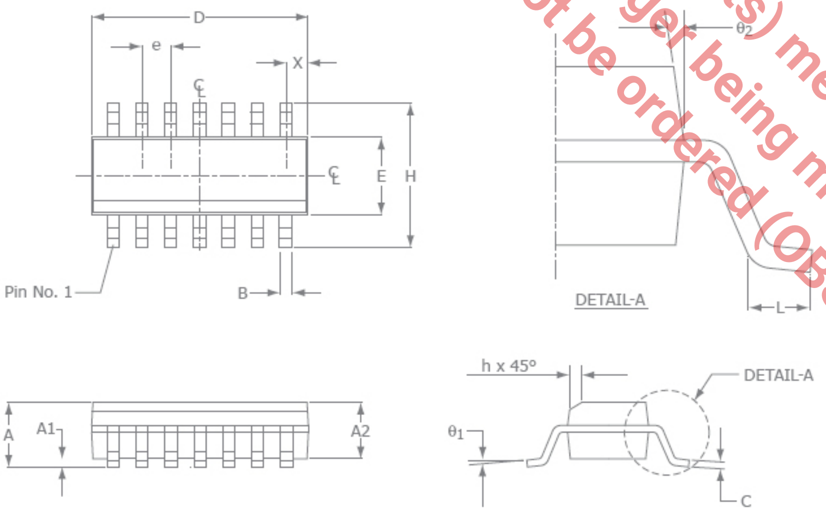
SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ1	0°	8°
X	0.55 ref	
θ2	7° BSC	

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

SOIC-14 Package



SOIC-14		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	8.56	8.74
E	3.84	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ1	0°	8°
X	0.51 ref	
θ2	7° BSC	

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") ma
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

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