Data Sheet

COMLINEAR® CLC2000, CLC4000

High Output Current Dual and Quad Amplifiers

FEATURES

- 9.4V_{pp} output drive into R_L = 25Ω
- Using both amplifiers, 18.8V_{pp} differential output drive into R_L = 25Ω
- ±200mA @ V_o = 9.4V_{pp}
- 0.009%/0.06° differential gain/phase error
- 250MHz -3dB bandwidth at G = 2
- 510MHz -3dB bandwidth at G = 1
- 210V/µs slew rate
- 4.5nV/√Hz input voltage noise
- 2.7pA/√Hz input current noise
- 7mA supply current
- Fully specified at 5V and 12V supplies

APPLICATIONS

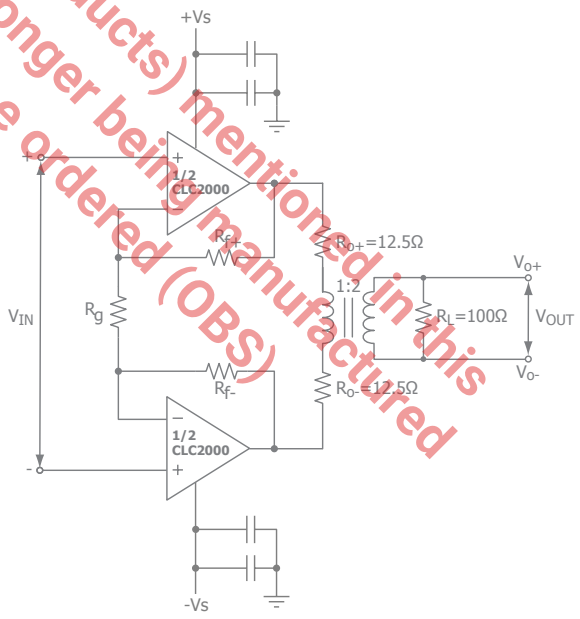
- ADSL PCI modem cards
- ADSL external modems
- Cable drivers
- Video line driver
- Twisted pair driver/receiver
- Power line communications

General Description

The *Comlinear* CLC2000 and CLC4000 are dual and quad voltage feedback amplifiers that offer ±200mA of output current at 9.4V_{pp}. The CLC2000 and CLC4000 are capable of driving signals to within 1V of the power rails. When connected as a differential line driver, the amplifier drives signals up to 18.8Vpp into a 25Ω load, which supports the peak upstream power levels for upstream full-rate ADSL CPE applications.

The *Comlinear* CLC2000 and CLC4000 can operate from single or dual supplies from 5V to 12V. It consumes only 7mA of supply current per channel. The combination of wide bandwidth, low noise, low distortion, and high output current capability makes the CLC2000 and CLC4000 ideally suited for Customer Premise ADSL or video line driving applications.

Typical Application - ADSL Application



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS).

Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packaging Method
CLC2000ISO8X	SOIC-8	Yes	-40°C to +85°C	Reel
CLC2000ISO8	SOIC-8	Yes	-40°C to +85°C	Rail
CLC4000ISO14X	SOIC-14	Yes	-40°C to +85°C	Reel
CLC4000ISO14	SOIC-14	Yes	-40°C to +85°C	Rail

Moisture sensitivity level for all parts is MSL-1.

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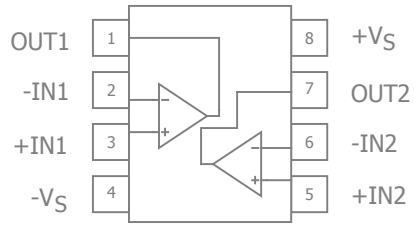
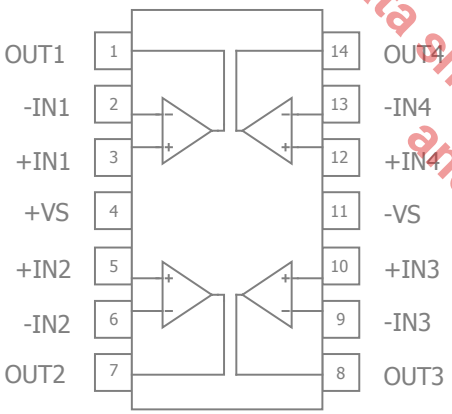
CLC2000 Pin Configuration



CLC2000 Pin Assignments

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

CLC4000 Pin Configuration



CLC4000 Pin Assignments

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$+V_S$	Positive supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	OUT3	Output, channel 3
9	-IN3	Negative input, channel 3
10	+IN3	Positive input, channel 3
11	$-V_S$	Negative supply
12	+IN4	Positive input, channel 4
13	-IN4	Negative input, channel 4
14	OUT4	Output, channel 4

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Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	±7 or 14	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
8-Lead SOIC		100		°C/W
14-Lead SOIC		88		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	
Human Body Model (HBM)	2.5kV
Charged Device Model (CDM)	2kV

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	±2.5		±6.5	V

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Electrical Characteristics

T_A = 25°C, V_S = 5V, R_f = R_g = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}, R_f = 0		422		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		236		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		68		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 0.2V_{pp}		77		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 1V step; (10% to 90%)		3.7		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		20		ns
OS	Overshoot	V_{OUT} = 0.2V step		6		%
SR	Slew Rate	V_{OUT} = 2V step		200		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	2V_{pp}, 100KHz, R_L = 25Ω		-83		dBc
		2V_{pp}, 1MHz, R_L = 100Ω		-85		dBc
HD3	3rd Harmonic Distortion	2V_{pp}, 100KHz, R_L = 25Ω		-86		dBc
		2V_{pp}, 1MHz, R_L = 100Ω		-82		dBc
D_G	Differential Gain	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.01		%
D_P	Differential Phase	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.05		°
e_n	Input Voltage Noise	> 1MHz		4.2		nV/√Hz
i_n	Input Current Noise	> 1MHz		2.7		pA/√Hz
X_{TALK}	Crosstalk	Channel-to-channel 5MHz		-63		dB
DC Performance						
V_{IO}	Input Offset Voltage			0.3		mV
dV_{IO}	Average Drift			0.383		µV/°C
I_{IO}	Input Offset Current			0.2		µA
I_b	Input Bias Current			10		µA
dI_{bni}	Average Drift			2.5		nA/°C
PSRR	Power Supply Rejection Ratio	DC		81		dB
A_{OL}	Open-Loop Gain	R_L = 25Ω		76		dB
I_S	Supply Current	per channel		6.75		mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		2.5		MΩ
C_{IN}	Input Capacitance			1		pF
CMIR	Common Mode Input Range			0.4 to 4.6		V
CMRR	Common Mode Rejection Ratio	DC		80		dB
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		0.01		Ω
V_{OUT}	Output Voltage Swing	R_L = 25Ω		0.95 to 4.05		V
		R_L = 1kΩ		0.75 to 4.25		V
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		1000		mA

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Electrical Characteristics

T_A = 25°C, V_S = 12V, R_f = R_g = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}, R_f = 0		510		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		250		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 4V_{pp}		35		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 0.2V_{pp}		32		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 4V step; (10% to 90%)		13.3		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		20		ns
OS	Overshoot	V_{OUT} = 0.2V step		2		%
SR	Slew Rate	V_{OUT} = 4V step		210		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	2V_{pp}, 100KHz, R_L = 25Ω		-84		dBc
		2V_{pp}, 1MHz, R_L = 100Ω		-86		dBc
		8.4V_{pp}, 100KHz, R_L = 25Ω		-63		dBc
		8.4V_{pp}, 1MHz, R_L = 100Ω		-82		dBc
HD3	3rd Harmonic Distortion	2V_{pp}, 100KHz, R_L = 25Ω		-88		dBc
		2V_{pp}, 1MHz, R_L = 100Ω		-80		dBc
		8.4V_{pp}, 100KHz, R_L = 25Ω		-63		dBc
		8.4V_{pp}, 1MHz, R_L = 100Ω		-83		dBc
D_G	Differential Gain	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.009		%
D_P	Differential Phase	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.06		°
e_n	Input Voltage Noise	> 1MHz		4.5		nV/√Hz
i_n	Input Current Noise	> 1MHz		2.7		pA/√Hz
X_{TALK}	Crosstalk	Channel-to-channel 5MHz		-62		dB
DC Performance						
V_{IO}	Input Offset Voltage(1)		-6	0.3	6	mV
dV_{IO}	Average Drift			0.383		µV/°C
I_{IO}	Input Offset Current(1)		-2	0.2	2	µA
I_b	Input Bias Current(1)			10	20	µA
dI_{bni}	Average Drift			2.5		nA/°C
PSRR	Power Supply Rejection Ratio(1)	DC	73	81		dB
A_{OL}	Open-Loop Gain	R_L = 25		76		dB
I_S	Supply Current(1)	per channel		7	12	mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		2.5		MΩ
C_{IN}	Input Capacitance			1		pF
CMIR	Common Mode Input Range			0.6 to 11.4		V
CMRR	Common Mode Rejection Ratio(1)	DC	70	79		dB
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		0.01		Ω
V_{OUT}	Output Voltage Swing	R_L = 25Ω (1)	1.5	1.2 to 10.8	10.5	V
		R_L = 1kΩ		0.8 to 11.2		V
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		1000		mA

Notes:
1. 100% tested at 25°C

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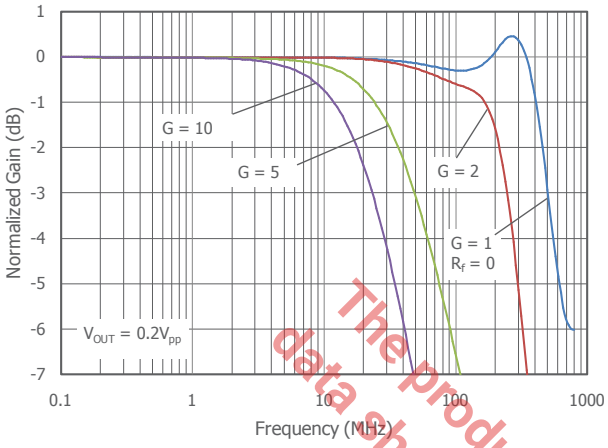
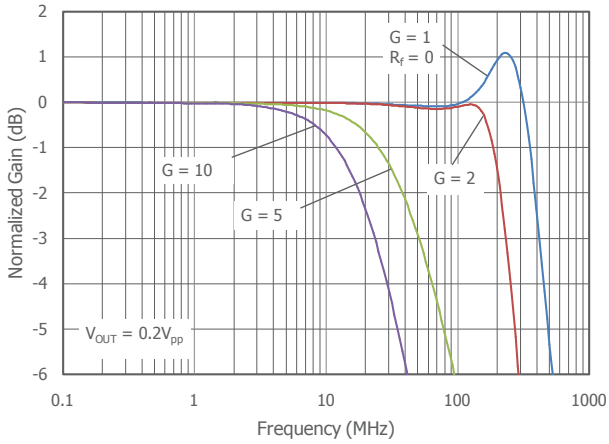
Typical Performance Characteristics

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

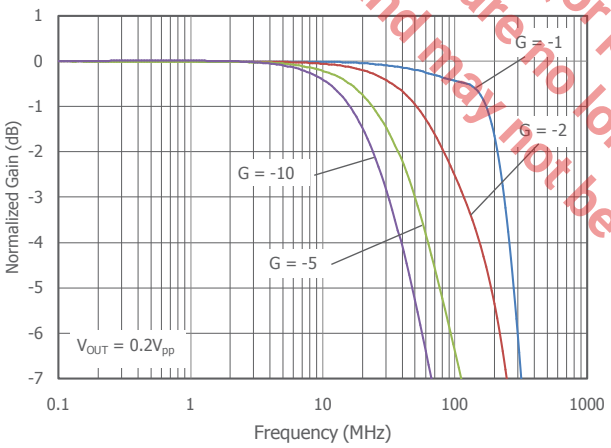
Non-Inverting Frequency Response



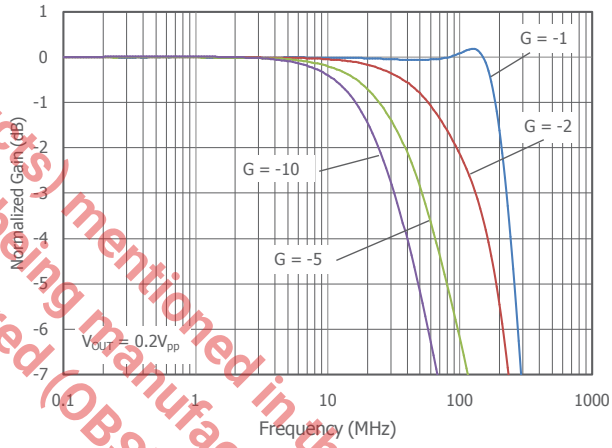
Non-Inverting Frequency Response (V_S=5V)



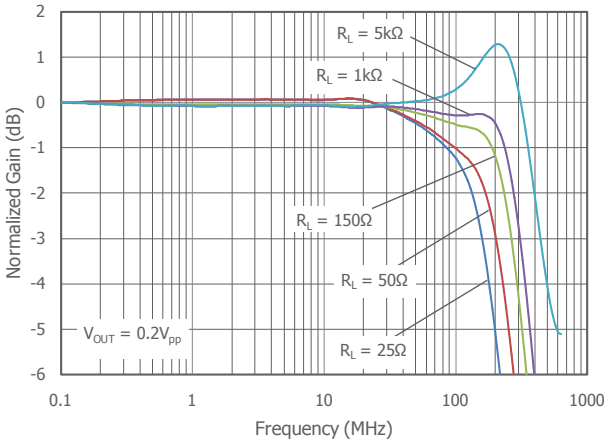
Inverting Frequency Response



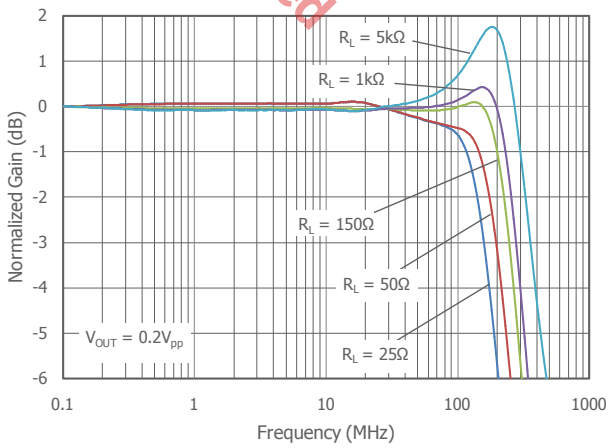
Inverting Frequency Response (V_S=5V)



Frequency Response vs. R_L



Frequency vs. R_L (V_S = 5V)



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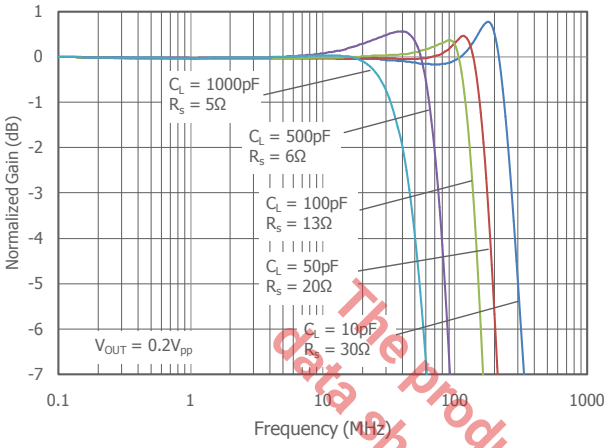
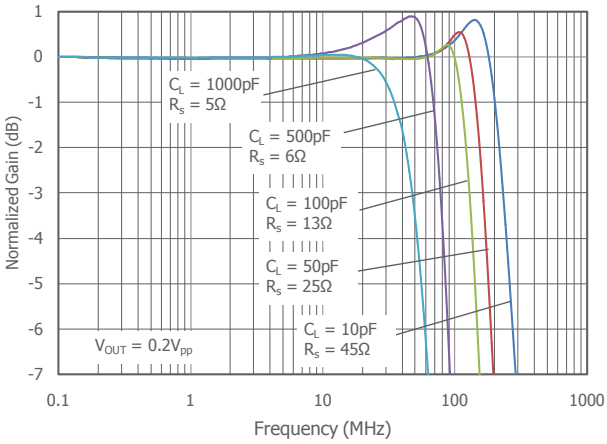
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

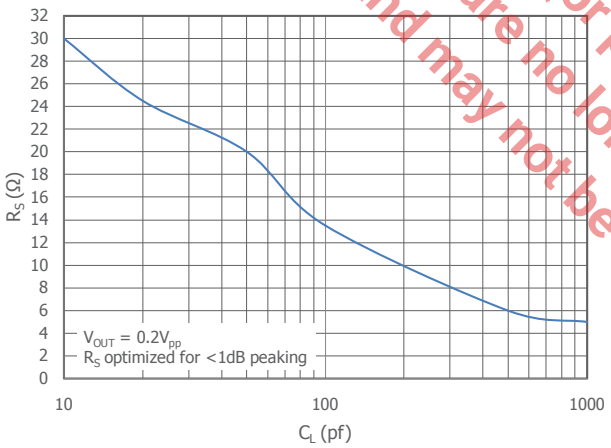
Frequency vs. C_L



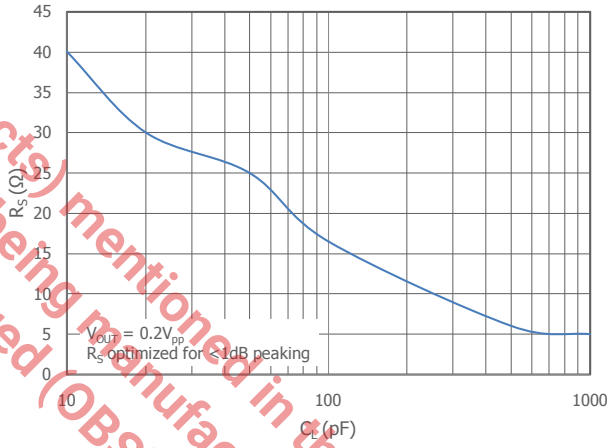
Frequency vs. C_L (V_S = 5V)



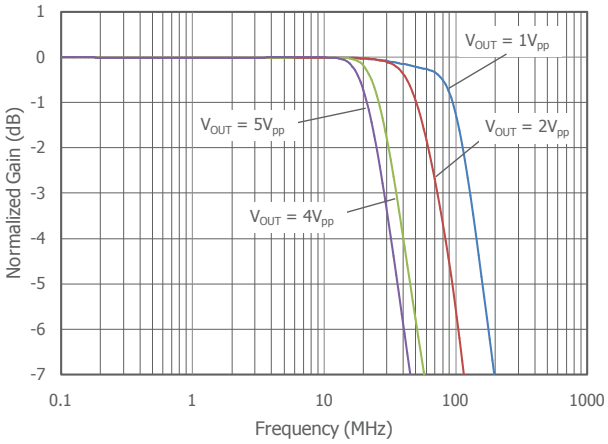
Recommended R_S vs. C_L



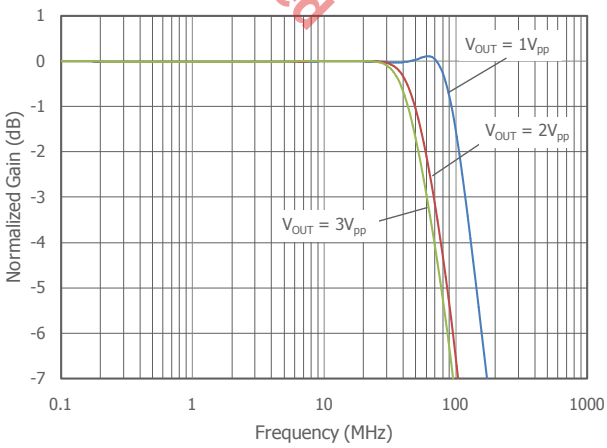
Recommended R_S vs. C_L (V_S = 5V)



Frequency Response vs. V_{OUT}



Frequency Response vs. V_{OUT} (V_S = 5V)



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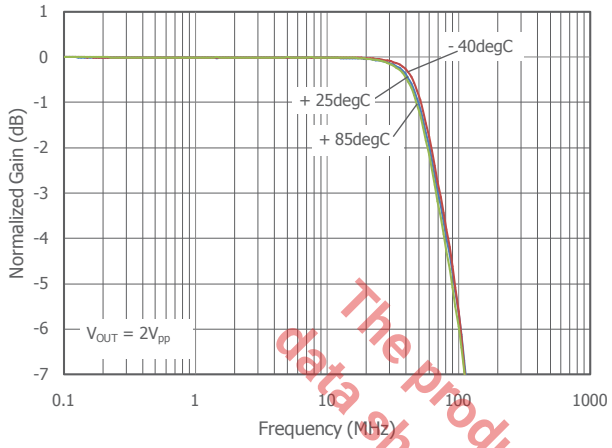
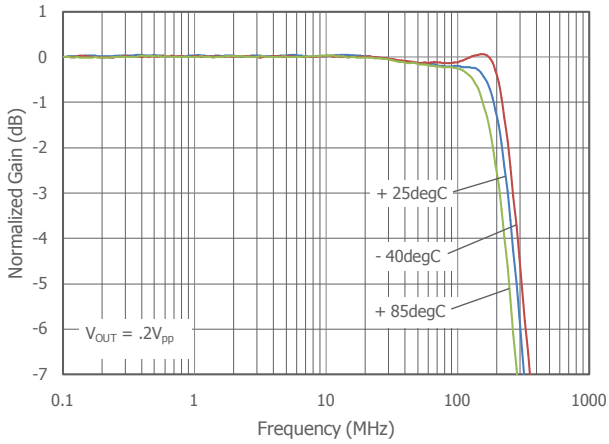
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

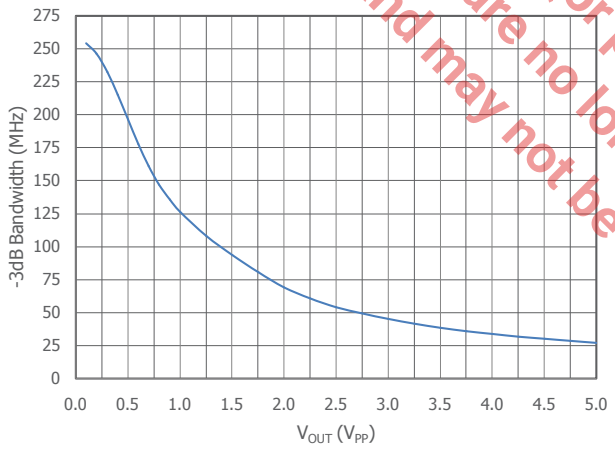
Frequency Response vs. Temperature



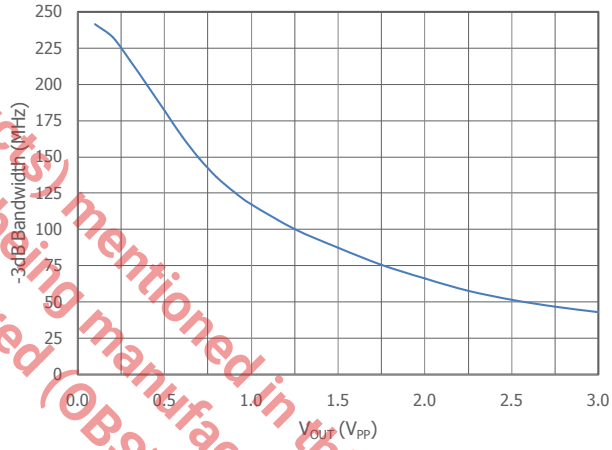
Frequency vs. Temperature (V_S = 5V)



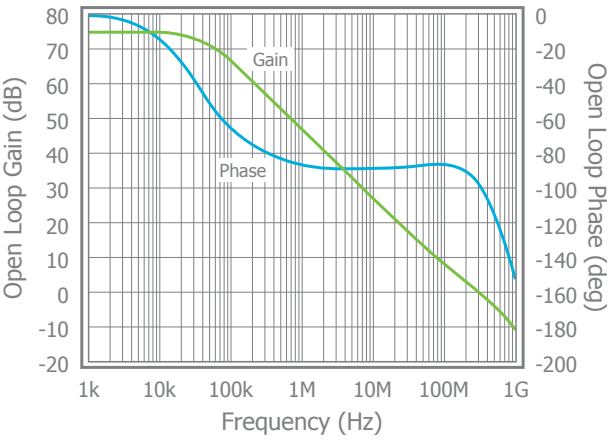
-3dB Bandwidth vs. Output Voltage



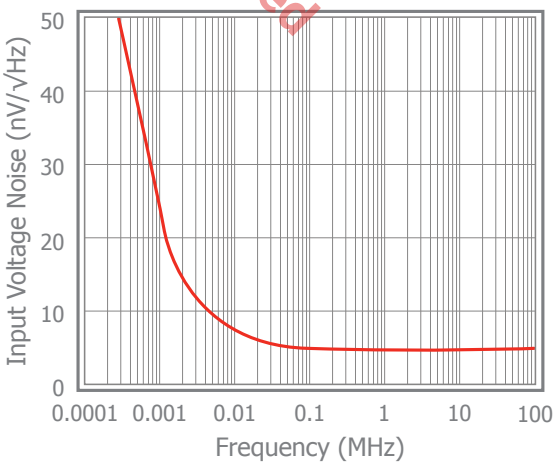
-3dB Bandwidth vs. Output Voltage (V_S=5V)



Open Loop Transimpendance Gain/Phase vs. Frequency



Input Voltage Noise



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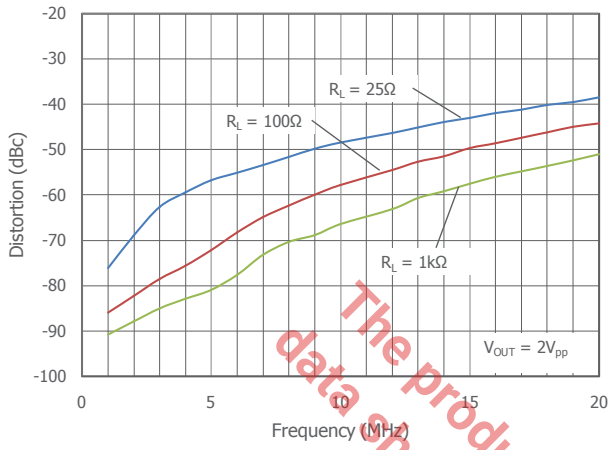
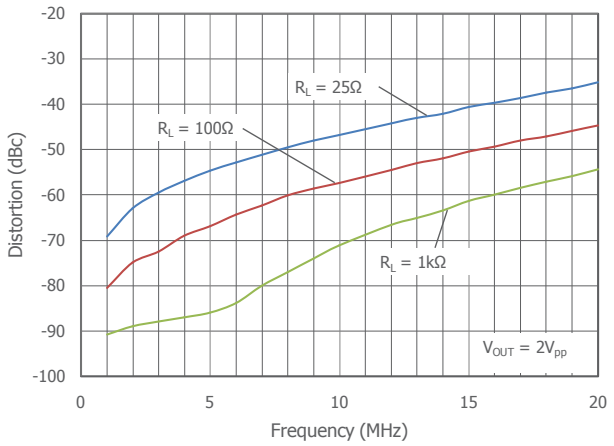
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

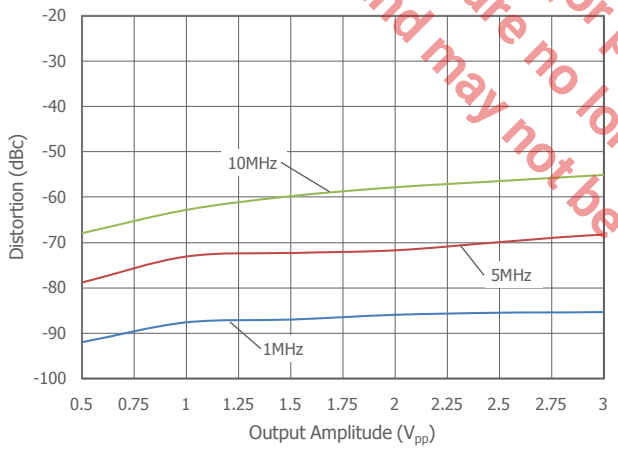
2nd Harmonic Distortion vs. R_L



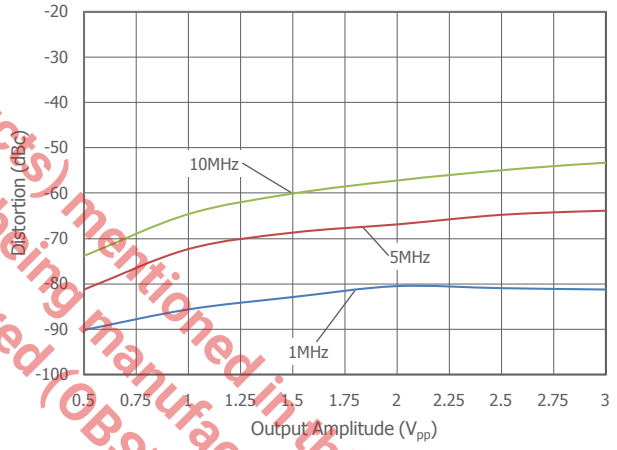
3rd Harmonic Distortion vs. R_L



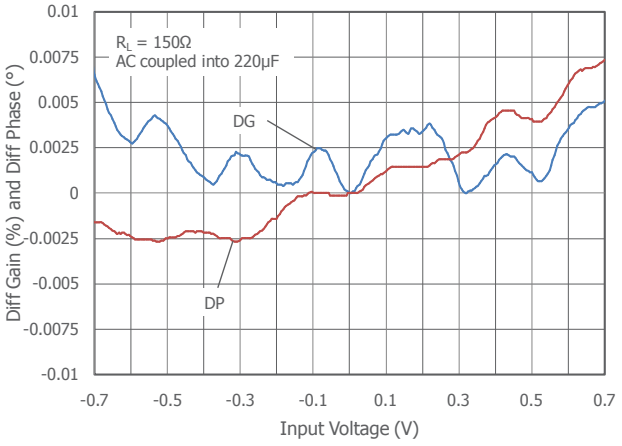
2nd Harmonic Distortion vs. V_{OUT}



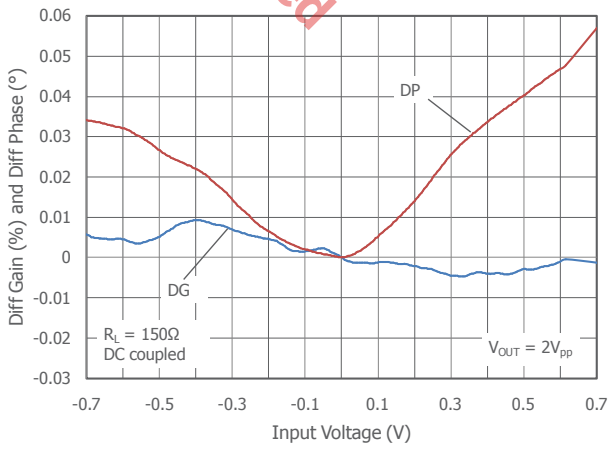
3rd Harmonic Distortion vs. V_{OUT}



Differential Gain & Phase AC Coupled



Differential Gain & Phase DC Coupled



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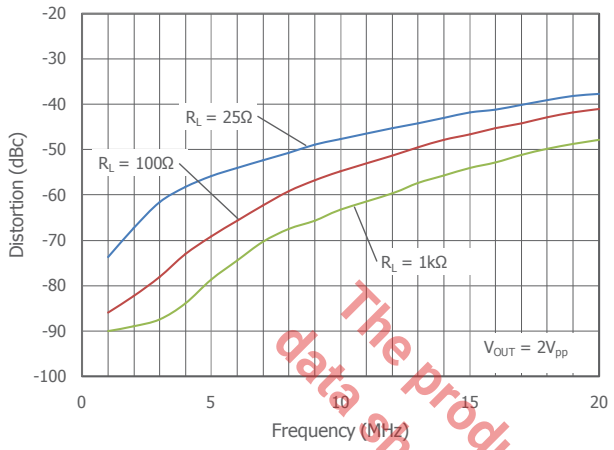
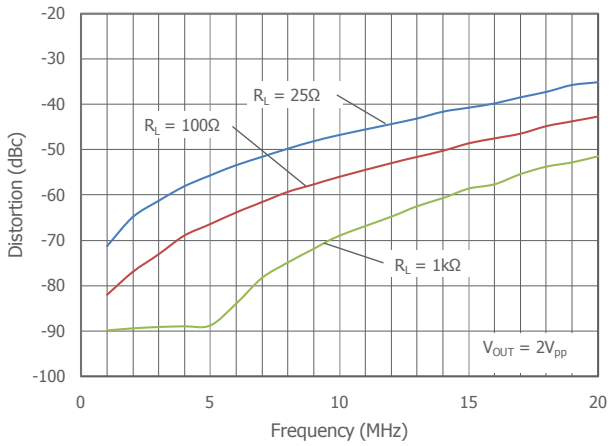
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

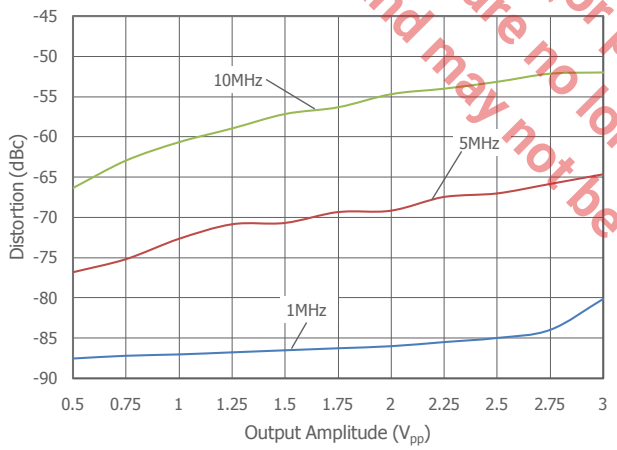
2nd Harmonic Distortion vs. R_L (V_S=5V)



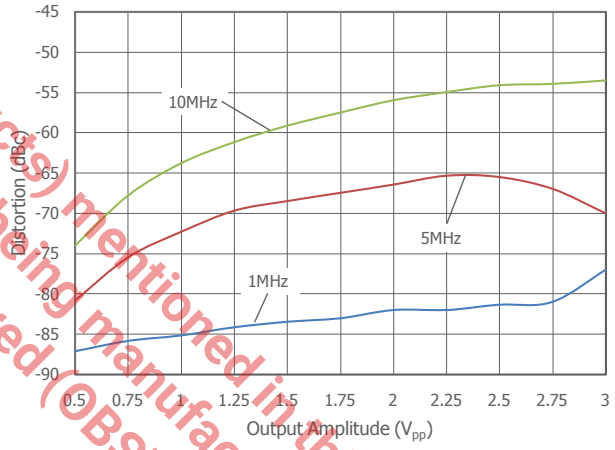
3rd Harmonic Distortion vs. R_L (V_S=5V)



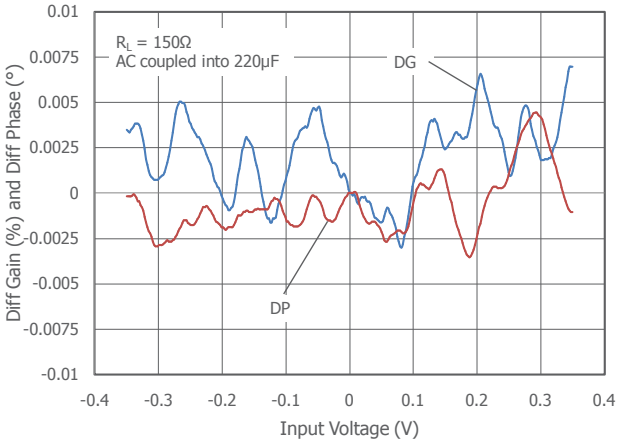
2nd Harmonic Distortion vs. V_{OUT} (V_S=5V)



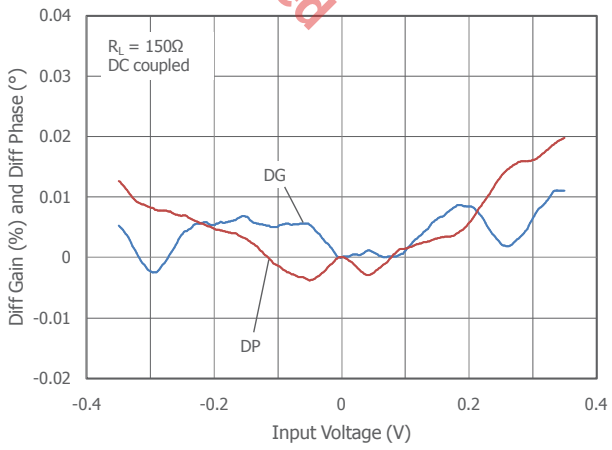
3rd Harmonic Distortion vs. V_{OUT} (V_S=5V)



Differential Gain & Phase AC Coupled (V_S=5V)



Differential Gain & Phase DC Coupled (V_S=5V)



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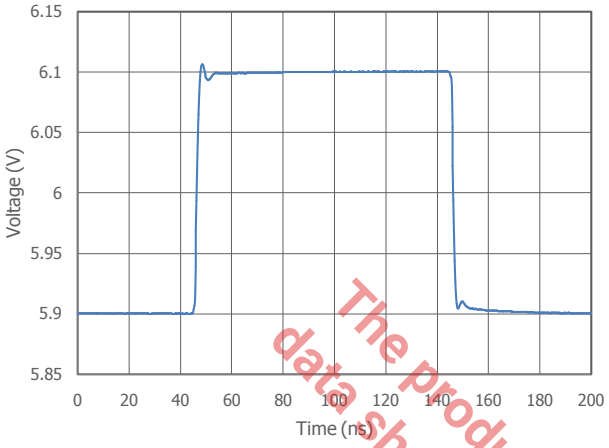
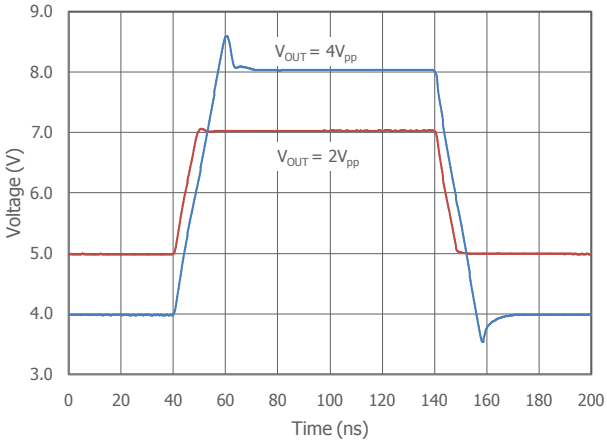
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

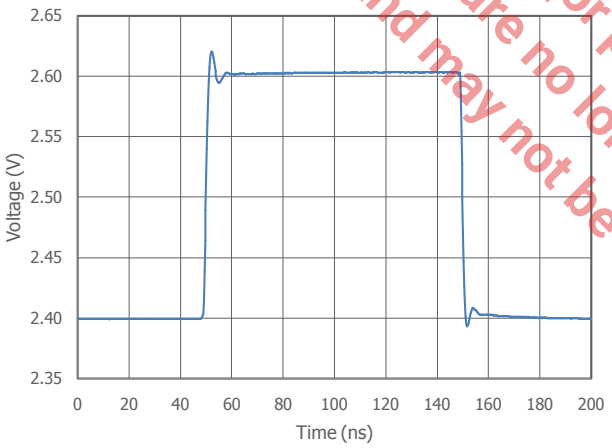
Small Signal Pulse Response



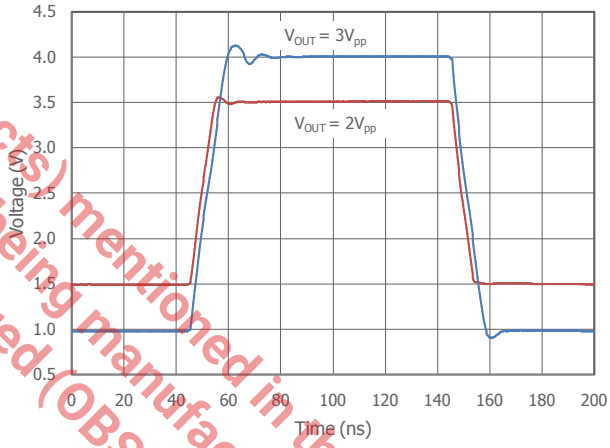
Large Signal Pulse Response



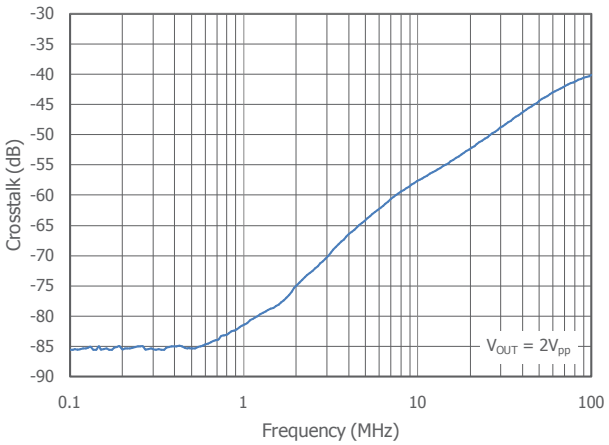
Small Signal Pulse Response (V_S=5V)



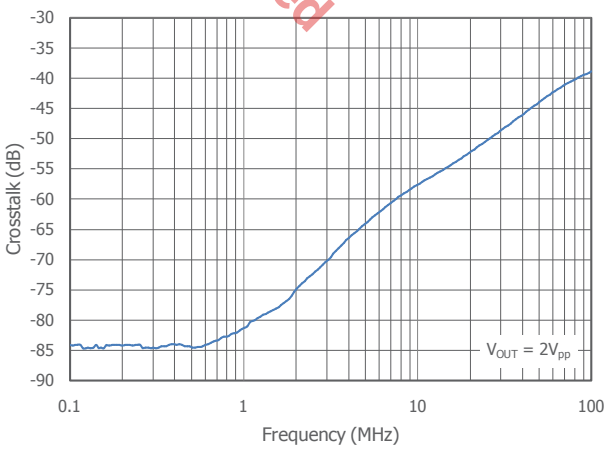
Large Signal Pulse Response (V_S=5V)



Crosstalk vs. Frequency



Crosstalk vs. Frequency (V_S=5V)



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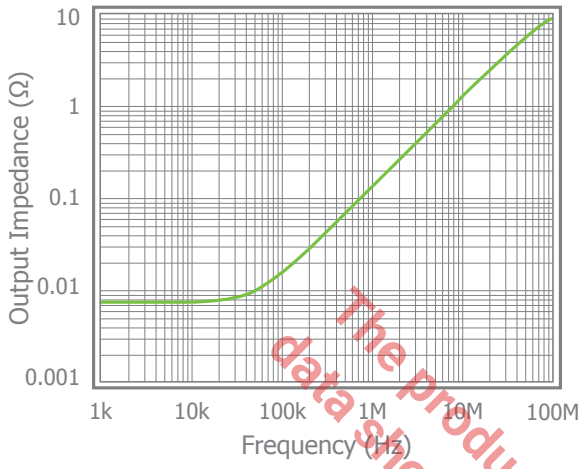
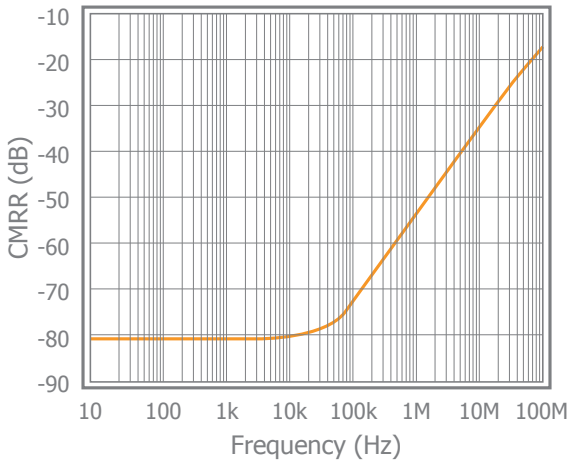
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

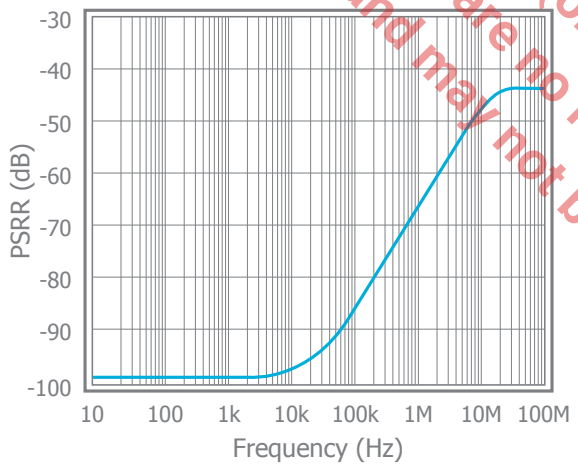
Closed Loop Output Impedance vs. Frequency



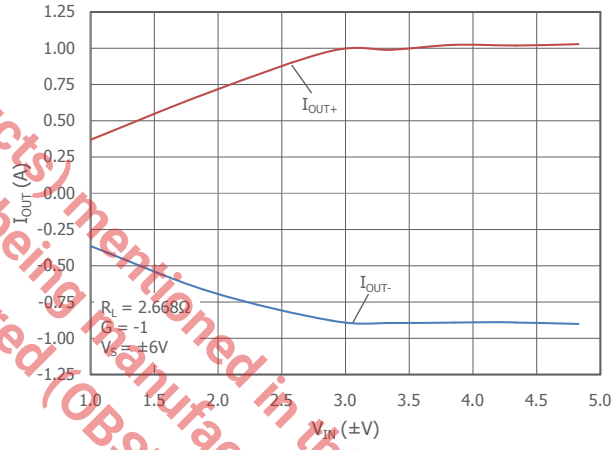
CMRR vs. Frequency



PSRR vs. Frequency



Input Voltage vs. Output Current



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Application Information

Basic Operation

Figures 1 and 2 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations.

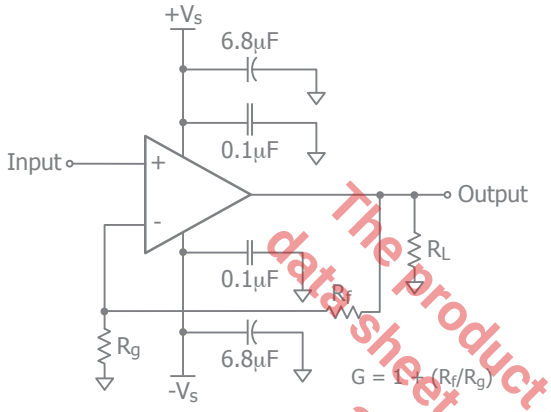

Figure 1. Typical Non-Inverting Gain Circuit

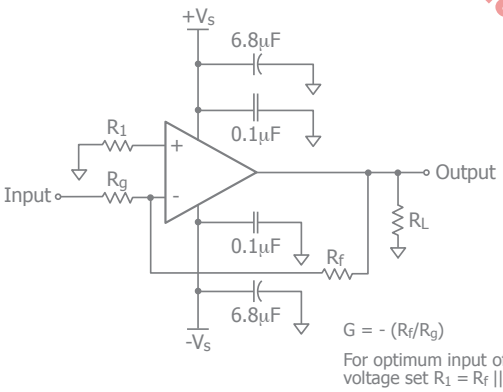

Figure 2. Typical Inverting Gain Circuit

Power Supply and Decoupling

The CLC2000 and CLC4000 can be powered with a low noise supply anywhere in the range from +5V to +13V. Ensure adequate metal connections to power pins in the PC board layout with careful attention paid to decoupling the power supply.

High quality capacitors with low equivalent series resistance (ESR) such as multilayer ceramic capacitors (MLCC) should be used to minimize supply voltage ripple and power dissipation.

Two decoupling capacitors should be placed on each power pin with connection to a local PC board ground plane. A large, usually tantalum, 10µF to 47µF capacitor is required to provide good decoupling for lower frequency signals and to provide current for fast, large signal changes at the CLC2000/CLC4000 outputs. It should be within 0.25" of the pin. A secondary smaller 0.1µF MLCC capacitor should located within 0.125" to reject higher frequency noise on the power line.

Power Dissipation

Power dissipation is an important consideration in applications with low impedance DC, coupled loads. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond its intended operating range. Calculations below relate to a single amplifier. For the CLC2000/CLC4000, all amplifiers power contribution needs to be added for the total power dissipation.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value $Theta_{JA}$ (Θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\Theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{(RMS\ supply)}$$

$$V_{supply} = V_{(S+)} - V_{(S-)}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{LOAD})_{RMS}^2) / Rload_{eff}$$

The effective load resistor will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in figure 1 would be calculated as:

$$R_L \,||\, (R_f + R_g)$$

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These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{Load}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply}. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$$

$$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / Rload_{eff}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8 Lead SOIC packages.

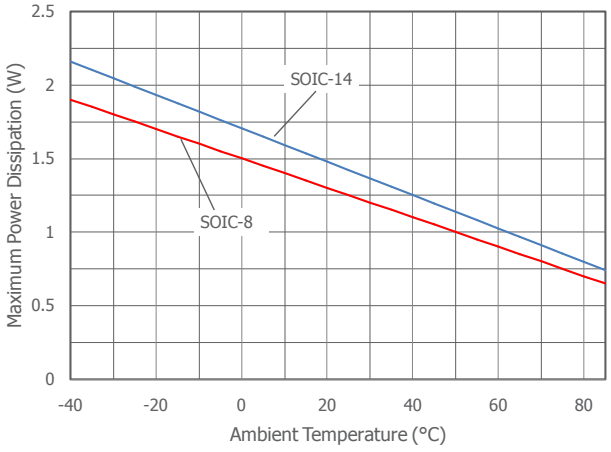

Figure 3. Maximum Power Derating

Better thermal ratings can be achieved by maximizing PC board metallization at the package pins. However, be careful of stray capacitance on the input pins.

In addition, increased airflow across the package can also help to reduce the effective Θ_{JA} of the package.

In the event of a short circuit condition, the CLC2000/CLC4000 has circuitry to limit output drive capability to ±1000mA. This will only protect against a momentary event. Extended duration under these conditions will cause junction temperatures to exceed 150°C. Due to internal metallization constraints, continuous output current should be limited to ±100mA.

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 4.

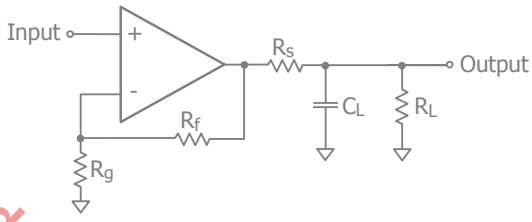

Figure 4. Addition of R_S for Driving Capacitive Loads

Table 1 provides the recommended R_S for various capacitive loads. The recommended R_S values result in <=1dB peaking in the frequency response. The Frequency Response vs. C_L plots, on page 7, illustrates the response of the CLC2000.

C_L (pF)	R_S (Ω)	-3dB BW (MHz)
10	40	275
20	24.5	250
50	20	175
100	13.5	135
500	6	75
1000	5	45

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

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Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLC2000/CLC4000 will typically recover in less than 40ns from an overdrive condition. Figure 5 shows the CLC2000 in an overdriven condition.

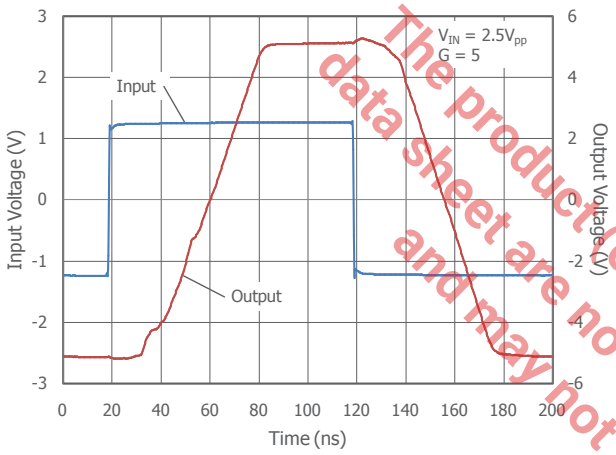

Figure 5. Overdrive Recovery

Using the CLC2000/CLC4000 as a Differential Line Driver

The combination of good large signal bandwidth and high output drive capability makes the CLC2000/CLC4000 well suited for low impedance line driver applications, such as the upstream data path for a ADSL CPE modem. The dual channel configuration of the CLC2000 provides better channel matching than a typical single channel device, resulting in better overall performance in differential applications. When configured as a differential amplifier as in figure 6, it can easily deliver the 13dBm to a standard 100Ω twisted-pair CAT3 or CAT5 cable telephone network, as required in a ADSL CPE application.

Differential circuits have several advantages over single-ended configurations. These include better rejection of common mode signals and improvement of power-supply rejection. The use of differential signaling also improves overall dynamic performance. Total harmonic distortion (THD) is reduced by the suppression of even signal harmonics and the larger signal swings allow for an improved signal to noise ratio (SNR).

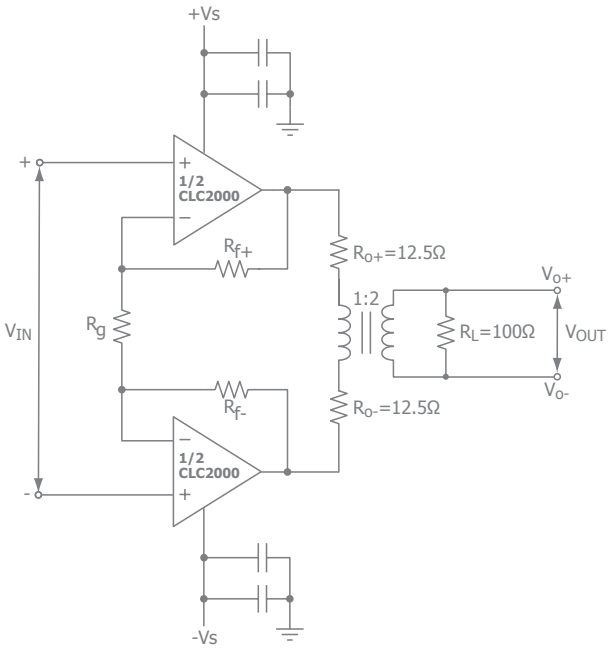

Figure 6: Typical Differential Transmission Line Driver

For any transmission requirement, the fundamental design parameters needed are the effective impedance of the transmission line, the power required at the load, and knowledge concerning the content of the transmitted signal. The basic design of such a circuit is briefly outlined below, using the ADSL parameters as a guideline.

Data transmission techniques, such as ADSL, utilize amplitude modulation techniques which are sensitive to output clipping. A signal's PEAK to RMS ratio, or Crest Factor (CF), can be used to determine the adequate peak signal levels to insure fidelity for a given signal.

For an ADSL system, the signal consists of 256 independent frequencies with varying amplitudes. This results in a noise-like signal with a crest factor of about 5.3. If the driver does not have enough swing to handle the signal peaks, clipping will occur and amplitude modulated information can be corrupted, causing degradation in the signals Bit Error Rate.

To determine the required swing, first use the specified load impedance to convert the RMS power to an RMS voltage. Then, multiply the RMS voltage by the crest factor to get the peak values. For example 13dBm, as referenced to 1mW, is ~20mW. 20mW into the 100Ω CAT5 impedance yields a RMS voltage of 1.413 VRMS . Using the ADSL crest factor of 5.3 yields ~ ±7.5V peak signals.

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Line coupling through a 1:2 transformer is used to realize these levels. Standard back termination is used to match the characteristic 100Ω impedance of the CAT5 cable. For proper power transfer, this requires an effective 1:4 impedance match of 25Ω at the inputs of the transformer. To account for the voltage drop of the impedance matching resistors, the signal levels at the output of the amplifier need to be doubled. Thus each amplifier will swing ±3.75V about a centered common mode output voltage.

In general, the CLC2000/CLC4000 can be used in any application where an economical and local hardwired connection is needed. For example, routing analog or digital video information for a in-cabin entertainment system. Networking of a local surveillance system also could be considered.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Exar has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.1µF ceramic capacitors for power supply decoupling
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation board is available to aid in the testing and layout of this device:

Evaluation Board	Products
CEB006	CLC2000
CEB018	CLC4000

Evalutaion Board Schematics

Evaluation board schematics and layouts are shown in Figures 7-9. These evaluation boards are built for dual- supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

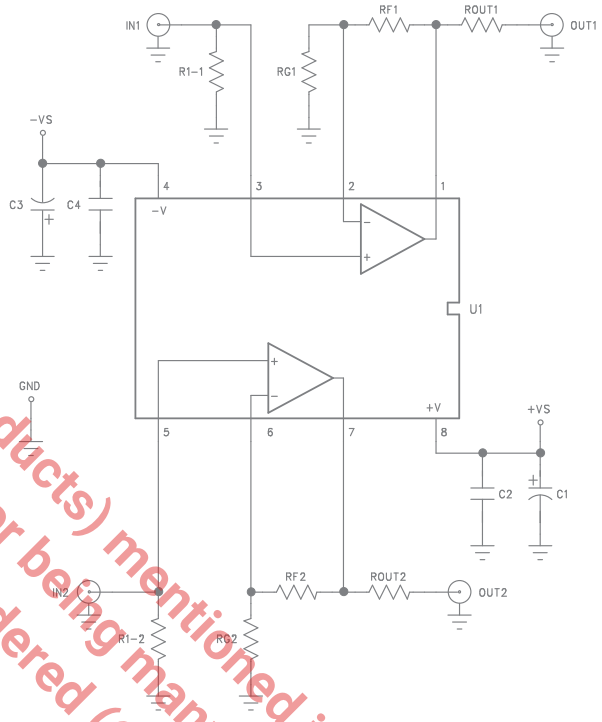

Figure 7. CEB006 Schematic

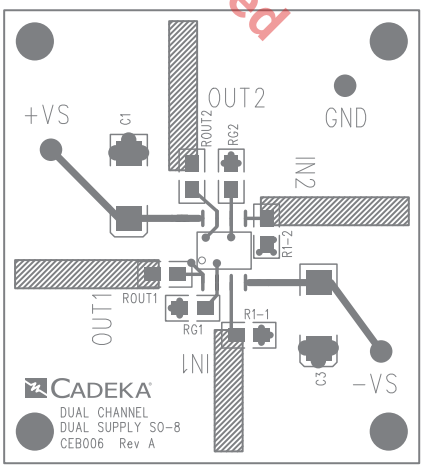

Figure 8. CEB006 Top View

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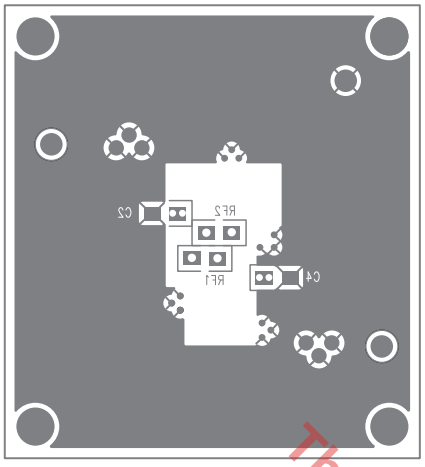

Figure 9. CEB006 Bottom View

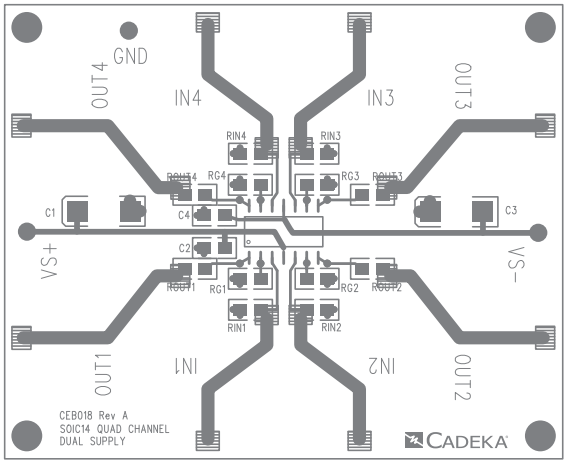

Figure 11. CEB018 Top View

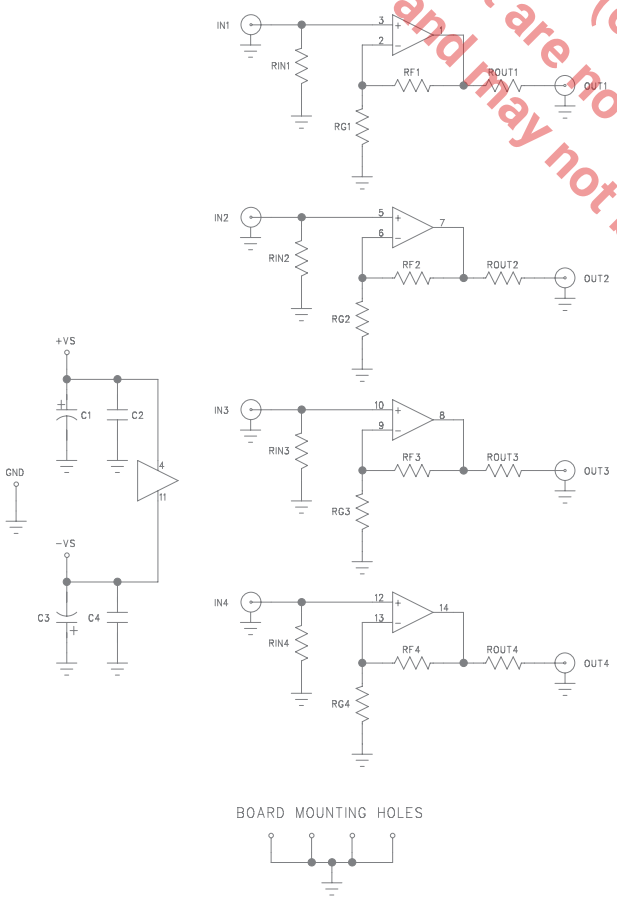

Figure 10. CEB018 Schematic

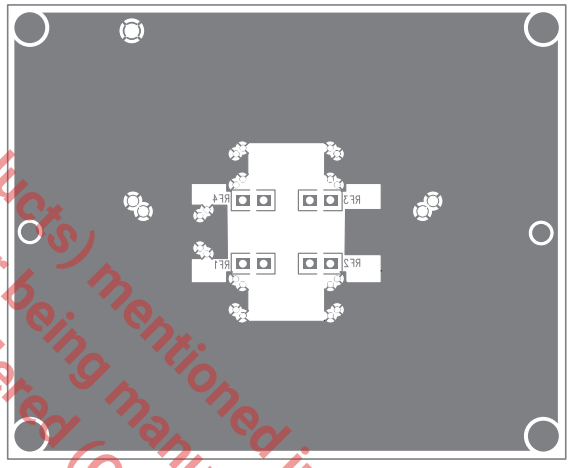

Figure 12. CEB018 Bottom View

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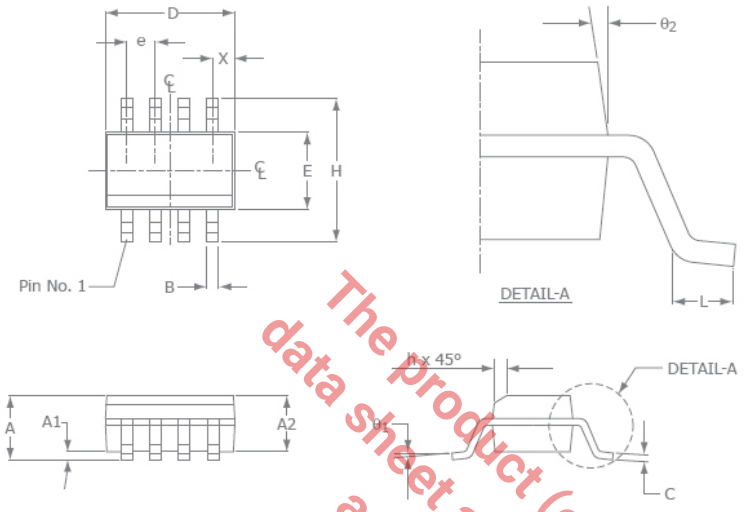
Mechanical Dimensions

SOIC-8 Package



SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.55 ref	
θ_2	7° BSC	

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

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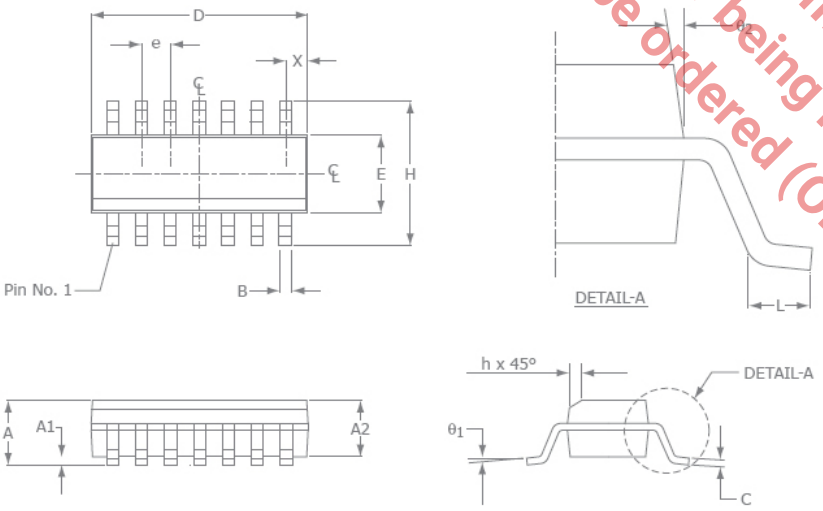
SOIC-14 Package



SOIC-14		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	8.56	8.74
E	3.84	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.51 ref	
θ_2	7° BSC	

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

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