

GENERAL DESCRIPTION

The XRA1203 is a 16-bit GPIO expander with an I²C/SMBus interface. After power-up, the XRA1203 has internal 100K ohm pull-up resistors on each I/O pin that can be individually enabled.

In addition, the GPIOs on the XRA1203 can individually be controlled and configured. As outputs, the GPIOs can be outputs that are high, low or in three-state mode. The three-state mode feature is useful for applications where the power is removed from the remote devices, but they may still be connected to the GPIO expander.

As inputs, the internal pull-up resistors can be enabled or disabled and the input polarity can be inverted. The interrupt can be programmed for different behaviors. The interrupts can be programmed to generate an interrupt on the rising edge, falling edge or on both edges. The interrupt can be cleared if the input changes back to its original state or by reading the current state of the inputs.

The XRA1203 is an enhanced version of the PCA9539 and TCA9539. The XRA1203 is pin and software compatible with the PCA9539 and TCA9539 (note: software registers are compatible to the PCA9539, but the I²C slave address is different).

The XRA1203 is available in 24-pin QFN and 24-pin TSSOP packages.

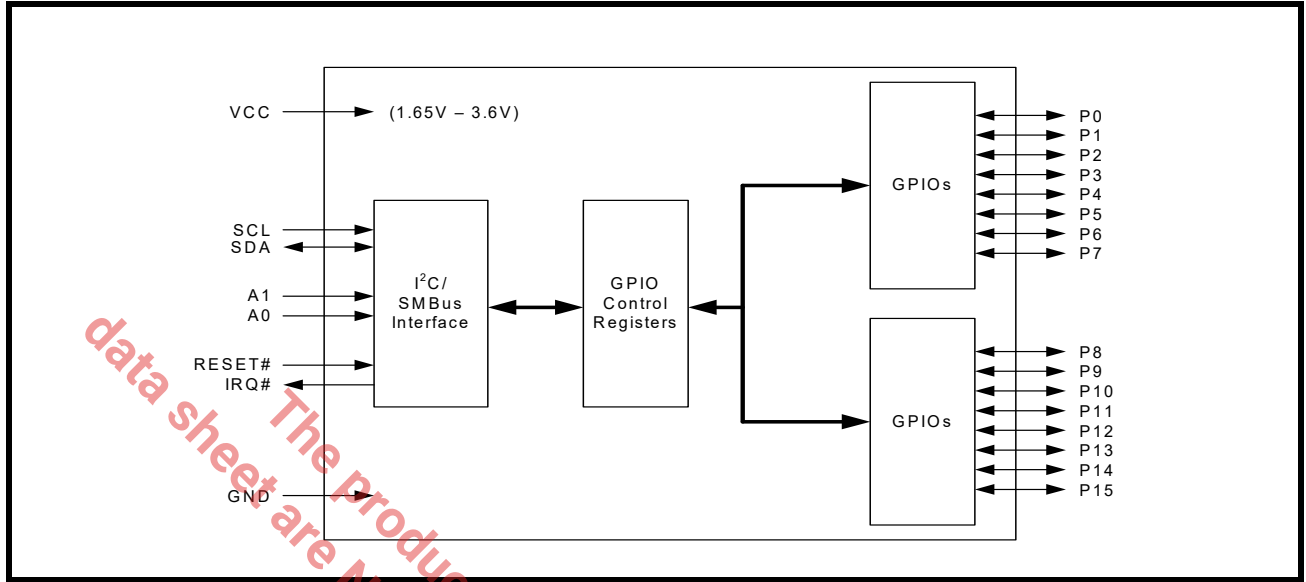
TSSOP version available, QFN version obsolete

FEATURES

- 1.65V to 3.6V operating voltage
- 16 General Purpose I/Os (GPIOs)
- 5V tolerant inputs
- Maximum stand-by current of 1uA at +1.8V
- I²C/SMBus bus interface
- I²C clock frequency up to 400kHz
- Noise filter on SDA and SCL inputs
- Up to 16 I²C Slave Addresses
- Individually programmable inputs
- Internal pull-up resistors
- Polarity inversion
- Individual interrupt enable
- Rising edge and/or Falling edge interrupt
- Input filter
- Individually programmable outputs
- Output Level Control
- Output Three-State Control
- Open-drain active low interrupt output
- Active-low reset input
- Pin and software compatible with PCA9539 and TCA9539
- 3kV HBM ESD protection per JESD22-A114F
- 200mA latch-up performance per JESD78B

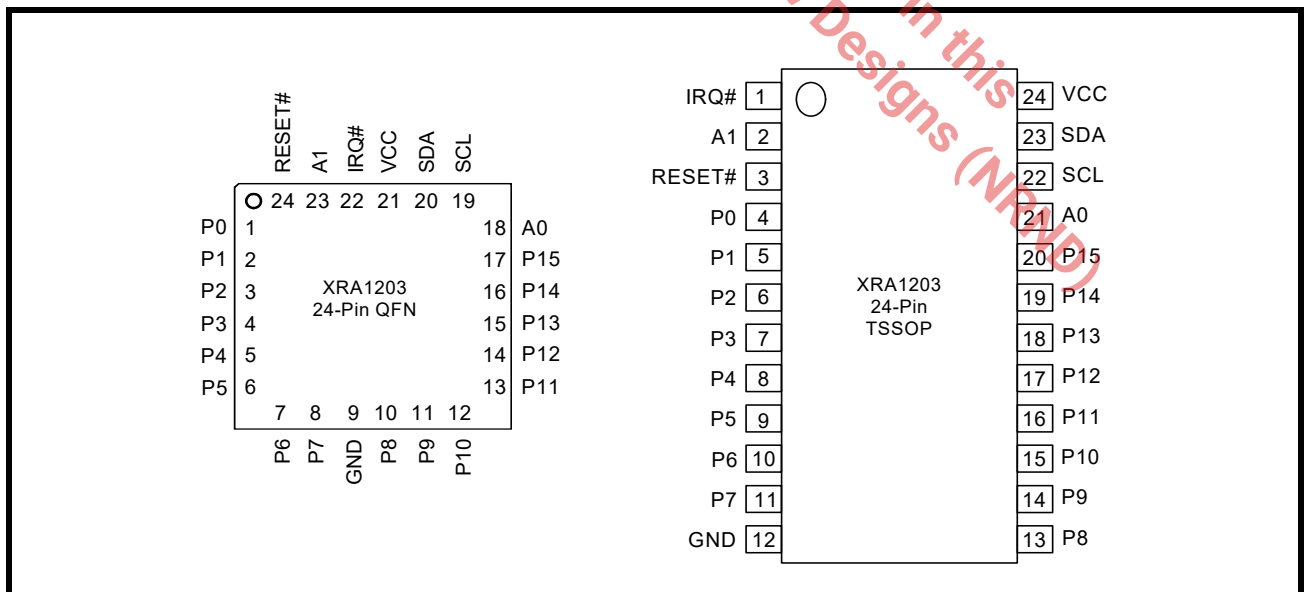
APPLICATIONS

- Personal Digital Assistants (PDA)
- Cellular Phones/Data Devices
- Battery-Operated Devices
- Global Positioning System (GPS)
- Bluetooth

FIGURE 1. XRA1203 BLOCK DIAGRAM

ORDERING INFORMATION

| PART NUMBER | NUMBER OF GPIOs | OPERATING TEMPERATURE RANGE | PACKAGE | PACKAGE METHOD | LEAD-FREE |
|-------------------|--------------------------|-----------------------------|----------|----------------|-----------|
| XRA1203IG24TR-F | 16 | -40°C to +85°C | TSSOP-24 | Tape and Reel | Yes |
| XRA1203IG24-0A-EB | XRA1203 Evaluation Board | | | | |

NOTE: For more information about part numbers, as well as the most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/XRA1203.

FIGURE 2. PIN OUT ASSIGNMENTS TSSOP-24 VERSION AVAILABLE, QFN-24 VERSION OBSOLETE


PIN DESCRIPTIONS

Pin Description **TSSOP-24 version available, QFN-24 version obsolete**

| NAME | QFN-24 PIN# | TSSOP-24 PIN# | TYPE | DESCRIPTION |
|--|--|--|---|---|
| I²C INTERFACE | | | | |
| SDA | 20 | 23 | I/O | I ² C-bus data input/output (open-drain). |
| SCL | 19 | 22 | I | I ² C-bus serial input clock. |
| IRQ# | 22 | 1 | OD | Interrupt output (open-drain, active LOW). |
| A0 A1 | 18 23 | 21 2 | I | These pins select the I ² C slave address. See Table 1 . |
| RESET# | 24 | 3 | I | Reset (active LOW) - A longer than 40 ns LOW pulse on this pin will reset the internal registers and all GPIOs will be configured as inputs. |
| GPIOs | | | | |
| P0 P1 P2 P3 P4 P5 P6 P7 | 1 2 3 4 5 6 7 8 | 4 5 6 7 8 9 10 11 | I/O I/O I/O I/O I/O I/O I/O | General purpose I/Os P0-P7. All GPIOs are configured as inputs upon power-up or after a reset. |
| P8 P9 P10 P11 P12 P13 P14 P15 | 10 11 12 13 14 15 16 17 | 13 14 15 16 17 18 19 20 | I/O I/O I/O I/O I/O I/O I/O | General purpose I/O P8-P15. All GPIOs are configured as inputs upon power-up or after a reset. |
| ANCILLARY SIGNALS | | | | |
| VCC | 21 | 24 | Pwr | 1.65V to 3.6V VCC supply voltage. |
| GND | 9 | 12 | Pwr | Power supply common, ground. |
| GND | Center Pad | - | Pwr | The exposed pad at the bottom surface of the package is designed for thermal performance. Use of a center pad on the PCB is strongly recommended for thermal conductivity as well as to provide mechanical stability of the package on the PCB. The center pad is recommended to be solder masked defined with opening size less than or equal to the exposed thermal pad on the package bottom to prevent solder bridging to the outer leads of the device. Thermal vias must be connected to GND plane as the thermal pad of package is at GND potential. |

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

1.0 FUNCTIONAL DESCRIPTIONS

1.1 I²C-bus Interface

The I²C-bus interface is compliant with the Standard-mode and Fast-mode I²C-bus specifications. The I²C-bus interface consists of two lines: serial data (SDA) and serial clock (SCL). In the Standard-mode, the serial clock and serial data can go up to 100 kbps and in the Fast-mode, the serial clock and serial data can go up to 400 kbps.

The first byte sent by an I²C-bus master contains a start bit (SDA transition from HIGH to LOW when SCL is HIGH), 7-bit slave address and whether it is a read or write transaction. The next byte is the sub-address that contains the address of the register to access. The XRA1203 responds to each write with an acknowledge (SDA driven LOW by XRA1203 for one clock cycle when SCL is HIGH). The last byte sent by an I²C-bus master contains a stop bit (SDA transition from LOW to HIGH when SCL is HIGH). See Figures 3 - 5 below. For complete details, see the I²C-bus specifications.

FIGURE 3. I²C START AND STOP CONDITIONS

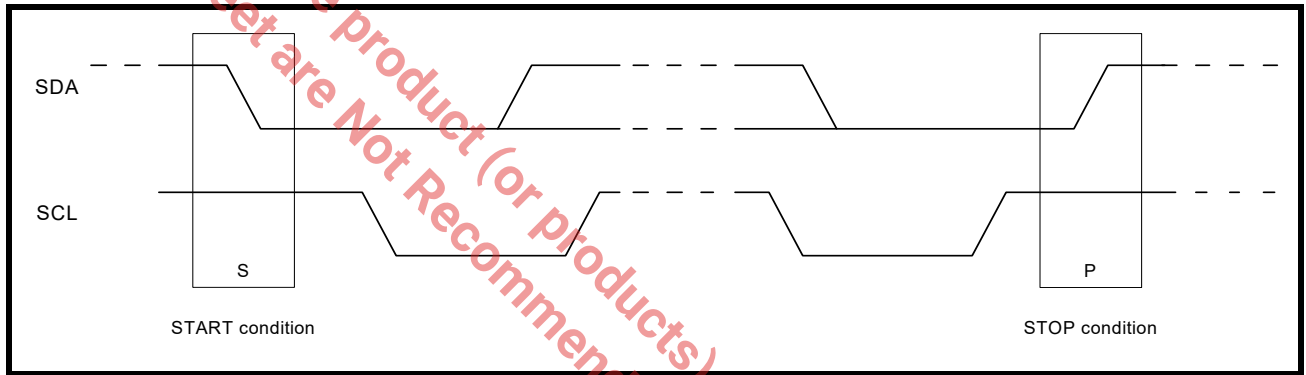


FIGURE 4. MASTER WRITES TO SLAVE

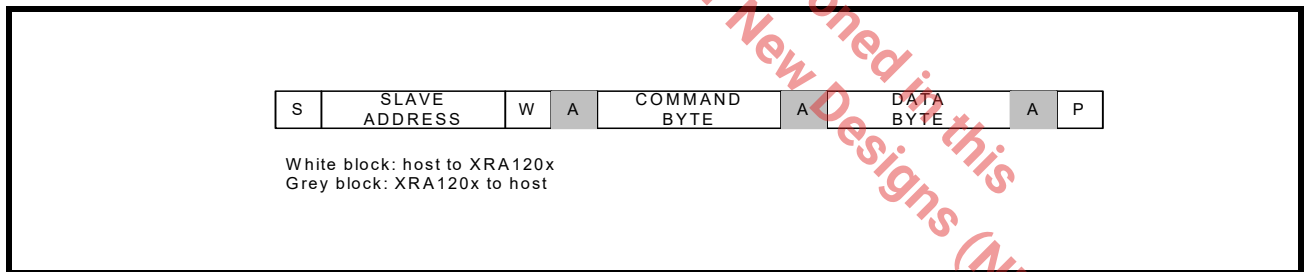
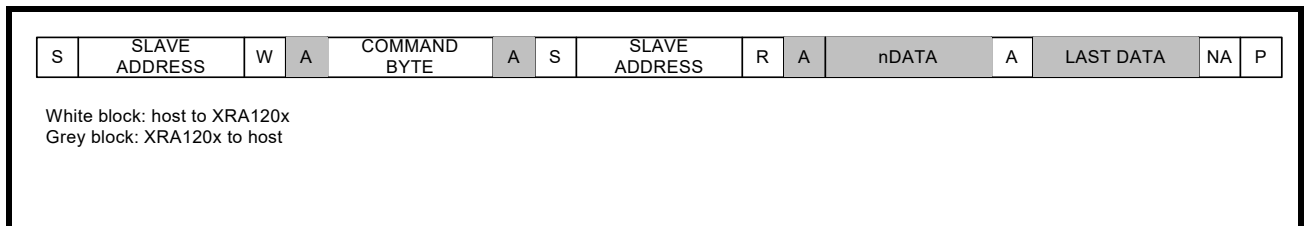


FIGURE 5. MASTER READS FROM SLAVE



1.1.1 I²C-bus Addressing

There could be many devices on the I²C-bus. To distinguish itself from the other devices on the I²C-bus, the XRA1203 has up to 16 I²C slave addresses using the A1-A0 address lines. Table 1 below shows the different addresses that can be selected.

TABLE 1: I²C ADDRESS MAP

| A1 | A0 | I ² C ADDRESS |
|-----|-----|--------------------------|
| SCL | GND | 0x20 (0010 000X) |
| SCL | VCC | 0x22 (0010 001X) |
| SDA | GND | 0x24 (0010 010X) |
| SDA | VCC | 0x26 (0010 011X) |
| SCL | SCL | 0x30 (0011 000X) |
| SCL | SDA | 0x32 (0011 001X) |
| SDA | SCL | 0x34 (0011 010X) |
| SDA | SDA | 0x36 (0011 011X) |
| GND | GND | 0x40 (0100 000X) |
| GND | VCC | 0x42 (0100 001X) |
| VCC | GND | 0x44 (0100 010X) |
| VCC | VCC | 0x46 (0100 011X) |
| GND | SCL | 0x50 (0101 000X) |
| GND | SDA | 0x52 (0101 001X) |
| VCC | SCL | 0x54 (0101 010X) |
| VCC | SDA | 0x56 (0101 011X) |

1.1.2 I²C Read and Write

A read or write transaction is determined by bit-0 of the slave address. If bit-0 is '0', then it is a write transaction. If bit-0 is '1', then it is a read transaction.

1.1.3 I²C Command Byte

An I²C command byte is sent by the I²C master following the slave address. The command byte indicates the address offset of the register that will be accessed. **Table 2** below lists the command bytes for each register.

TABLE 2: I²C COMMAND BYTE (REGISTER ADDRESS)

| COMMAND BYTE | REGISTER NAME DESCRIPTION | READ/WRITE | DEFAULT VALUES |
|--------------|--|------------|----------------|
| 0x00 | GSR1 - GPIO State for P0-P7 | Read-Only | 0xXX |
| 0x01 | GSR2 - GPIO State for P8-P15 | Read-Only | 0xXX |
| 0x02 | OCR1 - Output Control for P0-P7 | Read/Write | 0xFF |
| 0x03 | OCR2 - Output Control for P8-P15 | Read/Write | 0xFF |
| 0x04 | PIR1 - Input Polarity Inversion for P0-P7 | Read/Write | 0x00 |
| 0x05 | PIR2 - Input Polarity Inversion for P8-P15 | Read/Write | 0x00 |
| 0x06 | GCR1 - GPIO Configuration for P0-P7 | Read/Write | 0xFF |
| 0x07 | GCR2 - GPIO Configuration for P8-P15 | Read/Write | 0xFF |
| 0x08 | PUR1 - Input Internal Pull-up Resistor Enable/Disable for P0-P7 | Read/Write | 0x00 |
| 0x09 | PUR2 - Input Internal Pull-up Resistor Enable/Disable for P8-P15 | Read/Write | 0x00 |
| 0x0A | IER1 - Input Interrupt Enable for P0-P7 | Read/Write | 0x00 |
| 0x0B | IER2 - Input Interrupt Enable for P8-P15 | Read/Write | 0x00 |
| 0x0C | TSCR1 - Output Three-State Control for P0-P7 | Read/Write | 0x00 |
| 0x0D | TSCR2 - Output Three-State Control for P8-P15 | Read/Write | 0x00 |
| 0x0E | ISR1 - Input Interrupt Status for P0-P7 | Read | 0x00 |
| 0x0F | ISR2 - Input Interrupt Status for P8-P15 | Read | 0x00 |
| 0x10 | REIR1 - Input Rising Edge Interrupt Enable for P0-P7 | Read/Write | 0x00 |
| 0x11 | REIR2 - Input Rising Edge Interrupt Enable for P8-P15 | Read/Write | 0x00 |
| 0x12 | FEIR1 - Input Falling Edge Interrupt Enable for P0-P7 | Read/Write | 0x00 |
| 0x13 | FEIR2 - Input Falling Edge Interrupt Enable for P8-P15 | Read/Write | 0x00 |
| 0x14 | IFR1 - Input Filter Enable/Disable for P0-P7 | Read/Write | 0xFF |
| 0x15 | IFR2 - Input Filter Enable/Disable for P8-P15 | Read/Write | 0xFF |

1.2 Interrupts

The table below summarizes the interrupt behavior of the different register settings for the XRA1203.

TABLE 3: INTERRUPT GENERATION AND CLEARING

| GCR BIT | IER BIT | REIR BIT | FEIR BIT | IFR BIT | INTERRUPT GENERATED BY: | INTERRUPT CLEARED BY: |
|---------|---------|----------|----------|---------|---|--|
| 1 | 0 | X | X | X | No interrupts enabled (default) | N/A |
| 1 | 1 | 0 | 0 | 0 | A rising or falling edge on the input | Reading the GSR register or if the input changes back to its previous state (state of input during last read to GSR) |
| | | | | 1 | A rising or falling edge on the input and remains in the new state for more than 1075ns | |
| 1 | 1 | 1 | 0 | 0 | A rising edge on the input | Reading the GSR register |
| | | | | 1 | A rising edge on the input and remains high for more than 1075ns | |
| 1 | 1 | 0 | 1 | 0 | A falling edge on the input | Reading the GSR register |
| | | | | 1 | A falling edge on the input and remains low for more than 1075ns | |
| 1 | 1 | 1 | 1 | 0 | A rising or falling edge on the input | Reading the GSR register |
| | | | | 1 | A rising or falling edge on the input and remains in the new state for more than 1075ns | |
| 0 | x | x | x | x | No interrupts in output mode | N/A |

2.0 REGISTER DESCRIPTION

2.1 GPIO State Register 1 (GSR1) - Read-Only

The status of P7 - P0 can be read via this register. A read will show the current state of these pins (or the inverted state of these pins if enabled via the PIR Register). Reading this register will clear an input interrupt (see Table 3 for complete details). Reading this register will also return the last value written to the OCR register for any pins that are configured as outputs (ie. this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.2 GPIO State Register 2 (GSR2) - Read-Only

The status of P15 - P8 can be read via this register. A read will show the current state of these pins (or the inverted state of these pins if enabled via the PIR Register). Reading this register will clear an input interrupt (see Table 3 for complete details). Reading this register will also return the last value written to the OCR register for any pins that are configured as outputs (ie. this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.3 Output Control Register 1 (OCR1) - Read/Write

When P7 - P0 are defined as outputs, they can be controlled by writing to this register. Reading this register will return the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.4 Output Control Register 2 (OCR2) - Read/Write

When P15 - P8 are defined as outputs, they can be controlled by writing to this register. Reading this register will return the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.5 Input Polarity Inversion Register 1 (PIR1) - Read/Write

When P7 - P0 are defined as inputs, this register inverts the polarity of the input value read from the Input Port Register. If the corresponding bit in this register is set to '1', the value of this bit in the GSR Register will be the inverted value of the input pin. If the corresponding bit in this register is set to '0', the value of this bit in the GSR Register will be the actual value of the input pin. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.6 Input Polarity Inversion Register 2 (PIR2) - Read/Write

When P15 - P8 are defined as inputs, this register inverts the polarity of the input value read from the Input Port Register. If the corresponding bit in this register is set to '1', the value of this bit in the GSR Register will be the inverted value of the input pin. If the corresponding bit in this register is set to '0', the value of this bit in the GSR Register will be the actual value of the input pin. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.7 GPIO Configuration Register 1 (GCR1) - Read/Write

This register configures the GPIOs as inputs or outputs. After power-up or after reset, the GPIOs are inputs. Setting these bits to '0' will enable the GPIOs as outputs. Setting these bits to '1' will enable the GPIOs as inputs. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.8 GPIO Configuration Register 2 (GCR2) - Read/Write

This register configures the GPIOs as inputs or outputs. After power-up or after reset, the GPIOs are inputs. Setting these bits to '0' will enable the GPIOs as outputs. Setting these bits to '1' will enable the GPIOs as inputs. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.9 Input Internal Pull-up Enable/Disable Register 1 (PUR1) - Read/Write

This register enables/disables the internal pull-up resistors for an input. After power-up or after reset, the internal pull-up resistors are disabled by default. Writing a '1' to these bits will enable the internal pull-up resistors. Writing a '0' to these bits will disable the internal pull-up resistors. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.10 Input Internal Pull-up Enable/Disable Register 2 (PUR2) - Read/Write

This register enables/disables the internal pull-up resistors for an input. After power-up or after reset, the internal pull-up resistors are disabled by default. Writing a '1' to these bits will enable the internal pull-up resistors. Writing a '0' to these bits will disable the internal pull-up resistors. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.11 Input Interrupt Enable Register 1 (IER1) - Read/Write

This register enables/disables the interrupts for an input. After power-up or after reset, the interrupts are disabled. Writing a '1' to these bits will enable the interrupt for the corresponding input pins. See [Table 3](#) for complete details of the interrupt behavior for various register settings. No interrupts are generated for outputs when GCR bit is 0. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.12 Input Interrupt Enable Register 2 (IER2) - Read/Write

This register enables/disables the interrupts for an input. After power-up or after reset, the interrupts are disabled. Writing a '1' to these bits will enable the interrupt for the corresponding input pins. See [Table 3](#) for complete details of the interrupt behavior for various register settings. No interrupts are generated for outputs when GCR bit is 0. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.13 Output Three-State Control Register 1 (TSCR1) - Read/Write

This register can enable/disable the three-state mode of an output. Writing a '1' to these bits will enable the three-state mode for the corresponding output pins. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.14 Output Three-State Control Register 2 (TSCR2) - Read/Write

This register can enable/disable the three-state mode of an output. Writing a '1' to these bits will enable the three-state mode for the corresponding output pins. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.15 Input Interrupt Status Register 1 (ISR1) - Read-Only

This register reports the input pins that have generated an interrupt. See [Table 3](#) for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.16 Input Interrupt Status Register 2 (ISR2) - Read-Only

This register reports the input pins that have generated an interrupt. See [Table 3](#) for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.17 Input Rising Edge Interrupt Enable Register 1 (REIR1) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the rising edge. See [Table 3](#) for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.18 Input Rising Edge Interrupt Enable Register 2 (REIR2) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the rising edge. See [Table 3](#) for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.19 Input Falling Edge Interrupt Enable Register 1 (FEIR1) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the falling edge. Writing a '1' to these bits will make that input generate an interrupt on the rising edge only. See [Table 3](#) for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.20 Input Falling Edge Interrupt Enable Register 2 (FEIR2) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the falling edge. Writing a '1' to these bits will make that input generate an interrupt on the rising edge only. See [Table 3](#) for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.21 Input Filter Enable Register 1 (IFR1) - Read/Write

By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns will generate an interrupt (if enabled). Pulses that are less than 225ns will be filtered and will not generate an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a '0' to these bits will disable the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs will generate an interrupt (if enabled). See [Table 3](#) for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.22 Input Filter Enable Register 2 (IFR2) - Read/Write

By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns will generate an interrupt (if enabled). Pulses that are less than 225ns will be filtered and will not generate an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a '0' to these bits will disable the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs will generate an interrupt (if enabled). See [Table 3](#) for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

ABSOLUTE MAXIMUM RATINGS

| | |
|--|----------------|
| Power supply voltage | 3.6 Volts |
| Supply current | 160 mA |
| Ground current | 200 mA |
| External current limit of each GPIO | 25 mA |
| Total current limit for GPIO[15:8] and GPIO[7:0] | 100 mA |
| Total current limit for GPIO[15:0] | 200 mA |
| Total supply current sourced by all GPIOs | 160 mA |
| Operating Temperature | -40° to +85°C |
| Storage Temperature | -65° to +150°C |
| Power Dissipation | 200 mW |

TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

| | |
|-------------------------------|--------------------------------------|
| Thermal Resistance (24-QFN) | theta-ja = 38°C/W, theta-jc = 26°C/W |
| Thermal Resistance (24-TSSOP) | theta-ja = 84°C/W, theta-jc = 16°C/W |

TSSOP-24 version available, QFN-24 version obsolete

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA = -40° TO +85°C, VCC IS 1.65V TO 3.6V

| SYMBOL | PARAMETER | LIMITS 1.8V ± 10% | | LIMITS 2.5V ± 10% | | LIMITS 3.3V ± 10% | | UNITS | CONDITIONS |
|---------------------|----------------------------|----------------------|--------|----------------------|--------|----------------------|--------|-------------|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| V _{IL} | Input Low Voltage | -0.3 | 0.3VCC | -0.3 | 0.3VCC | -0.3 | 0.3VCC | V | Note 1 |
| V _{IL} | Input Low Voltage | -0.3 | 0.2 | -0.3 | 0.5 | -0.3 | 0.8 | V | Note 2 |
| V _{IH} | Input High Voltage | 1.3 | VCC | 1.8 | VCC | 2.3 | VCC | V | Note 1 |
| V _{IH} | Input High Voltage | 1.4 | 5.5 | 1.8 | 5.5 | 2.0 | 5.5 | V | Note 2 |
| V _{OL} | Output Low Voltage | | 0.4 | | 0.4 | | 0.4 | V V V | I _{OL} = 3 mA I _{OL} = 3 mA I _{OL} = 3 mA Note 3 |
| V _{OL} | Output Low Voltage | | 0.5 | | 0.5 | | 0.5 | V | I _{OL} = 8 mA Note 4 |
| V _{OL} | Output Low Voltage | | 0.4 | | 0.4 | | 0.4 | V V V | I _{OL} = 6 mA I _{OL} = 4 mA I _{OL} = 1.5 mA Note 5 |
| V _{OH} | Output High Voltage | 1.2 | | 1.8 | | 2.6 | | V V V | I _{OH} = -8 mA I _{OH} = -8 mA I _{OH} = -8 mA Note 4 |
| I _{IL} | Input Low Leakage Current | | ±10 | | ±10 | | ±10 | uA | |
| I _{IH} | Input High Leakage Current | | ±10 | | ±10 | | ±10 | uA | |
| C _{IN} | Input Pin Capacitance | | 5 | | 5 | | 5 | pF | |
| I _{CC} | Power Supply Current | | 50 | | 100 | | 200 | uA | Test 1 |
| I _{CC} | Power Supply Current | | 150 | | 250 | | 500 | uA | Test 2 |
| I _{CCS} | Standby Current | | 1 | | 2 | | 5 | uA | Test 3 |
| R _{GPIO} | GPIO pull-up resistance | 60 | 140 | 60 | 140 | 60 | 140 | kΩ | 100kΩ ± 40% |
| R _{RESET#} | Reset# pull-up resistance | 35 | 85 | 35 | 85 | 35 | 85 | kΩ | 60kΩ ± 40% |

NOTES:

1. For I²C input signals (SDA, SCL);
2. For GPIOs, A0, A1 and A2 signals;
3. For I²C output signal SDA;
4. For GPIOs;
5. For IRQ# signal;

Test 1: SCL frequency is 400 KHz with internal pull-ups disabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

Test 2: SCL frequency is 400 KHz with internal pull-ups enabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

Test 3: All inputs are steady at VCC or GND to minimize standby current. If internal pull-up is enabled, input voltage level should be the same as VCC. All GPIOs are configured as inputs. SCL and SDA are at VCC. Outputs are left floating or in tri-state mode.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise noted: $T_A = -40^{\circ}$ to $+85^{\circ}$ C, $V_{CC} = 1.65V - 3.6V$

| SYMBOL | PARAMETER | STANDARD MODE | | FAST MODE | | UNIT |
|---------------------|--|----------------------|------|----------------------|-----|------|
| | | I ² C-Bus | | I ² C-Bus | | |
| | | MIN | MAX | MIN | MAX | |
| f _{SCL} | Operating frequency | 0 | 100 | 0 | 400 | kHz |
| T _{BUF} | Bus free time between STOP and START | 4.7 | | 1.3 | | μs |
| T _{HD;STA} | START condition hold time | 4.0 | | 0.6 | | μs |
| T _{SU;STA} | START condition setup time | 4.7 | | 0.6 | | μs |
| T _{HD;DAT} | Data hold time | 0 | | 0 | | ns |
| T _{VD;ACK} | Data valid acknowledge | | 0.6 | | 0.6 | μs |
| T _{VD;DAT} | SCL LOW to data out valid | | 0.6 | | 0.6 | ns |
| T _{SU;DAT} | Data setup time | 250 | | 150 | | ns |
| T _{LOW} | Clock LOW period | 4.7 | | 1.3 | | μs |
| T _{HIGH} | Clock HIGH period | 4.0 | | 0.6 | | μs |
| T _F | Clock/data fall time | | 300 | | 300 | ns |
| T _R | Clock/data rise time | | 1000 | | 300 | ns |
| T _{SP} | Pulse width of spikes tolerance | 50 | | 50 | | ns |
| T _{D1} | I ² C-bus GPIO output valid | | 0.2 | | 0.2 | μs |
| T _{D4} | I ² C input pin interrupt valid | | 4 | | 4 | μs |
| T _{D5} | I ² C input pin interrupt clear | | 4 | | 4 | μs |
| T _{D15} | SCL delay after reset | 3 | | 3 | | μs |

FIGURE 6. I²C-BUS TIMING DIAGRAM

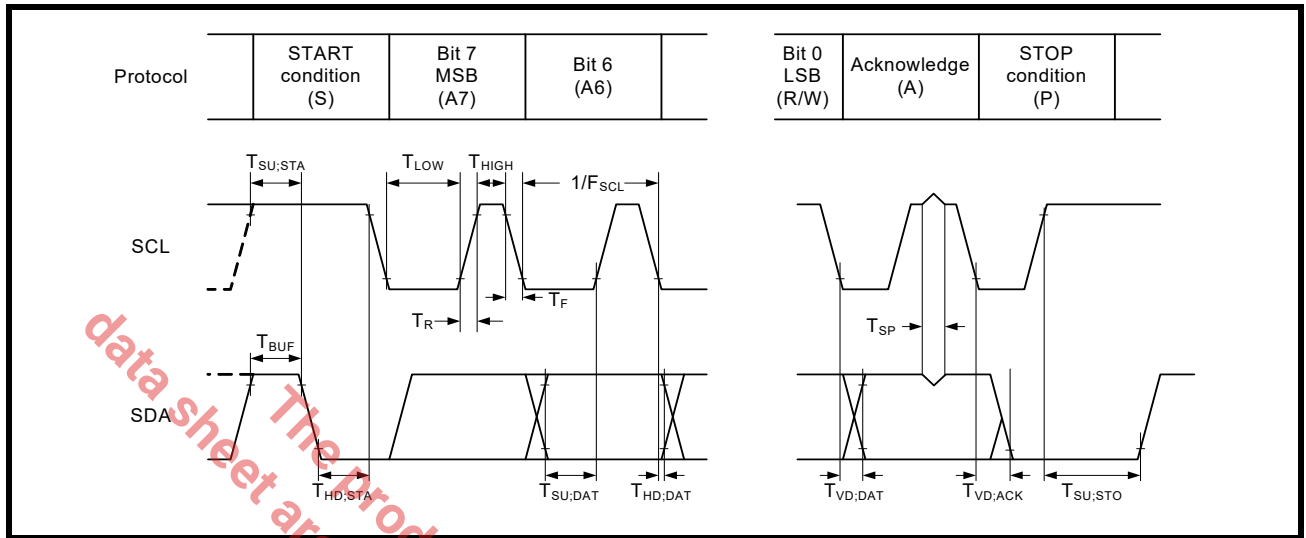


FIGURE 7. WRITE TO OUTPUT

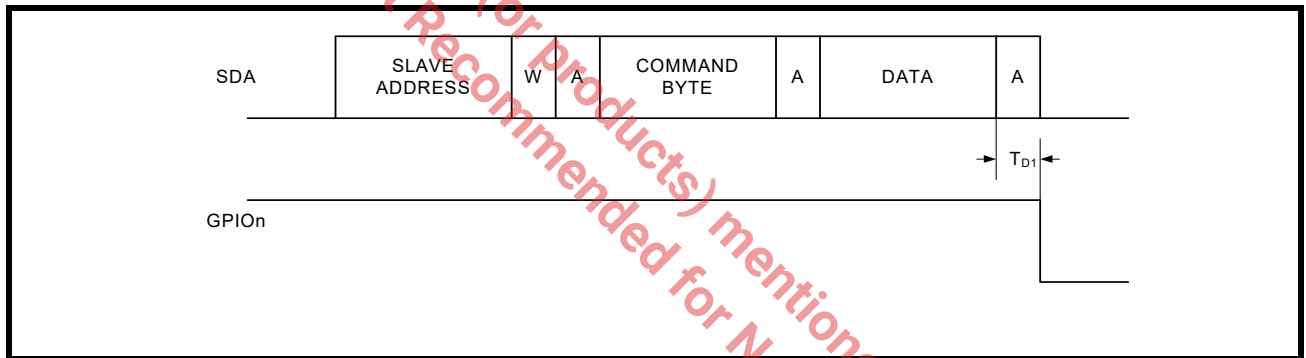
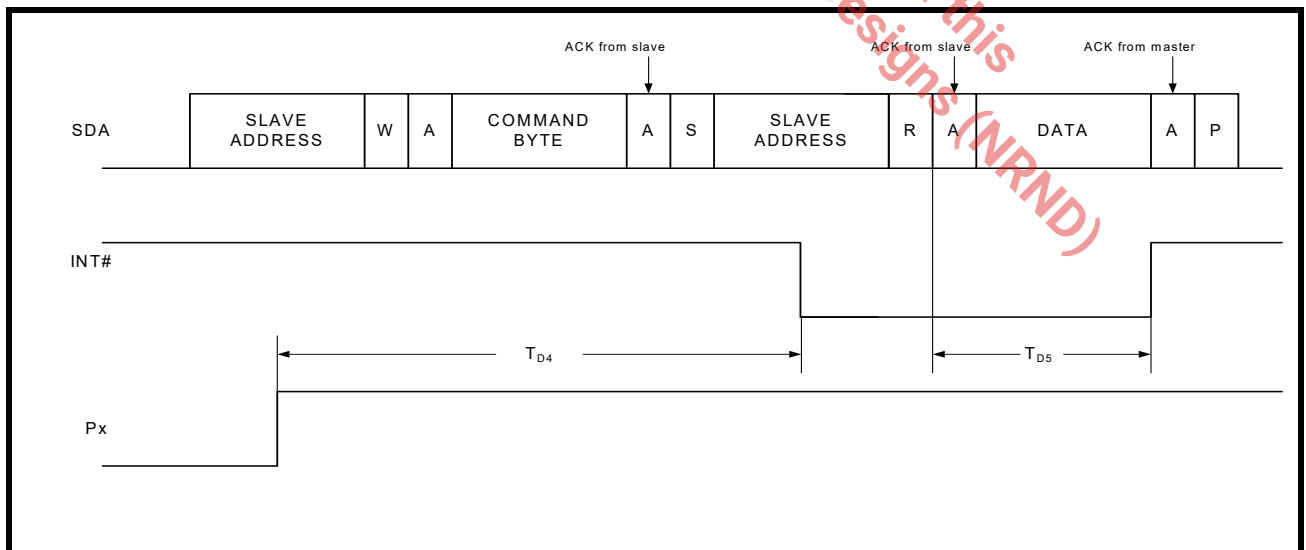
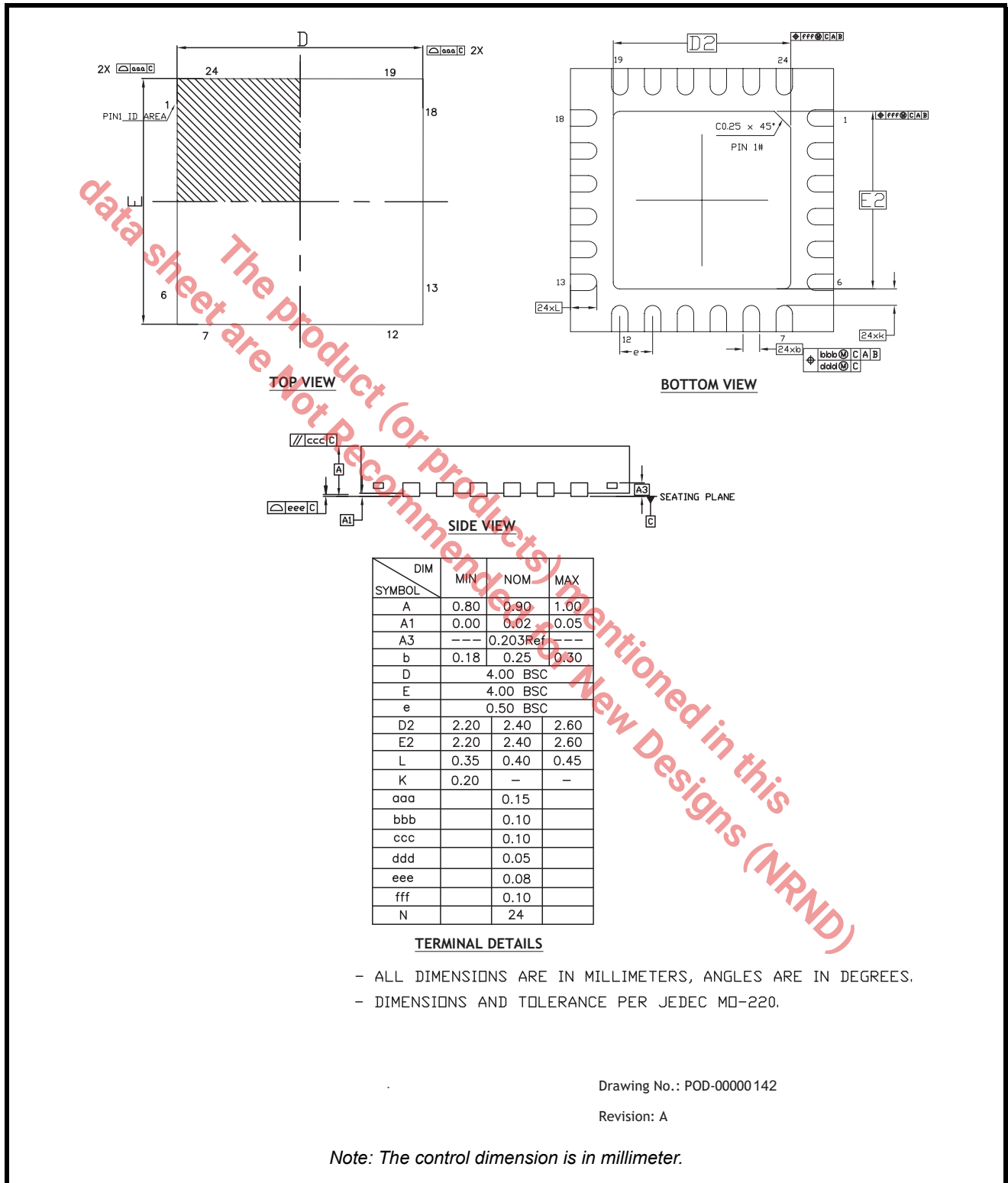


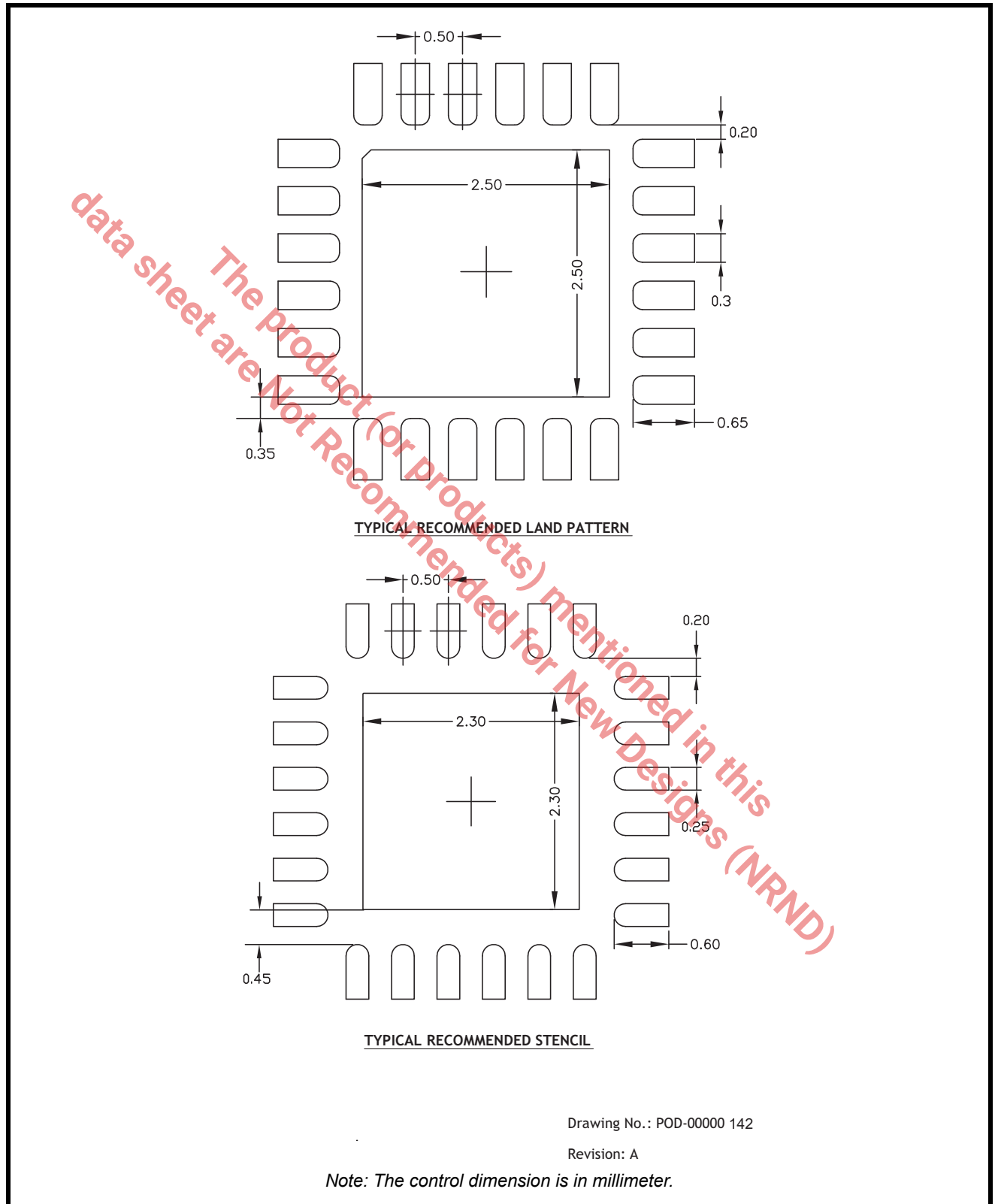
FIGURE 8. GPIO PIN INTERRUPT

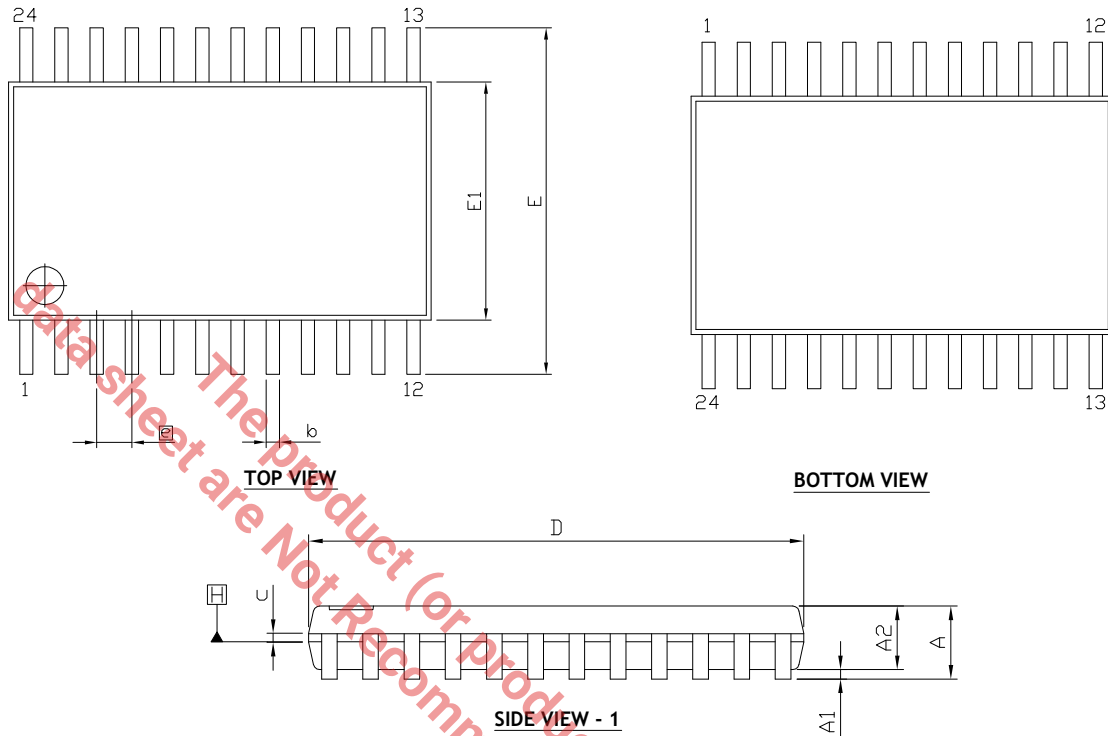


MECHANICAL DIMENSIONS (24 PIN QFN - 4 X 4 X 0.9 mm)
QFN-24 VERSION OBSOLETE


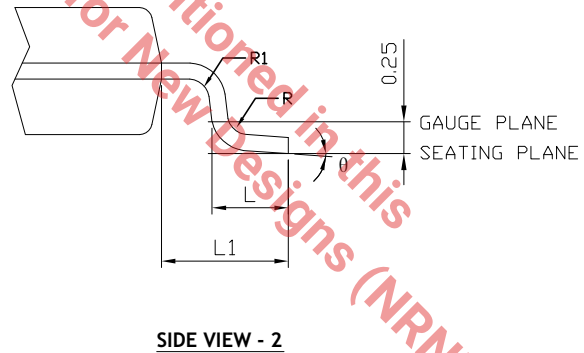
RECOMMENDED LAND PATTERN AND STENCIL (24 PIN QFN - 4 X 4 X 0.9 mm)

QFN-24 VERSION OBSOLETE



MECHANICAL DIMENSIONS (24 PIN TSSOP - 4.4 mm)


| DIM SYMBOL | MIN | NOM | MAX |
|------------|----------|------|------|
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | - | 0.30 |
| D | 7.70 | 7.80 | 7.90 |
| E | 6.40 BSC | | |
| e | 0.65 BSC | | |
| E1 | 4.30 | 4.40 | 4.50 |
| c | 0.09 | - | 0.20 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.0 REF | | |
| θ | 0 | - | 8 |
| R | 0.09 | - | - |
| R1 | 0.09 | - | - |
| N | | 24 | |

TERMINAL DETAILS


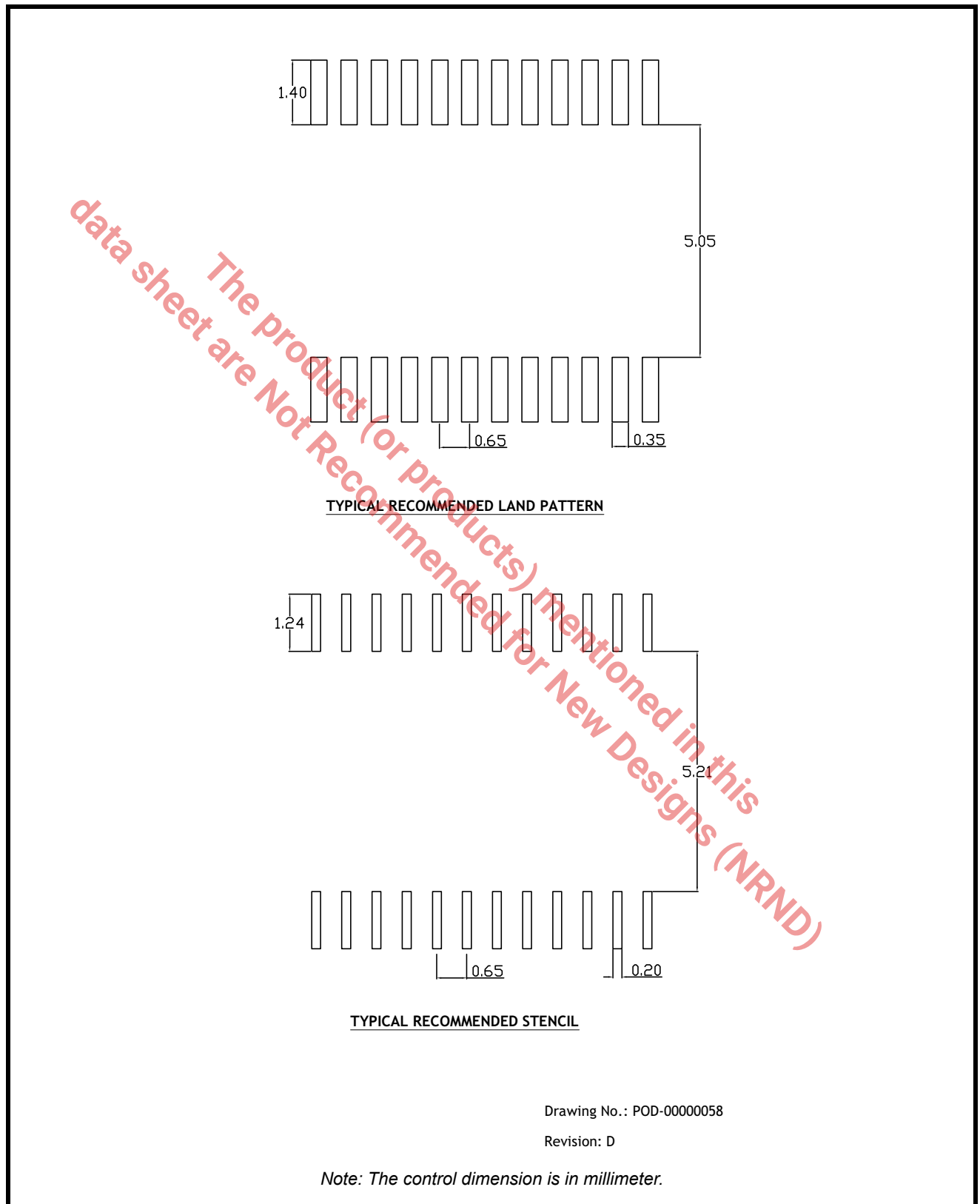
- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-153.

Drawing No.: POD-0000058

Revision: D

Note: The control dimension is in millimeter.

RECOMMENDED LAND PATTERN AND STENCIL (24 PIN TSSOP - 4.4 mm)



REVISION HISTORY

| DATE | REVISION | DESCRIPTION |
|----------------|----------|--|
| September 2011 | 1.0.0 | Final Datasheet. |
| August 2020 | 1.0.1 | Update to MaxLinear logo. Update Ordering Information. |
| March 9, 2022 | 1.0.2 | Updated: <ul style="list-style-type: none"> ■ "GPIO Configuration Register 1 (GCR1) - Read/Write" section. ■ "GPIO Configuration Register 2 (GCR2) - Read/Write" section. ■ Input Internal Pull-up Enable/Disable Register 1 (PUR1) - Read/Write ■ Input Internal Pull-up Enable/Disable Register 2 (PUR2) - Read/Write ■ "Input Interrupt Enable Register 1 (IER1) - Read/Write" section. ■ "Input Interrupt Enable Register 2 (IER2) - Read/Write" section. ■ "Mechanical Dimensions (24 pin QFN)" figure. ■ "Recommended Land Pattern and Stencil (24 pin QFN)" figure. ■ "Mechanical Dimensions (24 pin TSSOP)" figure. ■ "Recommended Land Pattern and Stencil (24 pin QFN)" figure. |



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