## GENERAL DESCRIPTION

The XRA1404 is an 8-bit GPIO expander with an SPI interface. After power-up, the XRA1404 has internal 100K ohm pull-up resistors on each I/O pin that can be individually enabled.

In addition, the GPIOs on the XRA1404 can individually be controlled and configured. As outputs, the GPIOs can be outputs that are high, low or in three-state mode. The three-state mode feature is useful for applications where the power is removed from the remote devices, but they may still be connected to the GPIO expander.

As inputs, the internal pull-up resistors can be enabled or disabled and the input polarity can be inverted. The interrupt can be programmed for different behaviors. The interrupts can be programmed to generate an interrupt on the rising edge, falling edge or on both edges. The interrupt can be cleared if the input changes back to its original state or by reading the current state of the inputs.

The XRA1404 is available in 16-pin QFN and 16-pin TSSOP packages.

QFN-16 version available, TSSOP-16 version obsolete



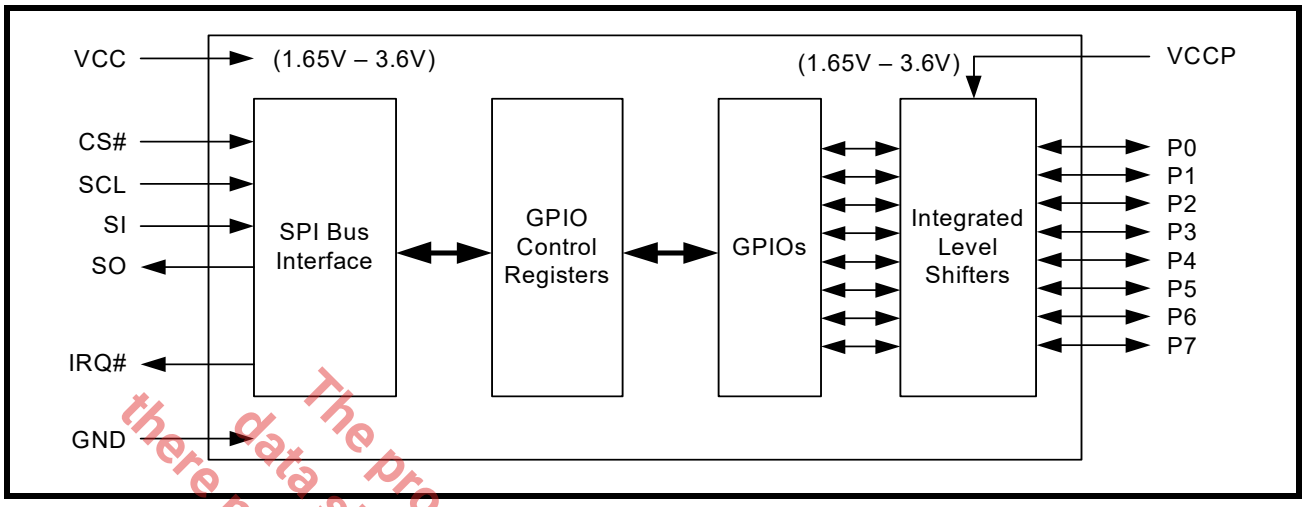
### *FEATURES*

- 1.65V to 3.6V operating voltage
- Integrated level shifters
- 8 General Purpose I/Os (GPIOs)
- 5V tolerant inputs
- Maximum stand-by current of 1uA at +1.8V
- SPI bus interface
  - SPI Clock Frequency up to 26MHz
- Individually programmable inputs
  - Internal pull-up resistors
  - Polarity inversion
  - Individual interrupt enable
  - Rising edge and/or Falling edge interrupt
  - Input filter
- Individually programmable outputs
  - Output Level Control
  - Output Three-State Control
- Open-drain active low interrupt output
- 3kV HBM ESD protection per JESD22-A114F
- 200mA latch-up performance per JESD78B

### *APPLICATIONS*

- Personal Digital Assistants (PDA)
- Cellular Phones/Data Devices
- Battery-Operated Devices
- Global Positioning System (GPS)
- Bluetooth

**FIGURE 1. XRA1404 BLOCK DIAGRAM**



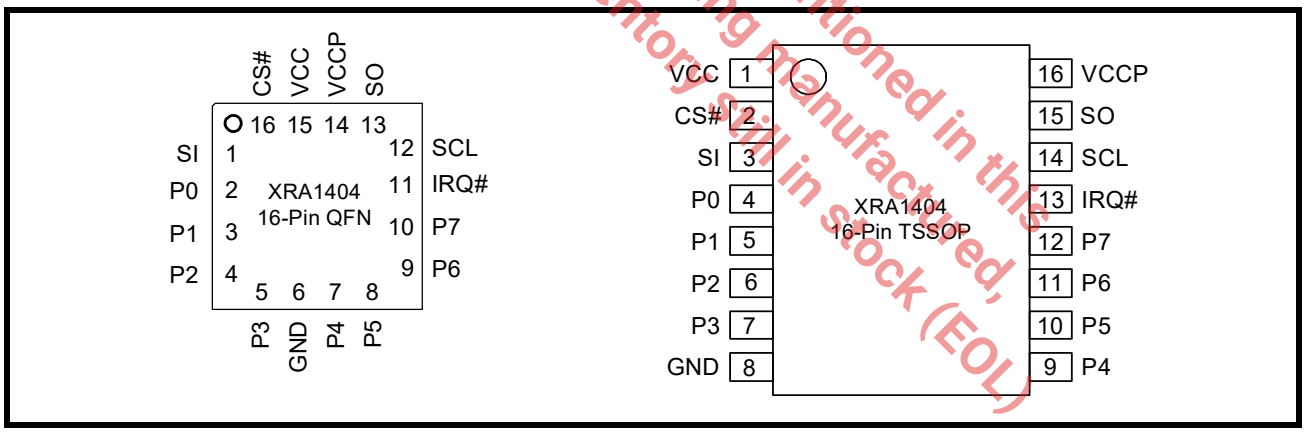



## *ORDERING INFORMATION*

| PART NUMBER | NUMBER OF GPIOS | OPERATING TEMPERATURE RANGE | PACKAGE | PACKAGE METHOD | LEAD FREE |
|---|---|---|---|---|---|
| XRA1404IL16TR-F | 8 | -40°C to +85°C | QFN-16 | Tape and Reel | Yes |

***NOTE:*** *For more information about part numbers, as well as the most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/XRA1404.*

**FIGURE 2. PIN OUT ASSIGNMENTS - XRA1404 QFN-16 VERSION AVAILABLE, TSSOP-16 VERSION OBSOLETE**



## PIN DESCRIPTIONS

**Pin Description** **QFN-16 version available, TSSOP-16 version obsolete**

| NAME | QFN-16 PIN# | TSSOP-16 PIN# | TYPE | DESCRIPTION |
|---|---|---|---|---|
| **SPI INTERFACE** | | | | |
| SO | 13 | 15 | O | SPI serial data output. |
| SCL | 12 | 14 | I | SPI serial input clock. |
| IRQ# | 11 | 13 | OD | Interrupt output (open-drain, active LOW). |
| CS# | 16 | 2 | I | SPI bus chip select. |
| SI | 1 | 3 | I | SPI serial data input. |
| **GPIOs** | | | | |
| P0 | 2 | 4 | I/O | General purpose I/Os P0-P7. All GPIOs are configured as inputs upon power-up. |
| P1 | 3 | 5 | I/O | |
| P2 | 4 | 6 | I/O | |
| P3 | 5 | 7 | I/O | |
| P4 | 7 | 9 | I/O | |
| P5 | 8 | 10 | I/O | |
| P6 | 9 | 11 | I/O | |
| P7 | 10 | 12 | I/O | |
| **ANCILLARY SIGNALS** | | | | |
| VCCP | 14 | 16 | Pwr | 1.65V to 3.6V VCC supply voltage for GPIOs. |
| VCC | 15 | 1 | Pwr | 1.65V to 3.6V VCC supply voltage for SPI bus interface. |
| GND | 6 | 8 | Pwr | Power supply common, ground. |
| GND | Center Pad | - | Pwr | The exposed pad at the bottom surface of the package is designed for thermal performance. Use of a center pad on the PCB is strongly recommended for thermal conductivity as well as to provide mechanical stability of the package on the PCB. The center pad is recommended to be solder masked defined with opening size less than or equal to the exposed thermal pad on the package bottom to prevent solder bridging to the outer leads of the device. Thermal vias must be connected to GND plane as the thermal pad of package is at GND potential. |

**Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.**

## 1.0 FUNCTIONAL DESCRIPTIONS

### *1.1 SPI bus Interface*

The SPI interface consists of four lines: serial clock (SCL), chip select (CS#), slave output (SO) and slave input (SI). The serial clock, slave output and slave input can be as fast as 26 MHz. To access the device in the SPI mode, the CS# signal is asserted by the SPI master, then the SPI master starts toggling the SCL signal with the appropriate transaction information. The first bit sent by the SPI master includes whether it is a read or write transaction and the register being accessed. See Table 1 below.

**TABLE 1: SPI COMMAND BYTE FORMAT**

| BIT | FUNCTION |
|---|---|
| 7 | Read/Write#<br>Logic 1 = Read<br>Logic 0 = Write |
| 6:1 | Command Byte |
| 0 | Reserved |



**FIGURE 3. SPI WRITE**

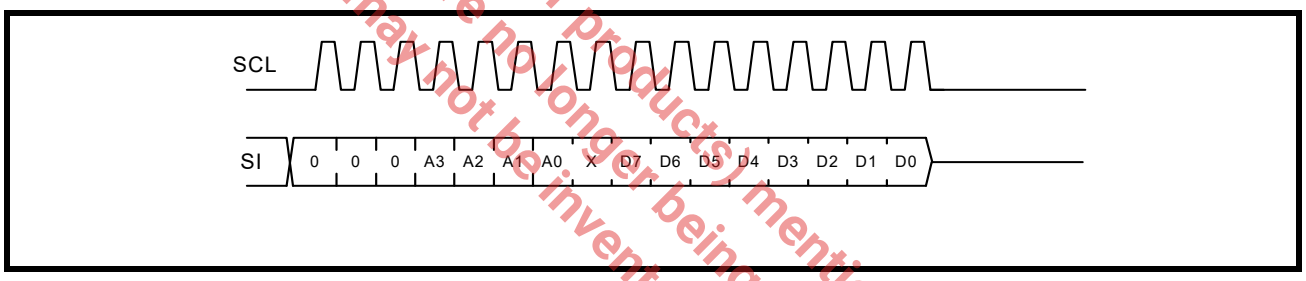
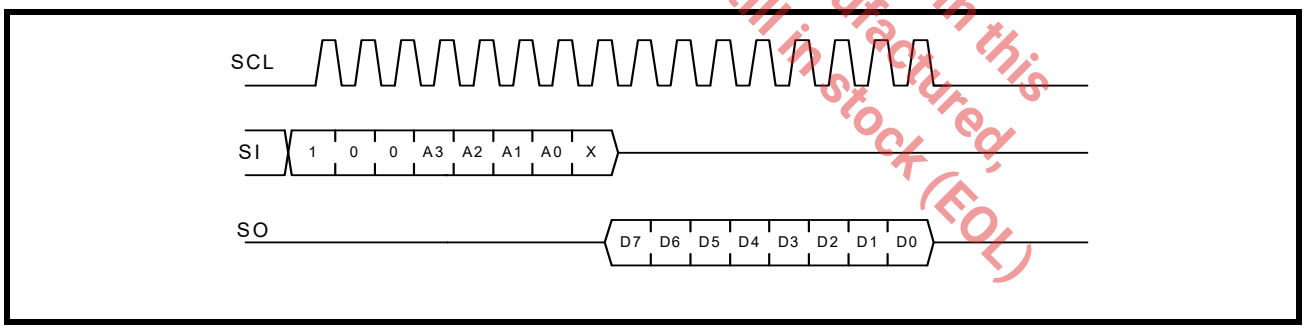



**FIGURE 4. SPI READ**




After the last read or write transaction, the SPI master will set the SCL signal back to its idle state (LOW).

### 1.1.1 SPI Command Byte

An SPI command byte is sent by the SPI master following the slave address. The command byte indicates the address offset of the register that will be accessed. Table 2 below lists the command bytes for each register.

**TABLE 2: COMMAND BYTE (REGISTER ADDRESS)**

| COMMAND BYTE | REGISTER NAME DESCRIPTION | READ/WRITE | DEFAULT VALUES |
|---|---|---|---|
| 0x00 | GSR - GPIO State | Read-Only | 0xXX |
| 0x01 | OCR - Output Control | Read/Write | 0xFF |
| 0x02 | PIR - Input Polarity Inversion | Read/Write | 0x00 |
| 0x03 | GCR - GPIO Configuration | Read/Write | 0xFF |
| 0x04 | PUR - Input Internal Pull-up Resistor Enable/Disable | Read/Write | 0x00 |
| 0x05 | IER - Input Interrupt Enable | Read/Write | 0x00 |
| 0x06 | TSCR - Output Three-State Control | Read/Write | 0x00 |
| 0x07 | ISR - Input Interrupt Status | Read | 0x00 |
| 0x08 | REIR - Input Rising Edge Interrupt Enable | Read/Write | 0x00 |
| 0x09 | FEIR - Input Falling Edge Interrupt Enable | Read/Write | 0x00 |
| 0x0A | IFR - Input Filter Enable/Disable | Read/Write | 0xFF |

## *1.2 Interrupts*

The table below summarizes the interrupt behavior of the different register settings for the XRA1404.

**TABLE 3: INTERRUPT GENERATION AND CLEARING**

| GCR BIT | IER BIT | REIR BIT | FEIR BIT | IFR BIT | INTERRUPT GENERATED BY: | INTERRUPT CLEARED BY: |
|---|---|---|---|---|---|---|
| 1 | 0 | X | X | X | No interrupts enabled (default) | N/A |
| 1 | 1 | 0 | 0 | 0 | A rising or falling edge on the input | Reading the GSR register or if the input changes back to its previous state (state of input during last read to GSR) |
| | | | | 1 | A rising or falling edge on the input and remains in the new state for more than 1075ns | |
| 1 | 1 | 1 | 0 | 0 | A rising edge on the input | Reading the GSR register |
| | | | | 1 | A rising edge on the input and remains high for more than 1075ns | |
| 1 | 1 | 0 | 1 | 0 | A falling edge on the input | Reading the GSR register |
| | | | | 1 | A falling edge on the input and remains low for more than 1075ns | |
| 1 | 1 | 1 | 1 | 0 | A rising or falling edge on the input | Reading the GSR register |
| | | | | 1 | A rising or falling edge on the input and remains in the new state for more than 1075ns | |
| 0 | x | x | x | x | No interrupts in output mode | N/A |

## 2.0 REGISTER DESCRIPTION

### *2.1 GPIO State Register (GSR) - Read-Only*

The status of P7 - P0 can be read via this register. A read will show the current state of these pins (or the inverted state of these pins if enabled via the PIR Register). Reading this register will clear an input interrupt (see Table 3 for complete details). Reading this register will also return the last value written to the OCR register for any pins that are configured as outputs (ie. this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.2 Output Control Register (OCR) - Read/Write*

When P7 - P0 are defined as outputs, they can be controlled by writing to this register. Reading this register will return the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.3 Input Polarity Inversion Register (PIR) - Read/Write*

When P7 - P0 are defined as inputs, this register inverts the polarity of the input value read from the Input Port Register. If the corresponding bit in this register is set to '1', the value of this bit in the GSR Register will be the inverted value of the input pin. If the corresponding bit in this register is set to '0', the value of this bit in the GSR Register will be the actual value of the input pin. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.4 GPIO Configuration Register (GCR) - Read/Write*

This register configures the GPIOs as inputs or outputs. Upon power-up, the GPIOs are configured as inputs by default. Setting these bits to '0' will enable the GPIOs as outputs. Setting these bits to '1' will enable the GPIOs as inputs. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.5 Input Internal Pull-up Enable/Disable Register (PUR) - Read/Write*

This register enables/disables the internal pull-up resistors for an input. Upon power-up, the internal pull-up resistors are disabled by default. Writing a '1' to these bits will enable the internal pull-up resistors. Writing a '0' to these bits will disable the internal pull-up resistors. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.6 Input Interrupt Enable Register (IER) - Read/Write*

This register enables/disables the interrupts for an input. Upon power-up, the interrupts are disabled by default. Writing a '1' to these bits will enable the interrupt for the corresponding input pins. See Table 3 for complete details of the interrupt behavior for various register settings. No interrupts are generated for outputs when GCR bit is 0. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.7 Output Three-State Control Register (TSCR) - Read/Write*

This register can enable/disable the three-state mode of an output. Writing a '1' to these bits will enable the three-state mode for the corresponding output pins. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.8 Input Interrupt Status Register (ISR) - Read-Only*

This register reports the input pins that have generated an interrupt. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.9 Input Rising Edge Interrupt Enable Register (REIR) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the rising edge. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.10 Input Falling Edge Interrupt Enable Register (FEIR) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the falling edge. Writing a '1' to these bits will make that input generate an interrupt on the rising edge only. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.11 Input Filter Enable Register (IFR) - Read/Write

By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns will generate an interrupt (if enabled). Pulses that are less than 225ns will be filtered and will not generate an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a '0' to these bits will disable the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs will generate an interrupt (if enabled). See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | 3.6 Volts |
| Supply current | 160 mA |
| Ground current | 200 mA |
| External current limit of each GPIO | 25 mA |
| Total current limit for GPIO[7:0] | 100 mA |
| Total supply current sourced by all GPIOs | 160 mA |
| Operating Temperature | -40° to +85°C |
| Storage Temperature | -65° to +150°C |
| Power Dissipation | 200 mW |

## TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

| | |
|---|---|
| Thermal Resistance (16-QFN) | theta-ja = 40°C/W, theta-jc = 26°C/W |
| Thermal Resistance (16-TSSOP) | theta-ja = 105°C/W, theta-jc = 20°C/W |

QFN-16 version available, TSSOP-16 version obsolete

# ELECTRICAL CHARACTERISTICS

## *DC ELECTRICAL CHARACTERISTICS*

**UNLESS OTHERWISE NOTED: TA = -40° TO +85°C, VCC IS 1.65V TO 3.6V**

| SYMBOL | PARAMETER | LIMITS 1.8V ± 10% MIN | LIMITS 1.8V ± 10% MAX | LIMITS 2.5V ± 10% MIN | LIMITS 2.5V ± 10% MAX | LIMITS 3.3V ± 10% MIN | LIMITS 3.3V ± 10% MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.3 | 0.2 | -0.3 | 0.5 | -0.3 | 0.8 | V | Note 1 |
| $V_{IH}$ | Input High Voltage | 1.4 | 5.5 | 1.8 | 5.5 | 2.0 | 5.5 | V | Note 1 |
| $V_{OL}$ | Output Low Voltage | | 0.4 | | 0.4 | | 0.4 | V<br>V<br>V | $I_{OL}$ = 6 mA<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 1.5 mA<br>Note 2 & Note 4 |
| $V_{OL}$ | Output Low Voltage | | 0.5 | | 0.5 | | 0.5 | V | $I_{OL}$ = 8 mA<br>Note 3 |
| $V_{OH}$ | Output High Voltage | 1.4 | | 1.8 | | 2.0 | | V<br>V<br>V | $I_{OL}$ = -4 mA<br>$I_{OL}$ = -2 mA<br>$I_{OL}$ = -0.2 mA<br>Note 2 |
| $V_{OH}$ | Output High Voltage | 1.2 | | 1.8 | | 2.6 | | V<br>V<br>V | $I_{OH}$ = -8 mA<br>$I_{OH}$ = -8 mA<br>$I_{OH}$ = -8 mA<br>Note 3 |
| $I_{IL}$ | Input Low Leakage Current | | ±10 | | ±10 | | ±10 | uA | |
| $I_{IH}$ | Input High Leakage Current | | ±10 | | ±10 | | ±10 | uA | |
| $C_{IN}$ | Input Pin Capacitance | | 5 | | 5 | | 5 | pF | |
| $I_{CC}$ | Power Supply Current | | 0.5 | | 1.0 | | 2.0 | mA | Test 1 |
| $I_{CC}$ | Power Supply Current | | 0.6 | | 1.2 | | 2.4 | mA | Test 2 |
| $I_{CCS}$ | Standby Current | | 1 | | 2 | | 5 | uA | Test 3 |
| $R_{GPIO}$ | GPIO pull-up resistance | 60 | 140 | 60 | 140 | 60 | 140 | kΩ | 100kΩ ± 40% |



***NOTE:*** *The Vcc comes from VCCP pin for the GPIOs and the VCC pin for the other signals;*

***NOTES:***

1. *For SPI input signals (SI, SCL) & GPIOs, A0, A1 and A2 signals;*
2. *For SPI output signal SO;*
3. *For GPIOs;*
4. *For IRQ# signal;*

Test 1: SCL frequency is 10 MHz with internal pull-ups disabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

Test 2: SCL frequency is 10 MHz with internal pull-ups enabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

Test 3: All inputs are steady at VCC or GND to minimize standby current. If internal pull-up is enabled, input voltage level should be the same as VCC. SCL and SI are at GND. CS# is at VCC. All GPIOs are configured as inputs. Outputs are left floating or in tri-state mode.

### *AC ELECTRICAL CHARACTERISTICS - SPI-BUS TIMING SPECIFICATIONS*

*Unless otherwise noted: TA=-40$^{o}$ to +85$^{o}$C, Vcc=1.65V - 3.6V*

| Symbol | Parameter | Limits 1.8V ± 10% | | | Limits 2.5V ± 10% | | | Limits 3.3V ± 10% | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| $f_{SCL}$ | Operating frequency | | | 15 | | | 26 | | | 26 | MHz | |
| $T_{CSS}$ | CS# to SCL setup time | 20 | | | 20 | | | 20 | | | ns | |
| $T_{CSH}$ | CS# to SCL hold time | 20 | | | 20 | | | 20 | | | ns | |
| $T_{DO}$ | SCL fall to SO valid time | | | 100 | | | 100 | | | 100 | ns | $C_L$ = 30 pF |
| $T_{DS}$ | SI to SCL setup time | 20 | | | 20 | | | 20 | | | ns | |
| $T_{DH}$ | SI to SCL hold time | 20 | | | 20 | | | 20 | | | ns | |
| $T_{CP}$ | SCL period | 66 | | | 38 | | | 38 | | | ns | $T_{CH}$ + $T_{CL}$ |
| $T_{CH}$ | SCL HIGH time | 30 | | | 15 | | | 15 | | | ns | |
| $T_{CL}$ | SCL LOW time | 30 | | | 15 | | | 15 | | | ns | |
| $T_{CSW}$ | CS# HIGH pulse width | 30 | | | 30 | | | 30 | | | ns | |
| $T_{D9}$ | SPI output data valid time | | 10 | | | 10 | | | 10 | | ns | |
| $T_{D13}$ | SPI input pin interrupt clear | | | 200 | | | 200 | | | 200 | ns | |

***Note:*** *The Vcc comes from the VCC pin.*

**FIGURE 5. SPI-BUS TIMING**

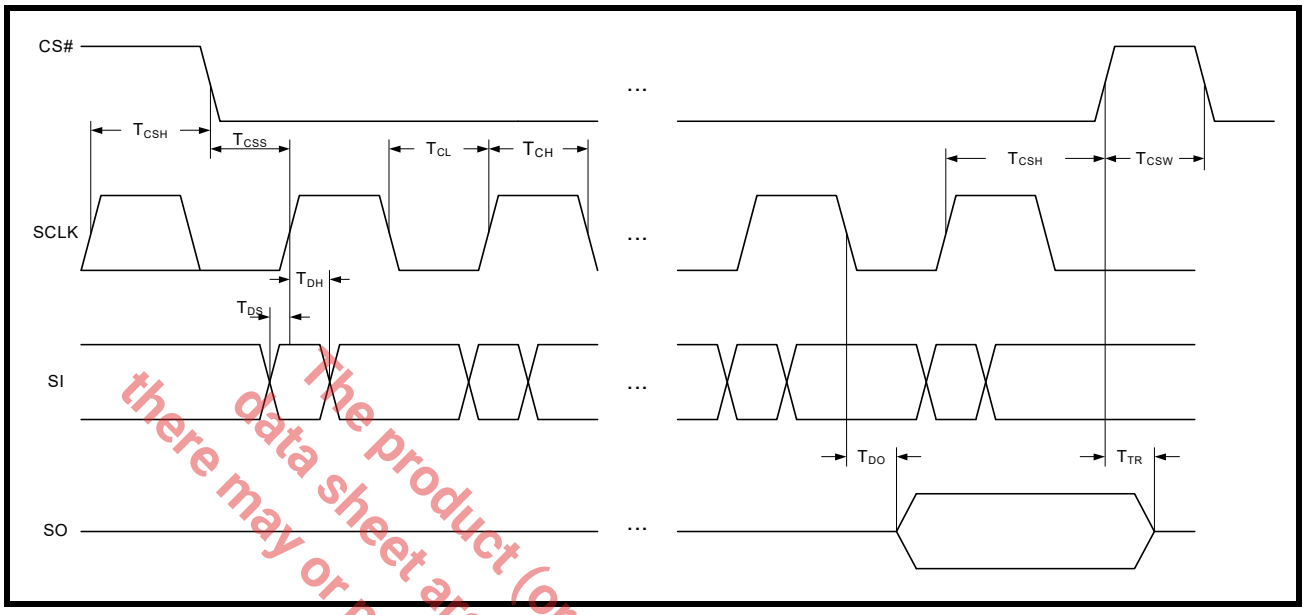



**FIGURE 6. READ INPUT PORT TO CLEAR GPIO INT**

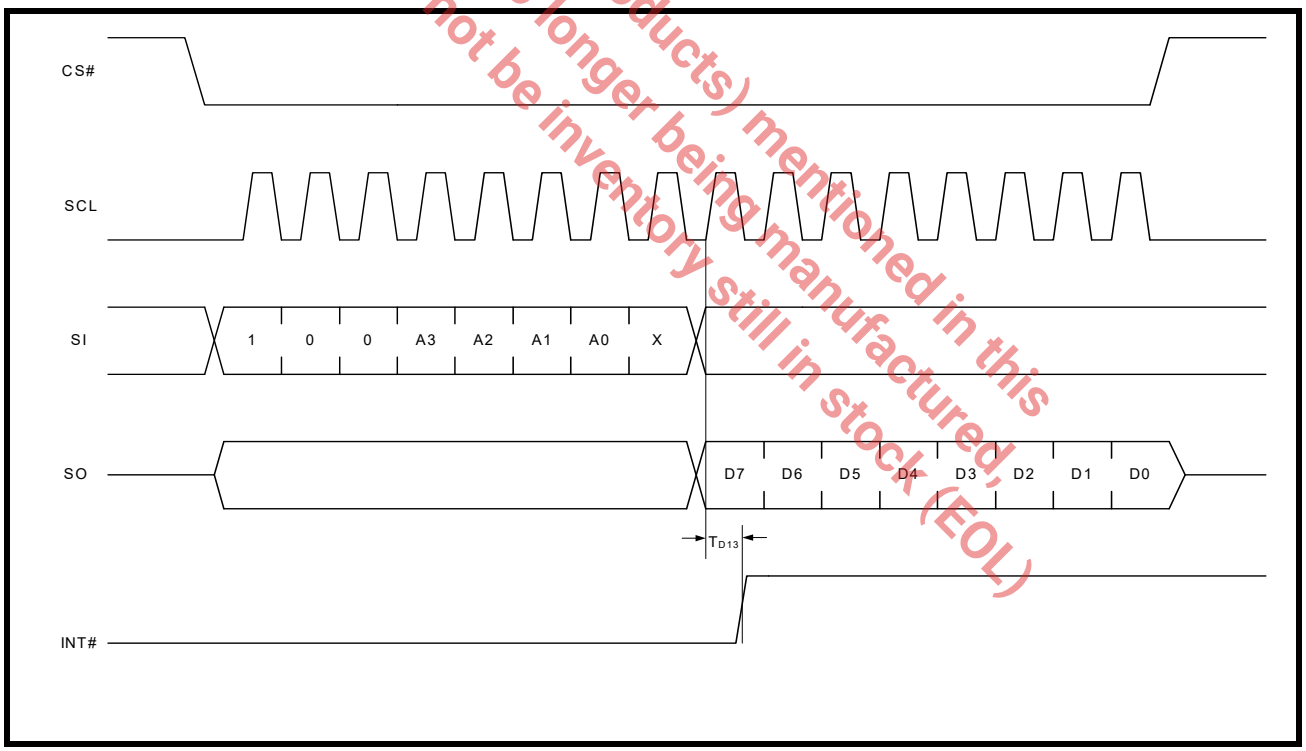
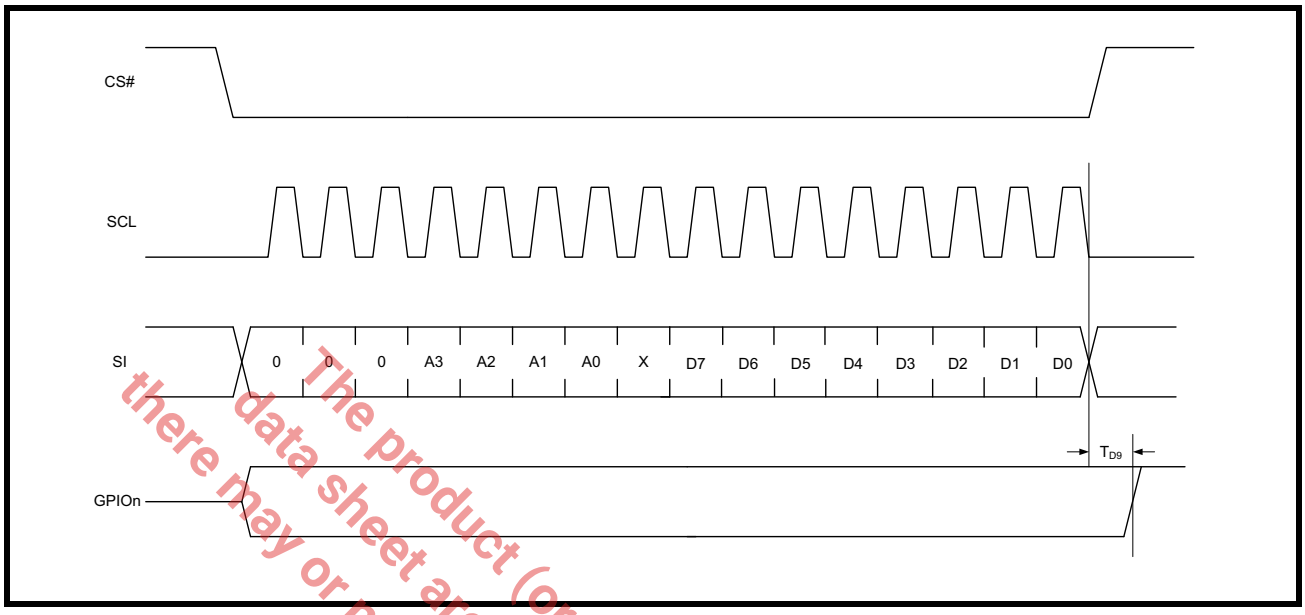
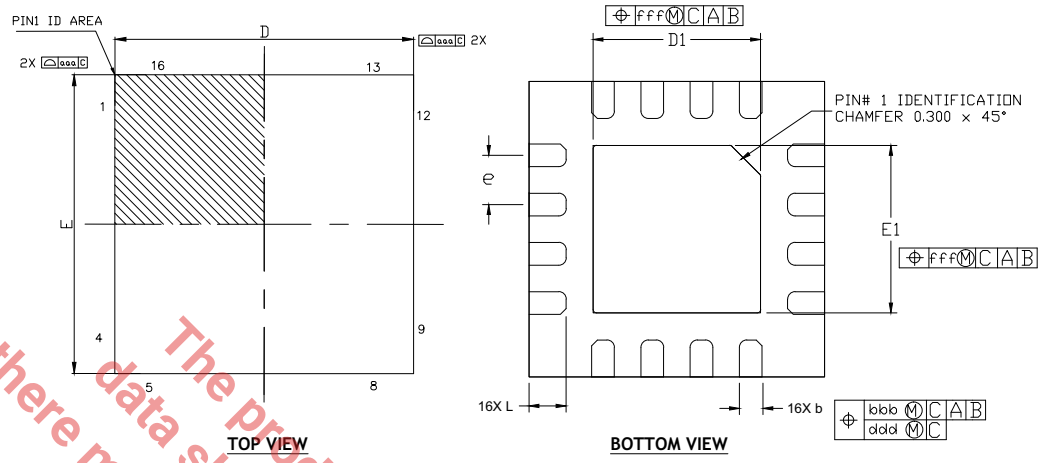
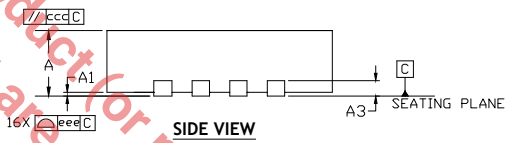


**FIGURE 7. SPI WRITE OUT TO GPIO SWITCH**



## MECHANICAL DIMENSIONS (16 PIN QFN - 3 X 3 X 0.9 mm)




| DIMENSION TABLE | | | |
|---|---|---|---|
| SYMBOL | MIN | NOM | MAX |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20Ref | |
| b | 0.18 | 0.25 | 0.30 |
| D | | 3.00 BSC | |
| E | | 3.00 BSC | |
| e | | 0.50 BSC | |
| D1 | 1.50 | 1.65 | 1.80 |
| E1 | 1.50 | 1.65 | 1.80 |
| L | 0.20 | 0.30 | 0.40 |
| K | 0.20 | – | – |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |
| N | | 16 | |

**TERMINAL DETAILS**

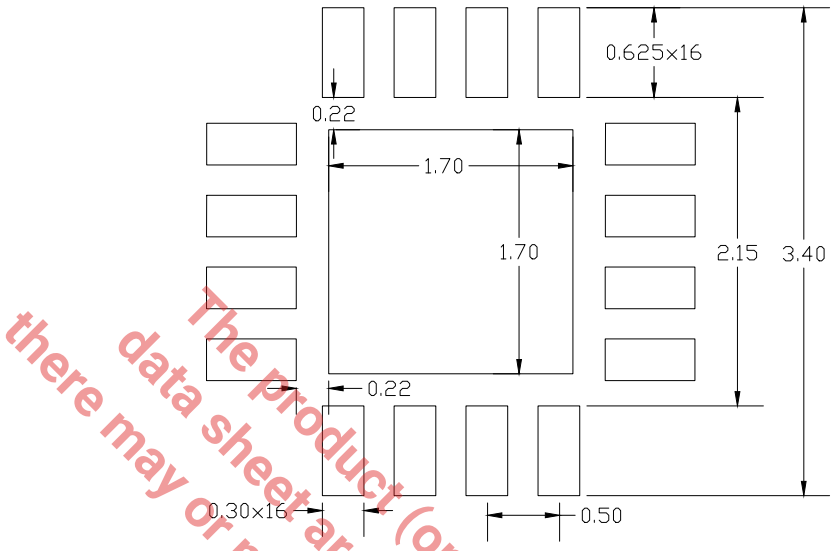
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

Drawing No.: POD- 00000138

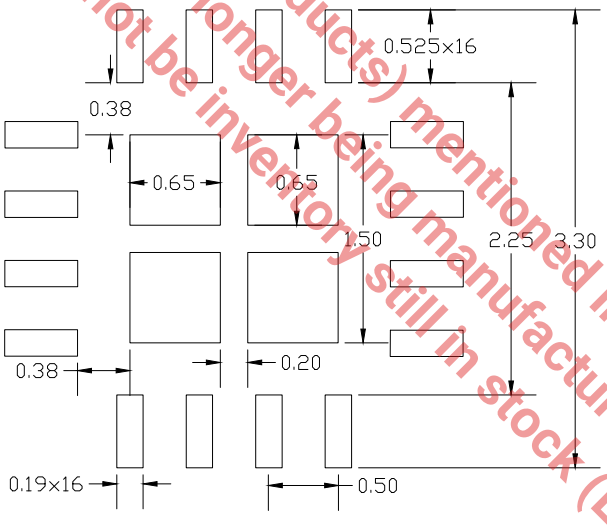
Revision: A

*Note: The control dimension is in millimeter.*

## RECOMMENDED LAND PATTERN AND STENCIL (16 PIN QFN - 3 X 3 X 0.9 mm)




TYPICAL RECOMMENDED LAND PATTERN




TYPICAL RECOMMENDED STENCIL

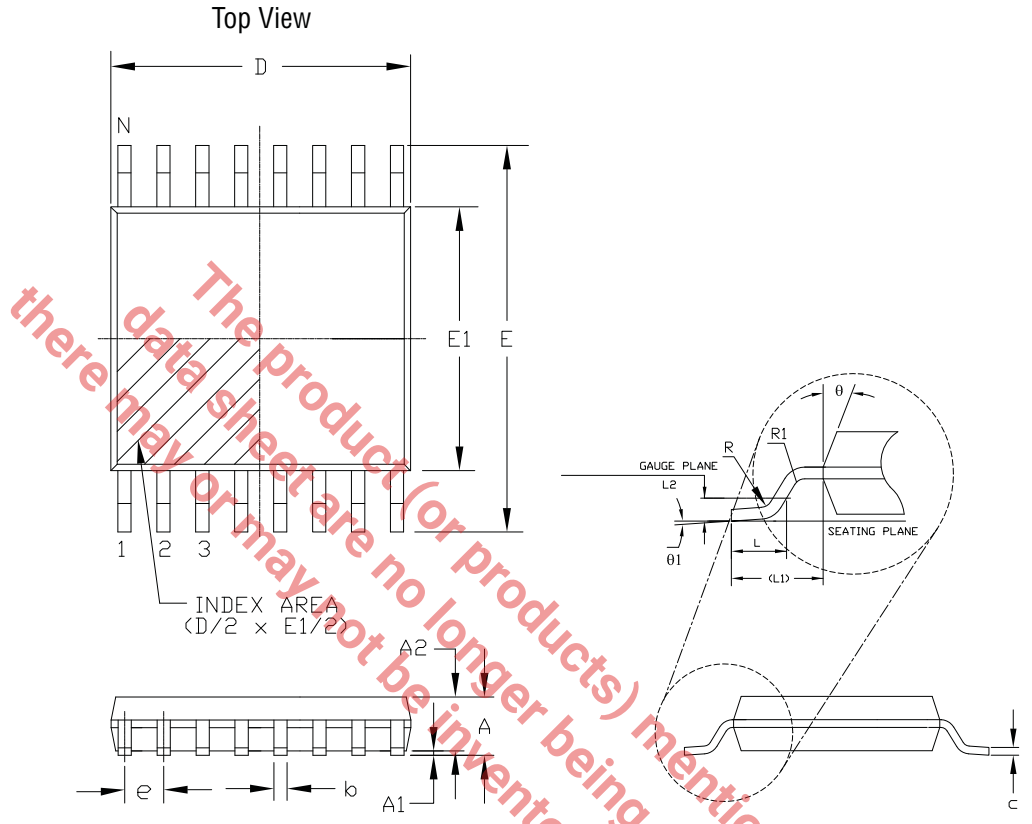
Drawing No.: POD- 00000138

Revision: A

*Note: The control dimension is in millimeter.*

## MECHANICAL DIMENSIONS (16 PIN TSSOP - 4.4 mm)

**16 PIN TSSOP VERSION OBSOLETE**




| 16 Pin TSSOP JEDEC MO-153 Variation AB | | | | | | |
|---|---|---|---|---|---|---|
| SYMBOLS | DIMENSIONS IN MM (Control Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 0.80 | 1.00 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | — | 0.30 | 0.007 | — | 0.012 |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| E | 6.40 BSC | | | 0.252 BSC | | |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.177 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R | 0.09 | — | — | 0.035 | — | — |
| R1 | 0.09 | — | — | 0.035 | — | — |
| θ | 12° REF | | | 12° REF | | |
| θ1 | 0° | — | 8° | 0° | — | 8° |
| D | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.200 |
| N | 16 | | | 16 | | |

Drawing No: POD-00000117
Revision: A

*Note: The control dimension is in millimeter.*

## *REVISION HISTORY*

| DATE | REVISION | DESCRIPTION |
|---|---|---|
| September 2011 | 1.0.0 | Final Datasheet. |
| February 4, 2022 | 1.0.1 | **Updated:**<br>■ In the "Pin Description" table, GPIOs parameter description.<br>■ "GPIO Configuration Register (GCR) - Read/Write" section.<br>■ "Input Internal Pull-Up Enable/Disable Register (PUR) - Read/Write" section.<br>■ "Input Interrupt Enable Register (IER) - Read/Write" section.<br>■ "Mechanical Dimensions (16 Pin QFN)" figure.<br>■ "Recommended Land Pattern and Stencil (16 Pin QFN)" figure.<br>■ "Mechanical Dimensions (16 Pin TSSOP)" figure.<br>**Added:**<br>■ In the "AC Electrical Characteristics - SPI-Bus Timing Specifications" table, "$T_{D9}$" parameter and "TYP" columns.<br>■ "SPI Write out to GPIO Switch" figure.<br>**Removed:**<br>■ In the "Features" section, "Active-low reset input" feature.<br>■ In the "Ordering Information" table, XRA1404IL16-F, XRA1404IG16-F, and XRA1404IG16TR-F obsolete part numbers. |



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